



Analysis and Design of a Delay-Locked Loop with Multiple Radiation-hardened Techniques

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Abstract

This paper presents a delay-locked loop (DLL) with multiple radiation-hardened techniques. A radiation-hardened charge pump (RH-CP) and a radiation-hardened voltage-controlled delay line (RH-VCDL) are proposed to mitigate effects on DLLs caused by single-event transient (SET). A lock detection module (LDM) is designed in the RH-CP to separate CP and VCDL when the DLL is locked. Thanks to LDM, the voltage transients caused by ion strikes on CP can be prevented from effecting the control voltage of VCDL and causing inverted lock error. A SET correction module (SCM) combined with sliced delay cells is used in the RH-VCDL to select the uncorrupted output and avoid missing pulses errors occurring at the output of DLL. The proposed DLL is designed in 22-nm CMOS process with an operation frequency of 5 GHz. Simulations at linear energy transfer (LET) between 40 and 100 MeV-cm²/mg show that RH-CP eliminates inverted lock error and RH-VCDL mitigates missing pulses generated by the DLL after ion strikes effectively.

Keywords Delay-locked loop · Single-event transient (SET) · Radiation-hardened techniques · Charge pump · Voltage-controlled delay line

1 Introduction

Delay-locked loops (DLLs) are widely used in clock distribution networks of electronic systems [3–5, 10, 12, 13]. Their main applications are high frequency clock generation, clock skew and jitter minimization and data synchronization. DLLs are critical modules which preserve the performance of the whole systems.

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With the development of space technology, the research about radiation-hardened DLLs has become a hot topic in recent years. In the space environment, there are a variety of energetic particles. When these charged particles pass through electronic devices, they transfer energy to the active silicon area, resulting in an undesirable effect called a single-event effect (SEE). Single-event transient (SET) is the focus research of SEE, which is the result of ionizing particles striking sensitive p–n junctions in an integrated circuit (IC) [8]. Missing pulses, inverted lock and duty cycle errors are three distinct types of transient errors that can occur after ion strikes on DLLs [9]. In order to ensure DLLs to work properly in space environment, there have been much research about radiation-hardened techniques [2, 6, 11, 14, 15].

According to the previous work, the voltage-controlled delay line (VCDL) was identified as the most sensitive sub-circuit. The strikes within any stage of the VCDL can result in output phase error and missing pulses. Ref. [7] hardens VCDLs by increasing the size of key transistors. However, missing pulses could still be observed at higher operating frequencies or reduced feature sizes. Charge pump (CP) is the second sensitive sub-circuit resulting in the phase displacement and persistent inverted lock error. Complementary current limiter circuit (CCL) is used in Ref. [16] to make CP radiation-hardened. Unfortunately, the method is less effective when the spurious current is smaller than the current threshold of CCL. The PFD has the lowest sensitivity to SET, which shows the least or no significant errors at the output after ion strikes.

In this paper, a delay-locked loop with multiple radiation-hardened techniques is proposed. The VCDL and CP are designed with radiation-hardened techniques to improve the performance of the proposed DLL under the effect of SET. A lock detection module (LDM) which is connected in series with CP is designed to monitor the state of DLL. CP and VCDL are separated by LDM when DLL is locked, so as to avoid voltage fluctuations due to SET on CP affecting the operation of VCDL. The proposed VCDL adopts slicing structure along with a SET correction module (SCM) to ensure the VCDL to operate properly under radiation. The slicing technique divides the VCDL into two parallel sub-VCDL paths, and SCM transmits the result of the sub-VCDL path without attack to the output by detecting two paths. The organization of the remaining part of this paper is as follows. Section 2 presents the architecture of the proposed DLL. Section 3 describes the simulation results. The conclusion is given in Sect. 4.

2 Architecture of the Proposed DLL

Figure 1 shows the mainly sub-circuit blocks of the proposed DLL: a start-up module, a phase frequency detector (PFD), a radiation-hardened charge pump (RH-CP), a loop filter and a radiation-hardened voltage-controlled delay line (RH-VCDL). The start-up module prevents harmonic locking of DLLs by producing a Setup signal which pulls the initial voltage of V_{CTRL} to V_{DD} . The PFD compares the phase difference between reference input (PFD_REF) and feedback output (PFD_FB). RH-CP and loop filter are combined together to generate V_{CTRL} controlling the delay of VCDL. RH-VCDL is composed of several variable delay elements connected in series and its output is fed back to start-up module. The total system is used for detecting the phase difference

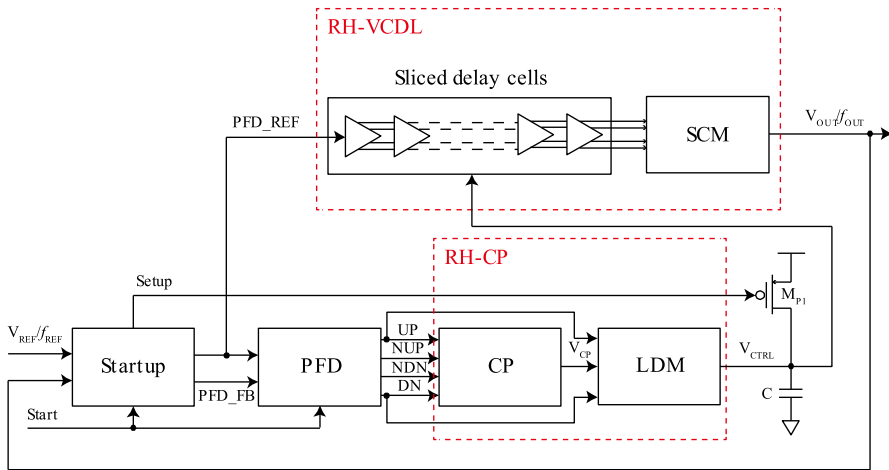


Fig. 1 Structure of the proposed DLL

between reference input and feedback output and aligning them. Finally, the DLL will be in lock until a minor phase difference detected by PFD does not change with time. The implementations of each sub-circuits will be given in later sections.

2.1 Start-Up Module

Figure 2 gives the structure of the start-up module, which is used to prevent harmonic locking of DLLs. The waveforms of the start-up module are shown in Fig. 3. When the system starts to work, both Start signal and Setup signal are at low level. In this state, PFD_REF and PFD_FB are both at low level. When Start signal changes from low level to high level, Path2 transmission path is on and FB is transmitted to PFD_FB. When the Setup signal becomes high, the Path1 transmission path is turned on and REF is transmitted to PFD_REF. The Setup signal is also connected to the gate of M_{P1} , which is shown in Fig. 1. When Setup signal is at low level, M_{P1} pulls the V_{CTRL} up to V_{DD} (0.9 V) as the initial voltage. At this time, the initial voltage on the capacitor is the maximum, which minimizes the initial delay of the VCDL to achieve anti-harmonic locking function.

2.2 PFD

The proposed PFD adopts D flip-flops (DFFs) composed of true single-phase clock (TSPC) logic unit, which is shown in Fig. 4. However, the initial state of such kind of PFD is uncertain. In order to solve the problem, the Start signal is introduced which is the same signal in the start-up module. In order to illustrate the working process of PFD, we use the case when REF leads FB as an example. The Start signal is used as the start-up signal of TSPC. When Start is logic 0, the voltages of nodes B and B' are pulled up to V_{DD} , which makes both UP and DN at logic 0. The Reset signal is at

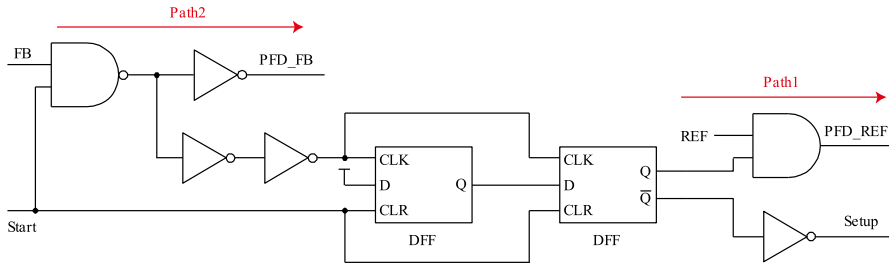


Fig. 2 Structure of the start-up module

low level as both NUP and NDN are logic 1. As a result, the voltage of node A is at high level. When the REF signal changes to high level, both M_4 and M_5 are enabled to pull node B down to logic 0 and UP rises to logic 1. After a period of time, when FB signal also rises to high level, node B' similarly falls to logic 0 and DN rises to logic 1. At this moment, both NUP and NDN are at low level, pulling the Reset signal to high level through the NOR. After that the voltages of nodes A and A' drop, while the voltages of nodes B and B' rise, making output signals UP and DN drop to logic 0.

2.3 RH-CP

In space environment, an ion strike on CP will change the amount of charge on the loop filter capacitor, thus directly affecting the V_{CTRL} by generating large burrs and therefore forcing the DLL to exit the lock mode. In the worst case, the voltage transients will even generate inverted lock error [9]. Figure 5 illustrates the inverted lock error when ion strikes occur on CP. The inverted lock error is persistent and results in a constant phase displacement.

In order to avoid the DLL losing the lock mode and generating inverted lock error caused by an ion strike on CP, a lock detection module (LDM) is proposed in this paper. Figure 6 shows the structure of the proposed RH-CP, which consists of a CP and an LDM. The CP charges or discharges the loop filter under the control of UP, NUP, DN and NDN, which are generated by the PFD containing phase error information, to provide a suitable V_{CTRL} for the VCDL. Figure 6b gives the structure of LDM mainly consisting of several control logics and a switch. LDM passes the current or not based on the state of DLL. When the DLL is not locked, the signals UP and DN are different and the output of exclusive OR (XOR) is a series of high and low levels controlling the switch S_0 on or off. The current can freely go through the switch S_0 when the switch is on, and can normally charge or discharge the capacitor without affecting the locking process of DLL. When the DLL is locked, the signals UP and DN are the same and the output of XOR is low, the switch S_0 is off. The LDM module prevents all current from passing through it. In this case, the large current burrs caused by SET can be restrained and will have no influence to VCDL as the output of CP is isolated from the control voltage of the VCDL by LDM.

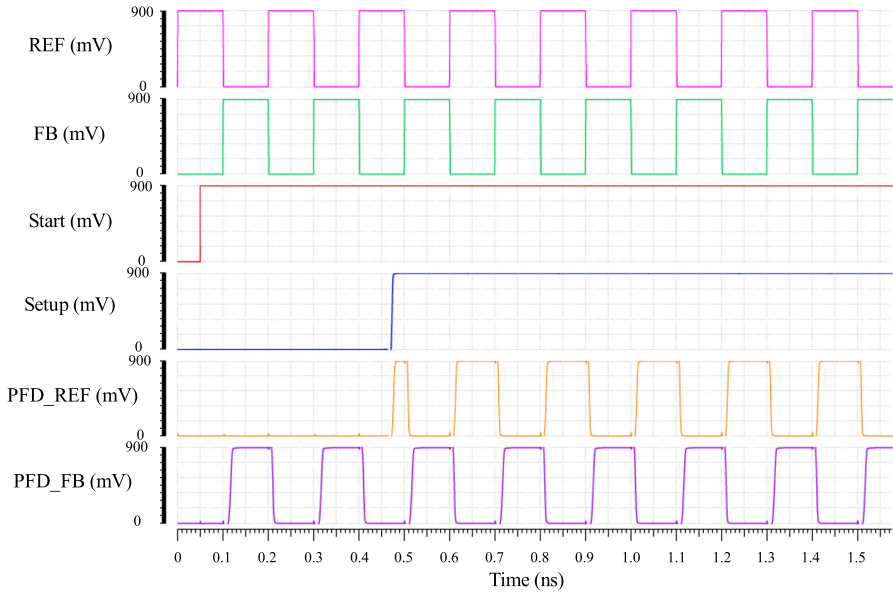


Fig. 3 Waveforms of start-up module

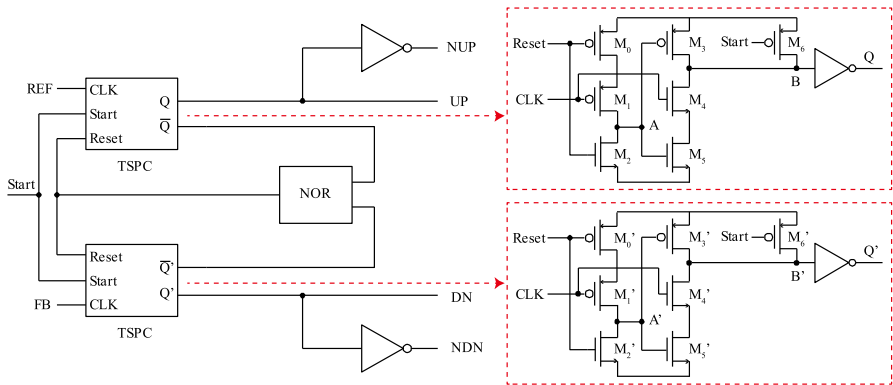
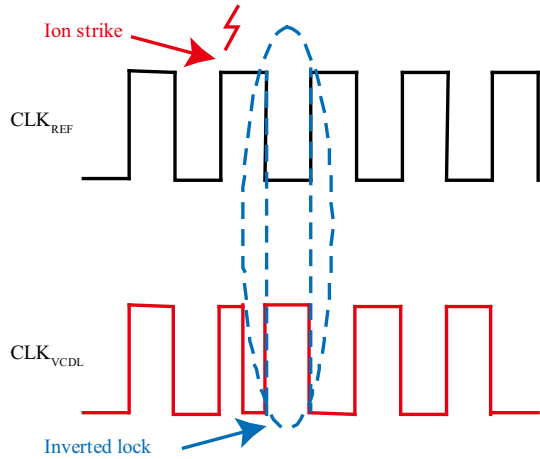


Fig. 4 Structure of PFD

The turn-off resistance of switch S_0 will affect the performance of LDM. When the turn-off resistance is small, the leakage is large, weakening the isolation capability of the LDM. In order to improve the turn-off resistance, T-type switch [1] is adopted in this paper. As shown in Fig. 6b, the T-type switch consists of three transmission gates forming a T-type structure. Figure 6b also gives the equivalent models when the T-type switch is on and off respectively. The turn-on resistance R_{ON} and turn-off resistance

Fig. 5 Illustration of inverted lock error



R_{OFF} of the T-type switches are calculated by:

$$R_{ON} = 2R_{small} + \frac{R_{small}^2}{R_{large}} \approx 2R_{small} = R_{MOS_ON} \tag{1}$$

$$R_{OFF} = 2R_{large} + \frac{R_{large}^2}{R_{small}} \gg 2R_{large} = R_{MOS_OFF} \tag{2}$$

where R_{MOS_ON} and R_{MOS_OFF} are turn-on resistance and turn-off resistance of traditional transmission gate switches, respectively. R_{ON} is almost the same as R_{MOS_ON} and R_{OFF} is increased enormously due to the T-type resistor compared with R_{MOS_OFF} . Figure 7 gives the simulation results about the turn-off resistance of the transmission gate and the T-type switch. The turn-off resistance of T-type switch is much greater than that of transmission gate switches. According to the results, the T-type switch helps to reduce the leakage and increase the turn-off resistance, which helps to improve the performance of LDM. The comparison results of LDM applying transmission gate and T-type switch will be discussed in later section.

2.4 RH-VCDL

The RH-VCDL consists of multiple cascaded delay cells. The ion strikes in either stage of delay cells will have an effect on the output of VCDL. Phase displacement error and number of missing pulses are used to identify the SET response of delay cells. The phase displacement error Φ_e and number of missing pulses N_{mis} are calculated as follows:

$$\Phi_e = \frac{t_e - T}{T} * 2\pi \tag{3}$$

$$N_{mis} = \frac{t_e - T}{T} \tag{4}$$

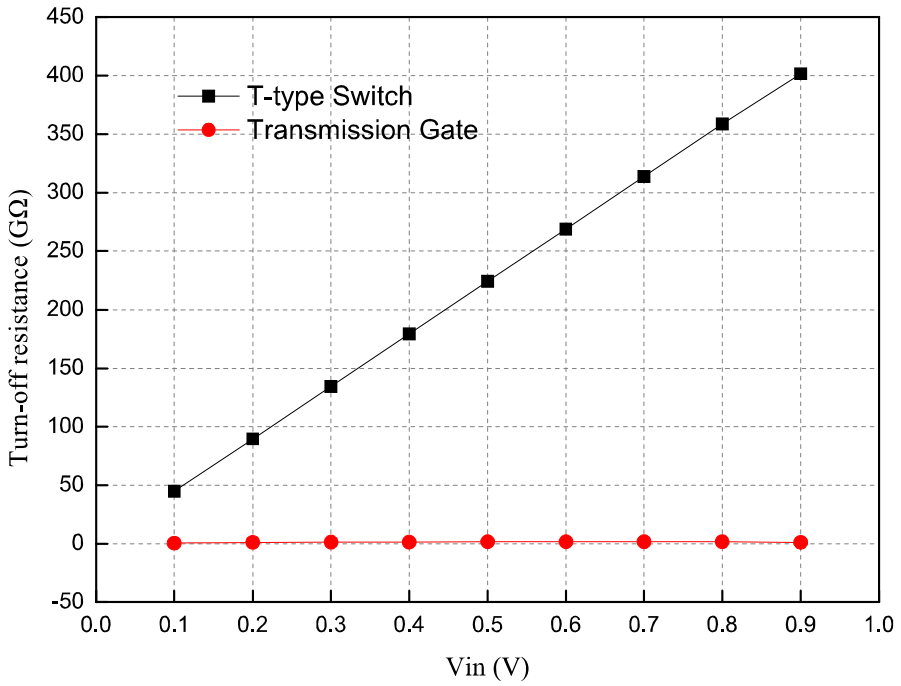


Fig. 7 Turn-off resistance of transmission gate and T-type switch

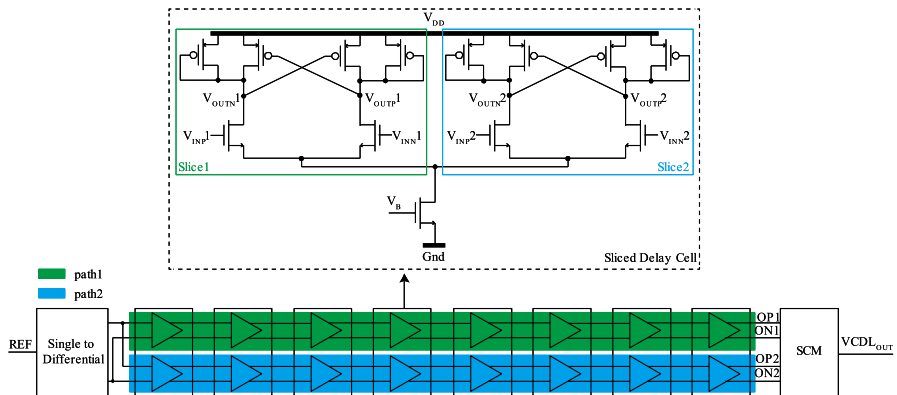


Fig. 8 Structure of the proposed RH-VCDL

where t_e is the time error and T the ideal input clock period. Missing pulses represent the case when one or more pulse(s) are absent from the output and each missing pulse equals an additional 2π of phase error.

Figure 8 shows the structure of the proposed RH-VCDL which consists of eight cascaded sliced delay cells. In order to harden the circuits, this paper adopts slicing

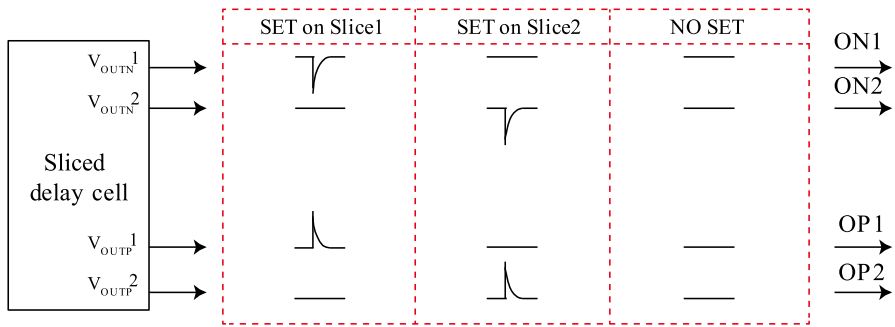


Fig. 9 Outputs of sliced delay cell when SETs occur on the proposed VCDL

technique to divide the VCDL into two parallel transmission paths. Slicing technique adopts the idea of redundant technique, which ensures that when one path is attacked by SET, the other path can operate normally. The SET correction module (SCM) is designed to select the uncorrupted clock when one of the two paths is attacked. The schematic of delay cell is also given in Fig. 8, which is split into two slices by halving the size of the transistors compared to the transistors used in delay cells not using slicing technique.

Figure 9 gives the three examples of outputs of two sliced delay cell paths with a SET on path1, with a SET on path2 and without SET, respectively. Due to the adoption of slicing technique, the proposed sliced delay cells will always generate an uncorrupted clock signal when SETs occur in the proposed VCDL. For example, if the output V_{OUTN1} is upset then the error will be mirrored to output V_{OUTP1} , but outputs V_{OUTP2} and V_{OUTN2} will generate a clock signal without a single-event transient.

Figure 10 gives the waveforms to explain the missing pulse of VCDL when SETs occur on path2. The VCDL was simulated at operating frequency of 5 GHz with linear energy transfer (LET) of 80 MeV-cm²/mg. As shown in Fig. 10, the P-terminal OP2 of path2 changes to constant logic 1, and N-terminal ON2 changes to constant logic 0 when path2 is attacked. Missing pulses occur on path2 while path1 is uncorrupted. The phase displacement error Φ_e is $11 \times 2\pi$, and number of missing pulses N_{mis} is 11.

The SCM designed in this paper is to detect whether SETs occur on the delay cells. If one of the two paths is attacked by SETs, the other uncorrupted path will be selected by SCM as the output of VCDL. The detailed structure of SCM is shown in Fig. 11. ON1 and OP1 are the differential outputs of path1, and ON2 and OP2 are the differential outputs of path2. The logic highlighted by red rectangle is designed to generate the selection signal S of multiplexer (MUX). MUX is a selector to choose the uncorrupted path as the output of VCDL according to the selection signal S.

During the working process of SCM, the XOR detects whether there is SET on delay cells and generates a control signal which is used as the trigger signal of DFFs. When there is no SET, the outputs of two sliced delay cell paths (ON1 and ON2) will always be the same which is shown in Fig. 10. The control signal will be low voltage level. When one of the sliced paths is hit by SET, ON1 and ON2 will be different. The voltage level of control signal will change from low to high and form a rising edge

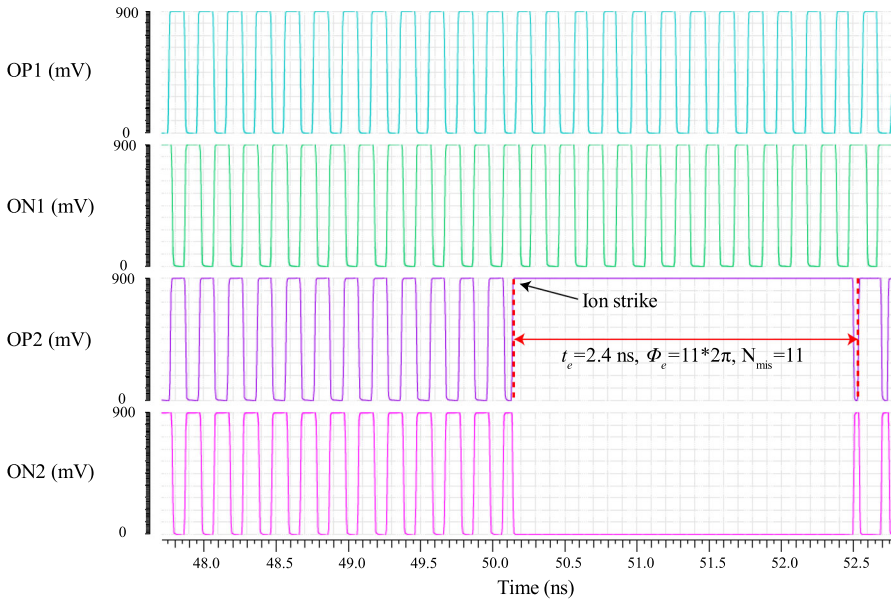


Fig. 10 Waveforms of sliced delay cell when path2 is attacked by SETs

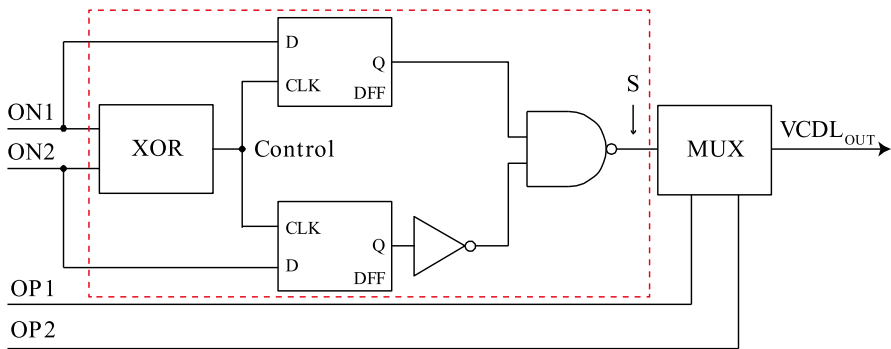


Fig. 11 Structure of SCM

trigger signal, which is used as the trigger signal of DFF. DFF will be controlled by the rising edge signal and transmit the input signal to the output to form the signal controlling MUX.

The output of MUX should be illustrated in three cases. When path2 is hit, the value of selection signal S will be logic 0. MUX will choose OP1 as the output of VCDL_{OUT}. When path1 is hit, the value of selection signal S will be logic 1. MUX will choose OP2 as the output of VCDL_{OUT}. When there is no SET on both paths, the value of selection signal S will be logic 1. MUX will choose OP2 as the output

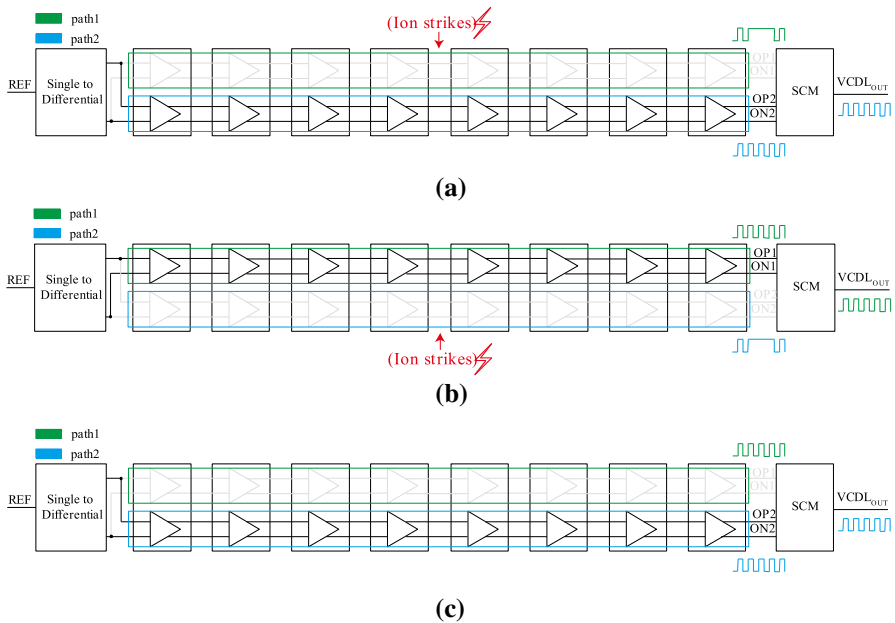


Fig. 12 Operation diagram of the proposed RH-VCDL in three cases: **a** A hit on path1, **b** A hit on path2, **c** No hit on both paths

of $VCDL_{OUT}$. Figure 12 shows the operation diagram of the proposed RH-VCDL in three cases.

3 Simulation Results of DLL

3.1 Set-Up of Simulation

The proposed DLL was implemented in 22-nm CMOS process with a supply voltage of 0.9 V. Figure 13 shows the current pulse generated by ion strikes with LET values between 40 and 100 MeV-cm²/mg, which is used to test the proposed radiation-hardened modules. The proposed DLL was simulated at a frequency of 5 GHz. A comparison of simulation results of the DLL with and without radiation-hardened techniques is illustrated in detail in the later section.

3.2 RH-CP

Figure 14 shows SET response of the proposed DLL and its corresponding transient output for an ion strike in CP at a LET = 100 MeV-cm²/mg for operating frequency of 5 GHz. Figure 14a shows the results of unhardened DLL which generates an inverted lock error, resulting from a voltage perturbation ΔV of 495 mV in V_{CTRL} . The comparison results of LDM applying transmission gate and T-type switch are illustrated

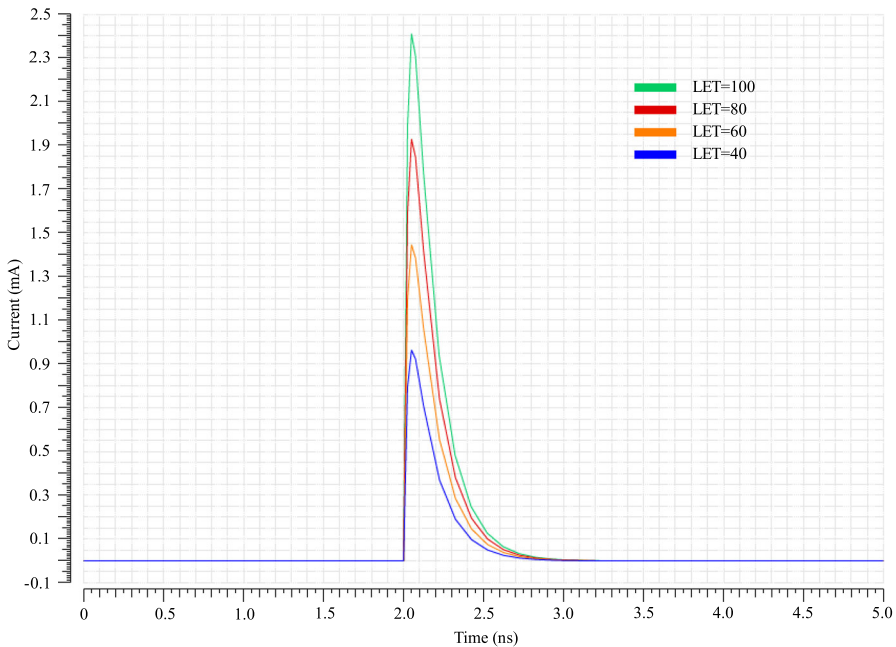


Fig. 13 Current pulse generated by ion strikes with LET values between 40 and 100 MeV-cm²/mg

in Fig. 14b and c, respectively. As shown in Fig. 14a and b, there is large voltage perturbation in V_{CTRL} which causes inverted lock errors in the output of DLL. As a result, a constant phase displacement can be observed between the reference clock and feedback clock. After using LDM with T-type switch in CP, the ΔV is reduced sharply and no inverted lock error occurs at the output which is shown in Fig. 14c. Figure 15 gives the value of ΔV for an ion strike in CP in three different cases with LET values between 40 and 100 MeV-cm²/mg.

3.3 RH-VCDL

Figure 16 illustrates the SET response generated by the proposed RH-VCDL at LET = 100 MeV-cm²/mg. The transient responses of the outputs of sliced delay cell paths (OP1 and OP2), selection signal S and the outputs of the DLL (VCDL_{OUT}) are compared in three different ion strike cases. Figure 16a represents the case when SET occurs on path1. There are missing pulses occurring at OP1 while OP2 stays uncorrupted. The selection signal S remains logic 1 choosing OP2 as the output and no missing pulses are observed at VCDL_{OUT}. Figure 16b shows the case when SET occurs on path2. OP2 generates missing pulses while OP1 stays uncorrupted. When there is no ion strike, selection signal S remains logic 1 choosing OP2 as the output. When SET occurs on Slice2, selection signal S changes to logic 0 and OP1 is selected to the output. As a result, no missing pulses are propagated into VCDL_{OUT}. Figure 16c gives the case when there is no ion strike on both paths. Selection signal S remains

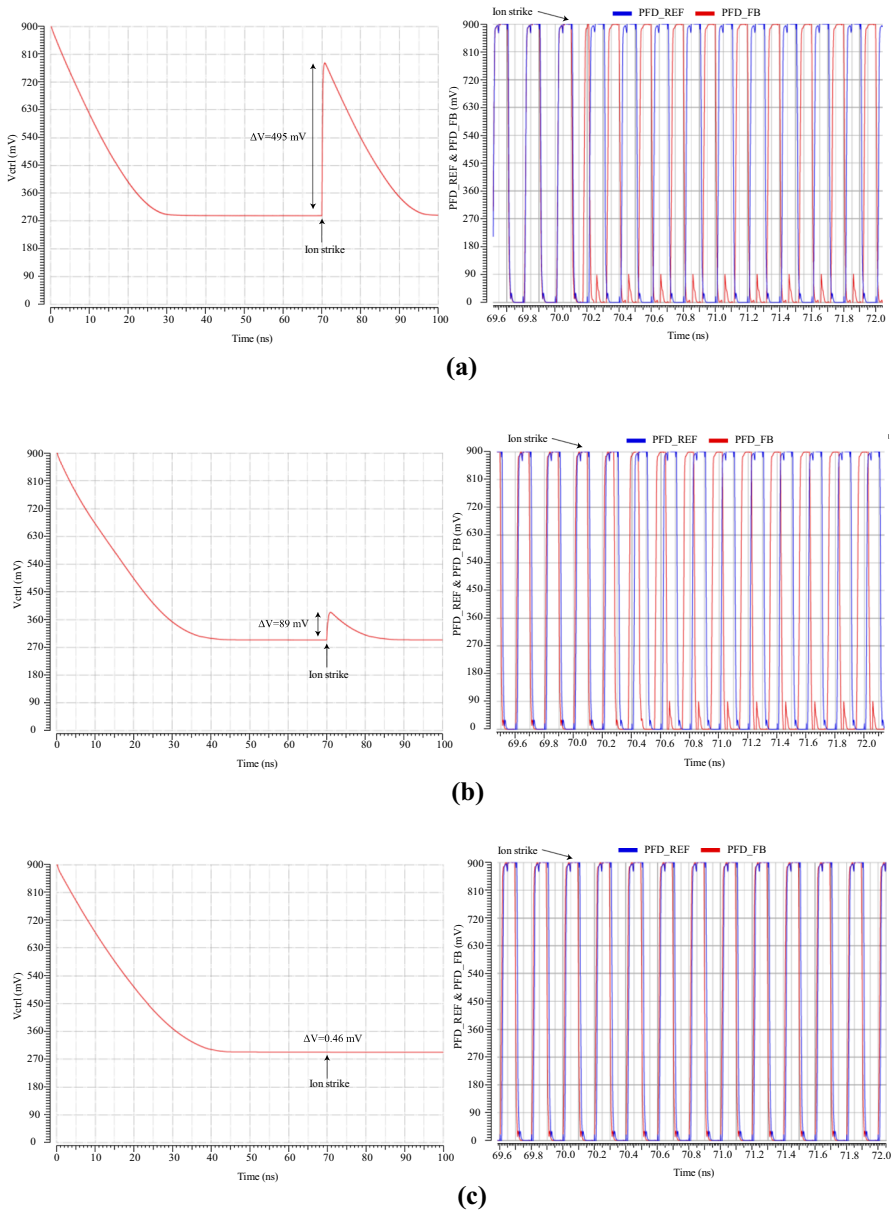


Fig. 14 SET response generated by the proposed RH-CP at $LET = 100 \text{ MeV-cm}^2/\text{mg}$: **a** Without LDM in CP, **b** With transmission gate in LDM, **c** With T-type switch in LDM

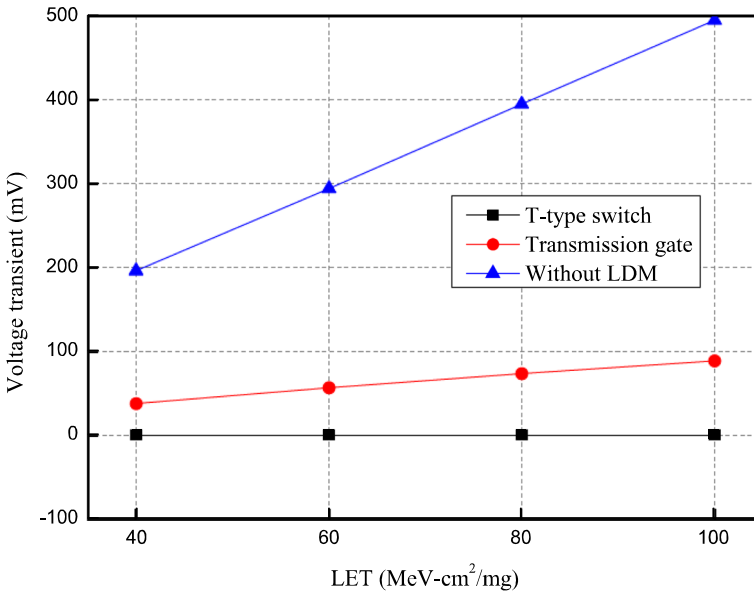


Fig. 15 Value of voltage transient ΔV for an ion strike in CP with LET values between 40 and 100 MeV-cm²/mg

logic 1 and send OP2 to the output. In all cases, no missing pulses were observed at the output of the DLL. Phase displacement error Φ_e and time error t_e caused by ion strikes are also marked in Fig. 16a and b. Figure 17 shows the simulation results of phase displacement error Φ_e for an ion strike in VCDL with LET values between 40 and 100 MeV-cm²/mg.

4 Conclusion

A delay-locked loop with multiple radiation-hardened techniques is presented in this paper. The radiation-hardened design is applied on CP and VCDL, respectively. The proposed RH-CP adopts a LDM as an isolation between CP and VCDL to prevent voltage transient caused by CP effecting the operation of VCDL. The voltage transient is sharply reduced and inverted lock error has been eliminated from the simulation results. The RH-VCDL uses slicing technique combined with SCM to choose the uncorrupted output, which is proved to eliminate missing pulses at the output of DLL effectively. Overall, the proposed radiation-hardened techniques should be applicable to a variety of different DLLs operating in space environment.

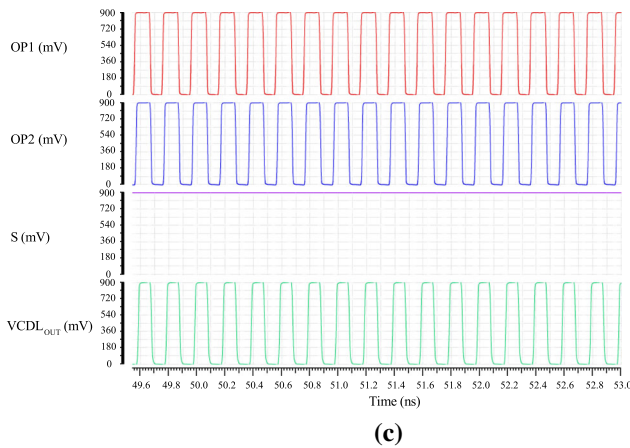
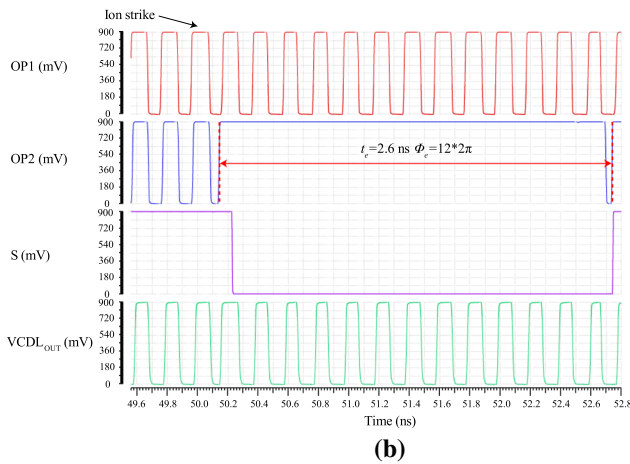
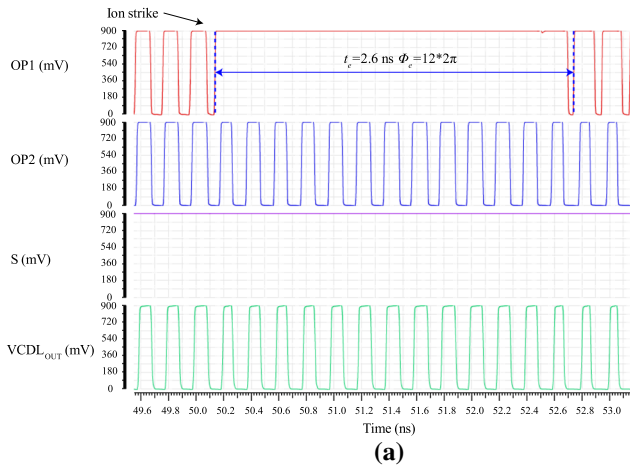


Fig. 16 SET response generated by the proposed RH-VCDL at a LET = 100 MeV-cm²/mg for: **a** A hit on path1, **b** A hit on path2, **c** No hit on both paths

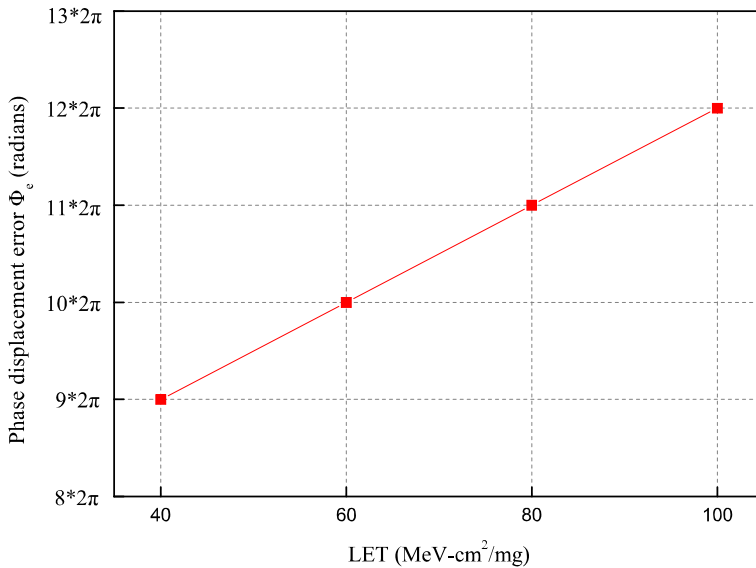


Fig. 17 Phase displacement error Φ_e for an ion strike in VCDL with LET values between 40 and 100 MeV-cm²/mg

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Data Availability The datasets generated during and/or analysed during the current study are available from the corresponding author on reasonable request.

Declarations

Conflict of interest The authors declare that they have no conflict of interest.

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