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V_{aq}-Assisted Low-Power Capacitor-Splitting Switching Scheme for SAR ADCs

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Abstract
In this paper, a novel four-level capacitor-splitting switching scheme for successive approximation register analog-to-digital converters is proposed. The fourth reference voltage V_{aq}, equal to $V_{REF}/4$, is introduced during the last bit-cycle to optimize capacitor area and power consumption. So, for a 10-bit SAR ADC, the capacitor area is reduced by 75%, and average switching energy of $-5.4\ CV_{REF}{}^2$ is achieved, which is 102.11% less than the monotonic switching method. The common-mode voltage remains at $V_{REF}/2$ except for the last two bit-cycles. 1% capacitor mismatch leads to root-mean-square (RMS) values of 0.321 LSB for DNL and INL. Inaccuracy of V_{CM}/V_{aq} has little effect on the accuracy of the SAR ADC. V_{aq} control logic is easier to design than those of other reference voltages. As a result, the proposed switching scheme offers a better trade-off between energy efficiency, capacitor saving, common-mode voltage variation, logic complexity, and accuracy. A 0.6-V 10-bit 20 KS/s SAR ADC in 0.18-μm 1P6M CMOS technology is designed, occupying an area of about $340 \times 380\ \mu m^2$. The SAR ADC with Nyquist rate input has ENOB, SNDR, and SFDR values of 9.57 bits, 59.41 dB, and 70.56 dB, respectively. It consumes 35.1 nW, resulting in a figure-of-merit (FoM) of 2.31 fJ/conversion-step.

Keywords Switching scheme · V_{aq}-assisted · Common-mode voltage · Capacitor-splitting · SAR ADC

1 Introduction

SAR ADCs have wide application in bio-electric signal conversion due to their low power consumption. A SAR ADC consists mainly of a comparator, double capacitive DACs, and SAR control logic. A dynamic latch comparator is often used to reduce

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power consumption. A scaling technology and a lowering power supply benefit digital SAR control logic. Thus, much attention has been being paid to reducing the switching energy of capacitive DACs, which focuses on energy-efficient switching techniques and reduction of DAC capacitor counts [1, 2, 4, 8, 9, 11, 13, 17, 21, 22, 24, 25, 29–32, 34, 37]. Capacitor-splitting switching scheme is proposed, reducing switching energy by 37% over the conventional one [8]. The monotonic switching method reduces energy consumption by 81% [11]. Switching techniques with two reference voltages (V_{REF} and ground) are not energy-efficient because of a large number of unit capacitors required. So, the third reference voltage V_{CM}, half of V_{REF}, is introduced [13, 17, 22, 29, 31]. The unit capacitor count is reduced by at least 75% using V_{CM} and top-plate sampling. The switching energy saves over 90%. To further decrease the switching energy, multiple switching methods are used, including the minus switching energy [24], the floating capacitor [1, 4, 25, 30, 32, 34], the charge recycling method [2], and the introduction of the fourth reference voltage V_{aq} [9, 21, 37], which is equal to $V_{REF}/4$. Nevertheless, each has its disadvantages. [1, 4, 25, 30, 32, 34] need many more switches and higher DAC logic complexity; the DAC control logic is complicated [2]; the common-mode voltage fluctuates wildly [9, 21, 37].

This paper applies V_{aq} to four dummy capacitors to create a four-level capacitor-splitting DAC switching technique. It achieves 102.11% less switching energy than the monotonic one for a 10-bit SAR ADC, which is better than [7, 11, 17, 26, 29, 31, 34, 36, 37]. The area of the capacitor can be reduced by 75%, which is superior to the results obtained from [11, 17, 31] and comparable to those obtained from [7, 26, 29, 34, 37]. Besides, the common-mode voltage does not change until the last two bit-cycles, which is a significant improvement over those described in [7, 11, 17, 26, 29, 31, 37]. In addition, the DAC control logic is not difficult to implement, which makes it superior to those presented in [34] and [36] and on par with those shown in [7]. Last but not least important, it is crucial to note that V_{CM}/V_{aq} does not have a significant impact on the accuracy of the SAR ADC, which is superior to [7, 17, 29, 31] and is on par with [26, 37]. Thus, it is a better trade-off in terms of energy efficiency, capacitor area, common-mode voltage variation, logic complexity, and accuracy. By utilizing the proposed switching scheme and careful circuit layout, the 10-bit SAR ADC consumes just 35.1 nW power at a sampling rate of 20 KS/s and achieves an ENOB of 9.57 bits.

The rest of this paper is organized as follows. Section 2 discusses the proposed V_{aq}-assisted capacitor-splitting switching scheme. In Sect. 3, non-ideal effects are investigated and evaluated. These effects include capacitor mismatch, parasitic capacitance, and reference voltage mismatch. Implementation of DAC control logic can be found in Sect. 4. Section 5 contains the post-layout simulation results. The conclusion is delivered in the final section.

2 Proposed V_{aq}-Assisted Capacitor-Splitting Switching Scheme

Capacitor-splitting structure [8, 10, 12, 19, 20, 26, 27, 33, 35] is utilized, resulting in low power consumption and high linearity. The N-bit SAR ADC with the proposed capacitor-splitting structure is shown in Fig. 1, consisting of the MSB and the LSB

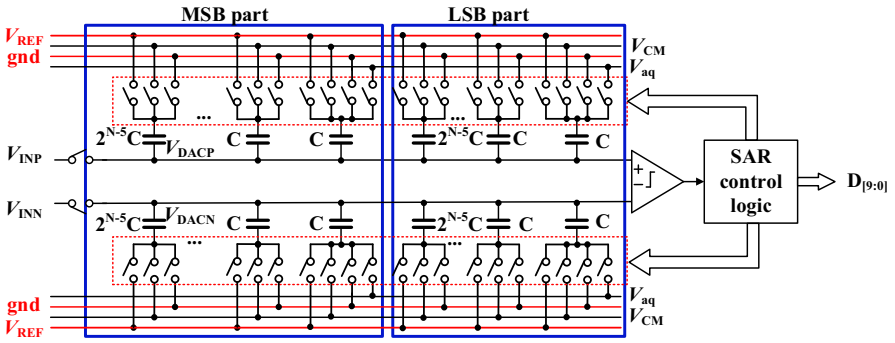


Fig. 1 Proposed V_{aq}-assisted capacitor-splitting structure

parts. The MSB part is equivalent to the LSB part, which is binary-weighted. The input and DAC output signals on the positive and negative sides are denoted by V_{INP}, V_{INN}, V_{DACP}, and V_{DACN}. $D_{[9:0]}$ are digital output. There are four reference voltages V_{REF}, V_{CM}, V_{aq}, and gnd, with gnd serving as the ground. The fact that V_{aq} is only used for four dummy capacitors results in a significant reduction in switching energy and capacitor area.

2.1 Operation Principle

To explain the proposed switching technique in detail, the 5-bit example is presented in Fig. 2. During the sampling phase, the input signal is sampled on the top plates of the capacitors, and the bottom plates of the MSB part and the LSB part on both sides are reset to ground and V_{REF}, respectively. Then, the sampling switches are off. The MSB (D_4) is obtained without any switching power ($E_1 = 0$) due to the top-plate sampling. All capacitor bottom-plates which are connected to V_{REF} on the high voltage side is switched to V_{CM}; meanwhile, all capacitor bottom-plates which are connected to the ground on the low voltage side are switched to V_{CM}. The comparator input variation is got by Eq. (1)

$$\Delta V_{DAC} = \Delta V_{DACP} - \Delta V_{DACN} = -\frac{1}{2}V_{REF} \tag{1}$$

The voltage on the low voltage side rises while the high voltage side falls by the same amount, $V_{REF}/4$. This results in a variation of $-V_{REF}/2$. By the second comparison, D_3 is obtained. During this bit-cycle, the consumed switching energy is calculated by

$$E_{2,D_4=1} = -\frac{1}{2}CV_{REF}^2 \tag{2}$$

Because the switching energy is negative, capacitors will discharge and return energy to the power supply [15, 18, 23]. As shown in Table 1, beginning with the third bit-cycle and excluding the last two, only two capacitors that are related but located in

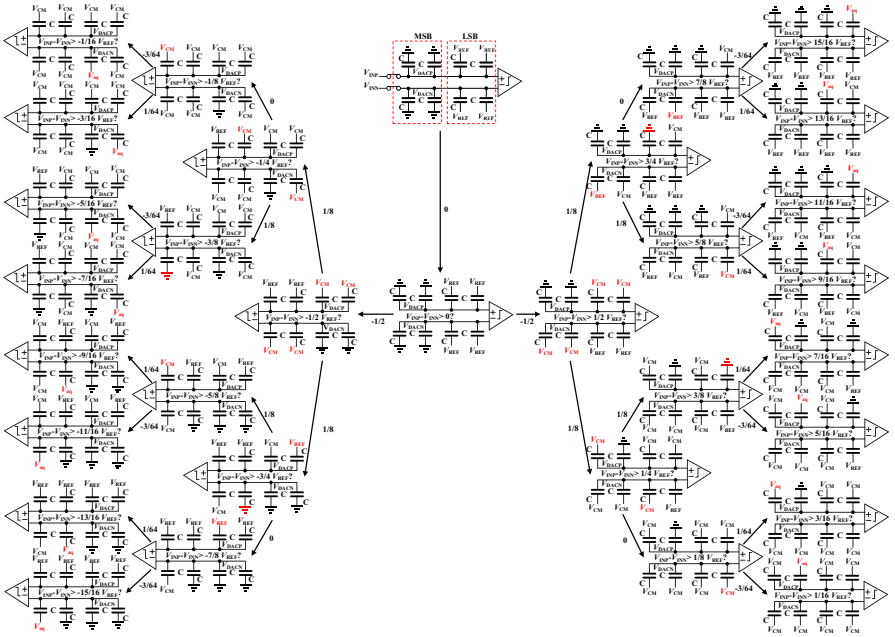


Fig. 2 Proposed switching scheme of 5-bit DAC

Table 1 The related capacitor switching during the third bit-cycle for 5-bit SAR ADC

D_4D_3	Switched capacitors
11	C in LSB part on the V_{DACP} side from V_{CM} to ground;
	C in MSB part on the V_{DACN} side from V_{CM} to V_{REF}
10	C in MSB part on the V_{DACP} side from ground to V_{CM};
	C in LSB part on the V_{DACN} side from V_{REF} to V_{CM}
01	C in LSB part on the V_{DACP} side from V_{REF} to V_{CM};
	C in MSB part on the V_{DACN} side ground to V_{CM}
00	C in MSB part on the V_{DACP} side from V_{CM} to V_{REF};
	C in LSB part on the V_{DACN} side from V_{CM} to ground

different parts on both sides are switched. If $D_4 == $ '1', the corresponding capacitor switching occurs between V_{CM} and ground in different parts on the V_{DACP} side, while the switching on the V_{DACN} side occurs between V_{CM} and V_{REF}. If $D_4 == $ '0', the switching takes place between V_{CM} and ground on the V_{DACN} side, while it does between V_{CM} and V_{REF} on the V_{DACP} side. In this bit-cycle, the switching energy is consumed by

$$E_{3,D_3=1} = \frac{1}{8} C V_{REF}^2 \tag{3}$$

Table 2 The dummy capacitor switching during the last but one bit-cycle for 5-bit SAR ADC

D_4D_2	The dummy capacitor switching	
11	V_{DACN} side	from V_{CM} to V_{REF} in MSB part
10		from V_{REF} to V_{CM} in LSB part
01	V_{DACP} side	from V_{REF} to V_{CM} in LSB part
00		from V_{CM} to V_{REF} in MSB part

Table 3 The dummy capacitor switching during the last bit-cycle for 5-bit SAR ADC

D_4D_1	The dummy capacitor switching	
11	V_{DACP} side	from V_{CM} to V_{aq} in LSB part
10		from ground to V_{aq} in MSB part
01	V_{DACN} side	from ground to V_{aq} in MSB part
00		from V_{CM} to V_{aq} in LSB part

$$E_{3,D_3=0} = \frac{1}{8} C V_{REF}^2 \tag{4}$$

During the last but one bit-cycle, a one-side double-level switching method is implemented. Only one dummy capacitor in MSB or LSB part on one side is switched between V_{REF} and V_{CM}. If $D_4 == '1'$, the switching occurs on the V_{DACN} side; otherwise, the switching takes place on the V_{DACP} side. The switching in detail is described in Table 2. If D_4 and D_2 are the same, the dummy capacitor in the MSB part is switched from V_{CM} to V_{REF}; If not, the dummy capacitor in the LSB part is switched from V_{REF} to V_{CM}.

During the last bit-cycle, only one dummy capacitor performs switching on the other side which differs from that of the former bit-cycle. If $D_4 == '1'$, the switching occurs on the V_{DACP} side, while the switching happens on the V_{DACN} side if $D_4 == '0'$. The switching in detail is described in Table 3. If D_4 and D_1 are the same, the dummy capacitor in the LSB part is switched from V_{CM} to ground; If not, the dummy capacitor in the MSB part is switched from ground to V_{CM}.

2.2 Output Voltage

The output waveform of the proposed switching scheme can be seen in Fig. 3. During the first four bit-cycles, the common-mode voltage is fixed at $V_{REF}/2$; but during the subsequent bit-cycles, it varies, and the maximum varied value is $V_{REF}/32$. The common-mode variation is so tiny that the induced non-linearity is negligible [3, 28].

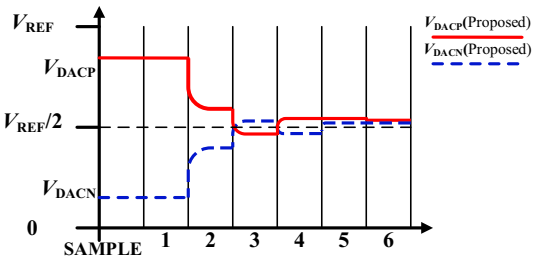


Fig. 3 Output waveform of proposed switching scheme for 6-bit SAR ADC

2.3 Switching Energy

The proposed switching scheme focuses on a significant reduction of the switching energy. The behavioral simulations are performed in MATLAB. For a 10-bit SAR ADC, the average switching energy is only -5.40 $CV_{REF}{}^2$. It requires 10.61 $CV_{REF}{}^2$ if the minus energy dissipated during the second and last but one bit-cycles is not taken into consideration.

The reset energy is dissipated when the final conversion state switches to the following initial state. So, the reset energy is considered when calculating the total switching energy. The behavioral simulation of the reset energy is performed in MATLAB. The reset energy of the proposed switching scheme is 63.88 $CV^2{}_{REF}$. The total switching energy of different switching techniques is plotted against the output code in Fig. 4. If the reset energy is not calculated, the proposed one requires -5.4 $CV_{REF}{}^2$ average

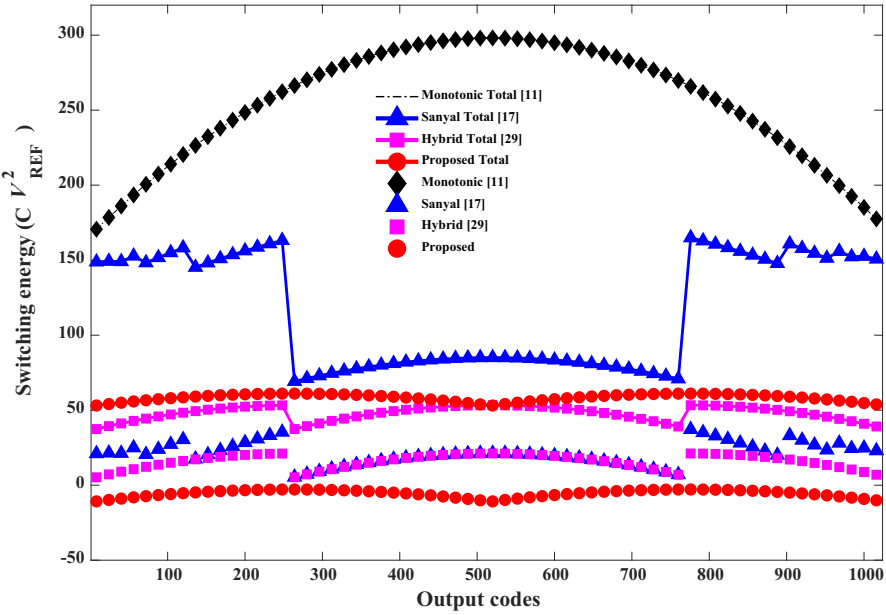


Fig. 4 Switching energy against output code

switching energy, 102.11% less than the monotonic one, which is the most energy-efficient; otherwise, the total switching energy is 58.48 $CV_{REF}{}^2$, 72.88% less.

3 Non-Ideal Effects

3.1 Capacitor Mismatch

The value of the unit capacitor C is usually determined by capacitor mismatch. C obeys Gaussian distribution with a nominal value of C_u and a standard deviation of σ_u. Thus, each capacitor in Fig. 1 can be expressed by the sum of the nominal value and the error term. C_{PM}, C_{PL}, C_{NM}, and C_{NL} are all equally binary-weighted, and for simplicity, only C_{PM} is described.

$$C_{PM,i} = \begin{cases} 2^{i-1}C_u + \delta_{PM,i} & 1 \le i \le N-4 \\ C_u + \delta_{PM,0} & i = 0 \end{cases} \tag{5}$$

where all error terms obey independent, identically distributed (i.i.d.) Gaussian distribution. The total capacitance can be achieved

$$C_{total} = C_{P,total} = 2^{N-3}C_u + \left(\sum_{i=0}^{N-4}\delta_{PM,i} + \sum_{i=0}^{N-4}\delta_{PL,i}\right) \approx 2^{N-3}C_u \tag{6}$$

So, their mean values and variances are

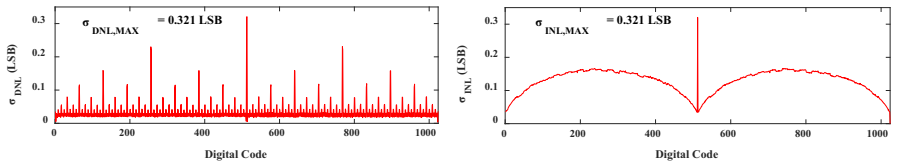
$$\begin{aligned} E\left(\delta_{PM,i}\right) &= 0 \\ E\left(\delta_{PM,i}^2\right) &= 2^{i-1}\sigma_u^2 \end{aligned} \tag{7}$$

Due to differential and capacitor-spitting structure, the worst integral nonlinearity (INL) appears at 1/2 ('0,111,111,111') of full-scale range V_{FS} for a 10-bit SAR ADC with the proposed switching method. The DAC analog output for $1/2V_{FS}$ is

$$\begin{aligned} &V_{DAC}(y = 0111111111) = V_{DACP}(y) - V_{DACN}(y) \\ &= (V_{INP} - V_{INN}) + V_{CM}\frac{\sum_{i=0}^{N-4}C_{PM,i} - \sum_{i=0}^{N-4}C_{PL,i} + \sum_{i=0}^{N-4}C_{NL,i} - \sum_{i=1}^{N-4}C_{NM,i} - \frac{C_{NM,0}}{2}}{C_{total}} \end{aligned} \tag{8}$$

Then, the error term is yielded by subtracting the nominal value

$$\begin{aligned} &\mathrm{INL}(y) = V_{DAC,err}(y) \\ &= \frac{\sum_{i=0}^{N-4}\delta_{PM,i} - \sum_{i=0}^{N-4}\delta_{PL,i} + \sum_{i=0}^{N-4}\delta_{NL,i} - \sum_{i=1}^{N-4}\delta_{NM,i} - \frac{\delta_{NM,0}}{2}}{2C_{total}}\frac{V_{REF}}{\mathrm{LSB}} \end{aligned} \tag{9}$$



(a) **(b)**

Fig. 5 The standard deviation of **a** DNL and **b** INL at each output code

where $\text{LSB} = \frac{2V_{\text{REF}}}{2^N}$. And its variance is

$$E\left[V_{\text{DAC,err}}(y)^2\right] = \left(2^N - 3\right)\frac{\sigma_{\text{u}}^2}{C_{\text{u}}^2} \tag{10}$$

Thus, the maximum INL variation is obtained

$$\sigma_{\text{INL,MAX}} = \sqrt{2^N - 3}\frac{\sigma_{\text{u}}}{C_{\text{u}}} \tag{11}$$

The differential nonlinearity (DNL) is the difference between the voltage errors at two consecutive DAC outputs

$$\text{DNL}(y) \approx \Delta V_{\text{DAC,err}}(y) = V_{\text{DAC,err}}(y) - V_{\text{DAC,err}}(y-1) \tag{12}$$

The worst DNL is also expected to occur at $1/2V_{\text{FS}}$ (from '1,000,000,000' to '0,111,111,111'). Its variance is

$$E\left[\Delta V_{\text{DAC,err}}(y)^2\right] = \left(2^N - 3\right)\frac{\sigma_{\text{u}}^2}{C_{\text{u}}^2} \tag{13}$$

As a result, the maximum DNL variation is

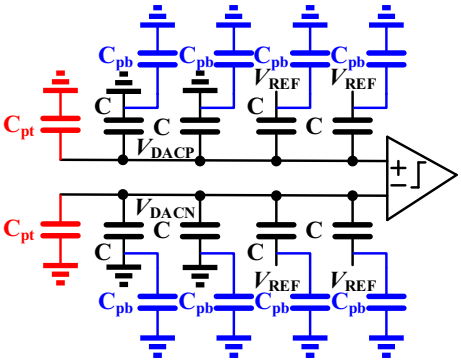
$$\sigma_{\text{DNL,MAX}} = \sqrt{2^N - 3}\frac{\sigma_{\text{u}}}{C_{\text{u}}} \tag{14}$$

Figure 5 depicts behavioral simulation results of 500 Monte Carlo runs of the proposed switching scheme for a 10-bit SAR ADC with $\sigma_{\text{u}}/C_{\text{u}} = 0.01$. The maximum DNL and INL root-mean-square (RMS) values are both 0.321 LSB, which occur at $1/2V_{\text{FS}}$. Thus, the proposed capacitor-splitting switching scheme shows good linearity performance.

3.2 Parasitic Capacitance

As seen in Fig. 6, the parasitic capacitance exists between capacitor top- or bottom-plates and substrate [5–7]. To calculate the energy required for switching, parasitic capacitors must be considered. To be fair with [7, 9, 23], the top-plate capacitance

Fig. 6 Parasitic capacitors



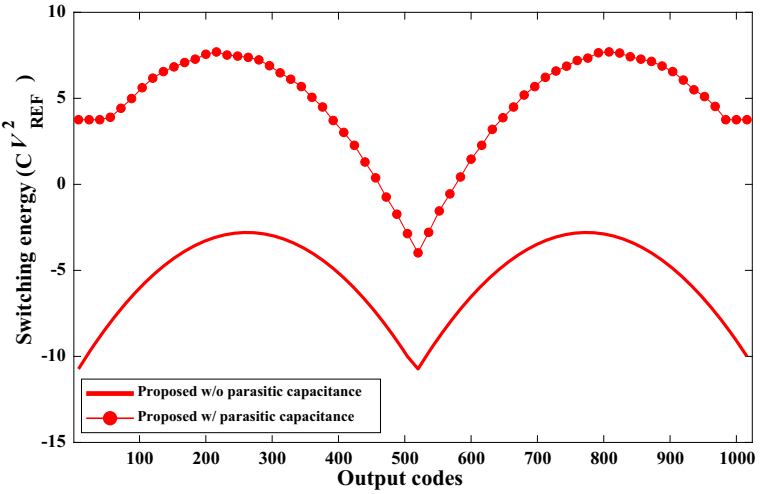


Fig. 7 The switching energy with parasitic capacitors

C_{pt} and the bottom-plate capacitance C_{pb} are assumed to be 10% C_{total} and 15% C, respectively. The switching energy is shown in Fig. 7. When parasitic capacitance is considered, the proposed switching method has switching energy of 4.56 $CV_{\text{REF}}{}^2$, which is much higher than that without parasitic capacitance.

3.3 Reference Voltage Mismatch

The ADC accuracy can suffer when there is a mismatch between V_{REF} and $V_{\text{CM}}/V_{\text{aq}}$ [9, 14, 16]. If V_{CM} varies by ΔV, then one side adds 2^{-i} $[V_{\text{REF}} - (V_{\text{CM}} + \Delta V)]$ while the other side subtracts 2^{-i} $(V_{\text{CM}} + \Delta V)$. Thus, owing to the differential structure, inaccuracy of V_{CM} does not affect the SAR ADC accuracy except for the last two bit-cycles. To evaluate the reference voltage mismatch effect, MATLAB behavioral simulation is performed. Under the case of mismatch between $V_{\text{CM}}/V_{\text{aq}}$ and V_{REF}

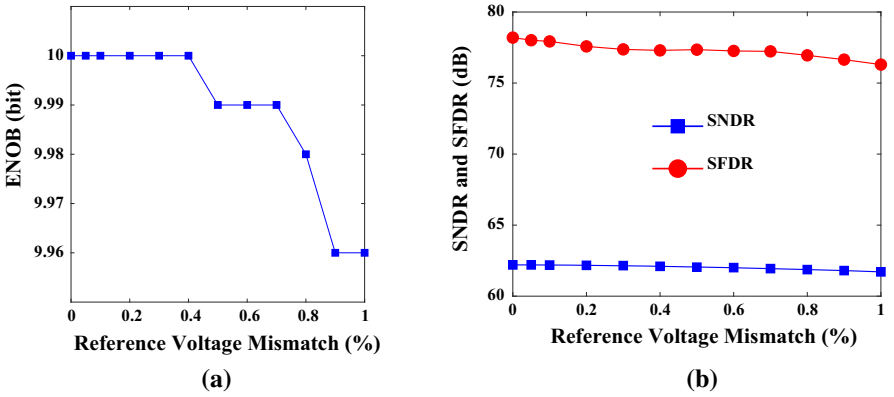


Fig. 8 **a** ENOB, **b** SNDR, and SFDR VS reference voltage mismatch

ranging from 0 to 1%, 500 run simulation results are shown in Fig. 8. All effective number of bits (ENOB), signal-to-noise-and-distortion ratio (SNDR), and spurious-free-dynamic-range (SFDR) have a very small shift. Because the mismatch between the reference voltages is often less than 0.3% [16], its effect on the accuracy of the SAR ADC can be negligible.

4 DAC Control Logic

DAC control logic of the proposed switching scheme for a 10-bit SAR ADC is shown in Fig. 9, which is implemented by gate logic design. D_i and $\overline{Di}$ are the comparison results, where $1 \leq i \leq 9$. $C_{PM,8\text{-}i}$, $C_{PL,8\text{-}i}$, $C_{NM,8\text{-}i}$, and $C_{NL,8\text{-}i}$ are all equally binary-weighted.

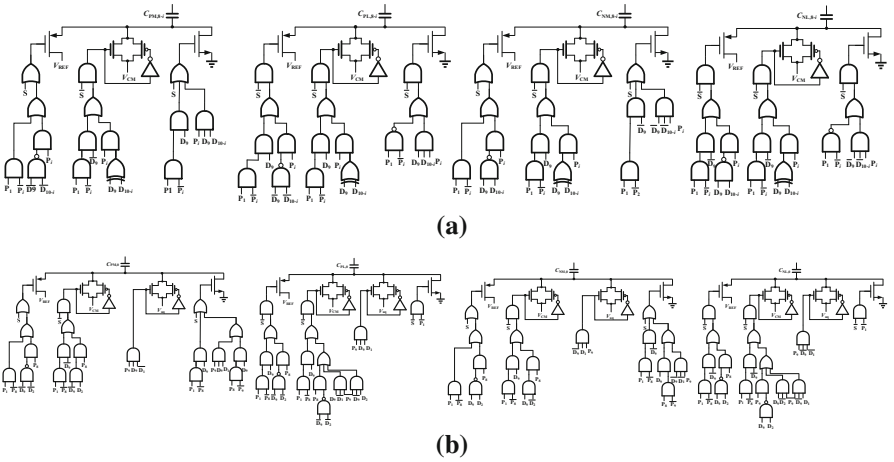


Fig. 9 DAC control logic: **a** all capacitor switching except the dummy one **b** the dummy capacitor switching

Except for the last two bit-cycles, $C_{PM,8\text{-}i}/C_{NL,8\text{-}i}$ or $C_{PL,8\text{-}i}/C_{NM,8\text{-}i}$ is switched in pair depending on the first and former comparison result, shown in Fig. 9(a). To describe in brief, only $C_{PM,8\text{-}i}$ is analyzed. When $i = 2$, $D_{10\text{-}i} = D_8$ is obtained, then the second switching is working. $C_{PM,8\text{–}2}$ ($2^{8-2-1}C = 32C$) pair or the other one is switched. For $i = 8$ and 9, $C_{PM,8\text{–}8} = C_{PM,8\text{–}9} = C$, where the dummy capacitor C is working, seen in Fig. 9(b). S *and* $\overline{S}$ are the sampling signals. During the sampling period, $S = 1$; otherwise, $S = 0$. P *and* $\overline{P_i}$ are the sequence control signals. From i-th to the last switching, P_i is always 1; otherwise, P_i is 0. V_{aq} is added to four dummy capacitors, whose control logics are easier to implement than those of V_{REF}, V_{CM}, and ground, shown in Fig. 9(b). Thus, the control logic is not complicated. A simple and direct technique for quantitatively evaluating the complexity of the DAC control logic is to count the average switched capacitors that are controlled by the DAC control logic during each bit-cycle. A piecewise function is used to express the logic complexity LC

$$LC = \begin{cases} 0 & m \le 2 \\ 1 & 2 < m \le 4 \\ 2 & m > 4 \end{cases} \tag{15}$$

where m is No. of the average switched capacitors. If m is not greater than 2, LC is 0, which means low; If m is greater than 2 but less than or equal to 4, LC is 1, which is medium; If m is greater than 4, LC is 2, which means high. The logic complexity of the proposed switching scheme and others is shown in Table 4.

The control logic of V_{aq} is related to P_9, D_9, and the former bit D_1. When the switching enters the P_9 phase, only one of the four dummy capacitors is switched. To express the process in detail, a truth table is shown in Table 5. If the true value is '1', V_{aq} switching occurs on this part while other parts remain unchanged.

5 Post-Layout Simulation Results

By using the proposed switching scheme, a 10-bit SAR ADC is designed in 0.18-μm 1P6M CMOS process with a sampling frequency of 20 KS/s and a supply voltage of 0.6-V. The SAR ADC layout occupies an area of about 340 × 380 μm^2, as shown in Fig. 10. To avoid linearity degradation, a partial common-centroid layout strategy is performed. The MIM capacitor is chosen, and the capacitor floor plan is shown in Table 6.

The DNL and INL of the proposed ADC are shown in Fig. 11. The peak DNL is − 0.49/0.52 LSB, and the peak INL is -0.41/0.48 LSB, respectively.

Figure 12 illustrates the dynamic performance. SNDR and SFDR are 59.41 and 70.56 dB, respectively. Thus, ENOB is 9.57 bits. And the total power consumption of the proposed SAR ADC is 35.1 nW. The Walden figure-of-merit (FOMW) is defined as

$$\text{FOM} = \frac{P}{f_s \times 2^{\text{ENOB}}} \tag{16}$$

Table 4 Comparison of different switching schemes for 10-bit SAR ADC

Switching schemes	Switching energy ($CV_{REF}{}^2$)	Energy savings (%)	Reset energy ($CV_{REF}{}^2$)	Total energy saving (%)	Area saving (%)	Reference voltage	MCMVV (V_{REF})	Sensitivity to the accuracy of V_{CM}/V_{aq}	Logic complexity
Monotonic [11]	255.5	Reference	0	Reference	Reference	V_{REF}, gnd	1/4	NO	Low
Tri-level [31]	42.42	83.40	0	83.40	50	V_{REF}, V_{CM}, gnd	1/4	High	Low
Sanyal & Sun [17]	21.33	91.65	95.75	54.17	50	V_{REF}, V_{CM}, gnd	1/4	High	Low
Hybrid [29]	15.88	93.78	32.125	81.21	50	V_{REF}, V_{CM}, gnd	1/4	High	Low
Wang [26]	10.54	95.87	32	83.35	75	V_{REF}, V_{CM}, gnd	1/4	Low	Low
LSB-split [7]	10.8	95.77	48.12	76.94	75	V_{REF}, V_{CM}, gnd	1/4	High	Medium
Yousef [34]	0	100	62	75.73	74.6	V_{REF}, V_{CM}, gnd	0	NO	High
Zhang [36]	6.75	97.48	0.55	97.14	87.1	V_{REF}, V_{CM}, gnd	0	NO	High
V_{aq}-based [37]	48.03	81.20	0.03	81.19	75	V_{REF}, V_{aq}, gnd	1/8	Low	Low
Proposed	10.61	95.85	63.88	70.85	75	V_{REF}, V_{CM},	1/256	Low	Medium
Proposed with Minus Energy	−5.40	102.11		72.88		V_{aq}, gnd			

MCMVV: Maximum Common-Mode Voltage Variation

Table 5 V_{aq} switching true table during the last bit-cycle

D_9D_1	V_{aq} switching			
	MSB part on V_{INP} side	LSB part on V_{INP} side	MSB part on V_{INN} side	LSB part on V_{INN} side
11	0	1	0	0
10	1	0	0	0
01	0	0	1	0
00	0	0	0	1

Fig. 10 SAR ADC layout

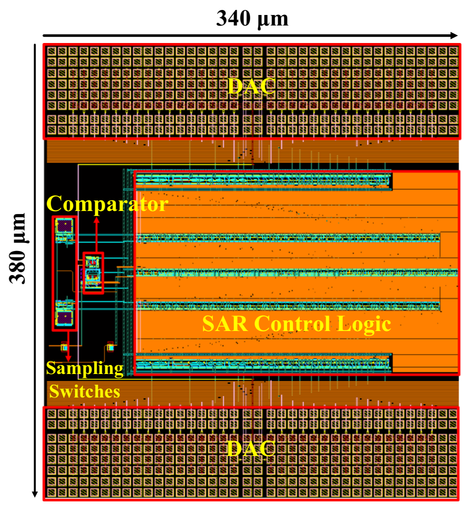


Table 6 The floor plan of DAC

D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
D	D	6	6	5	6	6	5	4	3	4	5	6	6	5	6	6	0	D	D	0	6	6	5	6	6	5	4	3	4	5	6	6	5	6	6	D	D
D	D	6	6	5	6	6	5	4	3	4	5	6	6	5	6	6	1	D	D	1	6	6	5	6	6	5	4	3	4	5	6	6	5	6	6	D	D
D	D	6	6	5	6	6	5	4	3	4	5	6	6	5	6	6	2	D	D	2	6	6	5	6	6	5	4	3	4	5	6	6	5	6	6	D	D
D	D	6	6	5	6	6	5	4	3	4	5	6	6	5	6	6	2	D	D	2	6	6	5	6	6	5	4	3	4	5	6	6	5	6	6	D	D
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

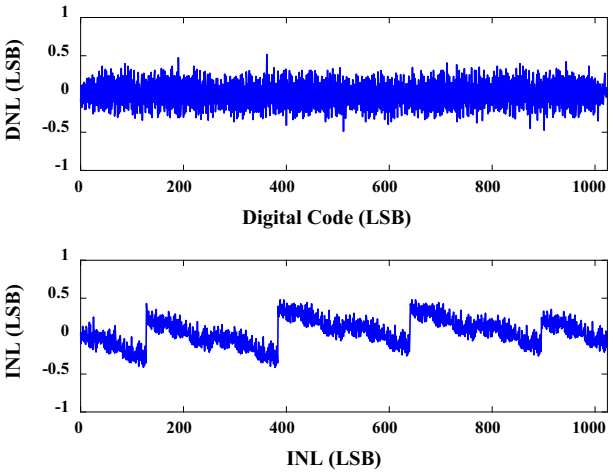


Fig. 11 DNL and INL

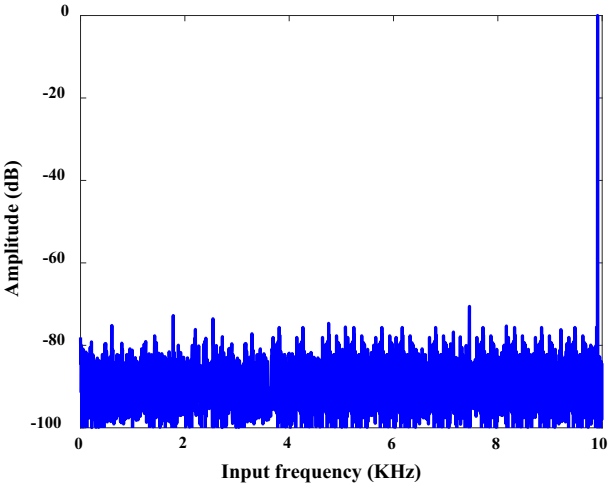


Fig. 12 FFT spectrum

where f_s represents the sampling rate, and P is the power consumption of the SAR ADC. Therefore, the proposed SAR ADC achieves a FOM of 2.31 fJ/conversion step, which achieves good power efficiency. Besides, the SFDR and SNDR of the proposed SAR ADC versus the input frequency are shown in Fig. 13. Both of them are approximately unchanged over the entire bandwidth.

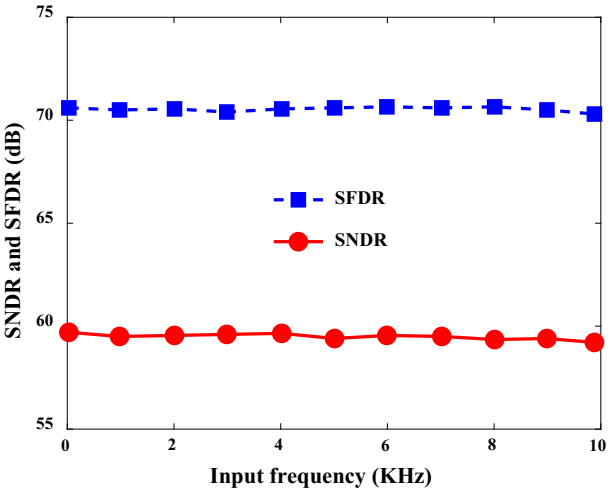


Fig. 13 SFDR and SNDR versus input frequency

6 Conclusion

In this paper, a V_{aq}-assisted four-level capacitor-splitting switching algorithm is proposed. It is a better trade-off among energy efficiency, capacitor area, common-mode voltage variation, logic complexity, and accuracy. The proposed switching procedure achieves lower switching energy and a smaller capacitor area. The DAC output common-mode voltage keeps nearly constant. The capacitor and reference voltage mismatches have a little effect on the SAR ADC accuracy. The DAC control logic complexity is not high. A 0.6-V 10-bit 20 KS/s SAR ADC in 0.18-μm 1P6M CMOS technology is designed, which adopts the proposed switching scheme. It has a FOM of 2.31 fJ/conversion step and occupies an active area of about 0.13 mm^2. Thus, simulation results demonstrate the power efficiency of the proposed switching scheme, which is suitable for low-power, low- or medium-speed SAR ADCs.

Data Availability This manuscript has no associated data.

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