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SHORT PAPER

Design of a Highly Stable and Robust 10T SRAM Cell for Low-Power Portable Applications

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Abstract

This paper investigates a novel highly stable and robust single-ended 10T SRAM cell appropriate for low-power portable applications. The cell core of the proposed design is a combination of a normal inverter with a stacked NMOS transistor and a Schmitt-trigger (ST) inverter with a double-length pull-up transistor. This improves hold stability and leakage power dissipation. The read and write operations of the proposed cell are performed with the aid of separated paths and bitlines, lowering power consumption. The strong cell core and decoupled read path eliminate the read-disturbance issue in the proposed cell, resulting in read static noise margin (RSNM) enhancement. Furthermore, the feedback-cutting write-assist technique used in the proposed design mitigates the writing '1' issue; consequently, write static noise margin (WSNM)/write margin (WM) improves. To prove the superiority of the proposed SRAM cell in various performance metrics, it is compared with state-of-the-art SRAM cells, introduced as 6T, TG9T, 10T-P1, and SB11T, using HSPICE and 16-nm CMOS technology node taking into consideration the impact of the severe process, voltage, and temperature (PVT) variations. Obtained results at $V_{DD} = 0.7$ V show that the proposed design offers the highest HSNM/RSNM/WSNM (or WM). The read/write delay of the proposed cell is 3.92X/2.37X higher than that of the 6T SRAM cell due to its single-ended reading/writing structure. However, in terms of power consumption, the proposed cell exhibits 1.64X/1.54X lower than that of 6T SRAM cell. Though the proposed cell occupies a 1.24X higher area compared with the 6T SRAM cell due to its higher count of transistor, it shows the highest proposed figure of merit among all the studied SRAM cells, which is 26.90X higher than that of 6T SRAM cell.

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1 Introduction

Nowadays, with the rapid prospering of the portable electronics market, low power and high stability have become two main design features of a system-on-chip (SoC) [14, 26]. Lowering the power consumption in static random access memories (SRAMs) is an important task, which can reduce the total power of the SoC. This is because SRAMs are the main contributor to the SoC's area and consequently its power [26]. There are many approaches to achieve low power and/or high stability in the SRAM cells such as minimizing the supply voltage (V_{DD}) to reduce total power, utilizing multi-threshold complementary metal–oxide–semiconductor (CMOS) process to decrease leakage power, and using multiple SRAM sub-macros rather than one single SRAM macro to increase stability and to minimize dynamic power [14]. Among them, V_{DD} scaling is the well-known and efficient approach to access the low-power operation in the SRAM cell due to the existence of a linear and a quadratic relation between pairs of V_{DD} and leakage current and V_{DD} and dynamic power, respectively [3]. Nevertheless, V_{DD} reduction poses many problems as follows. The delay increases with V_{DD} reduction, and therefore, energy consumption increases [24]. The voltage difference between V_{DD} and threshold voltage (V_{th}) reduces with downscaling V_{DD}, which leads to the grave degradation of static noise margin (SNM) and makes the circuit unreliable [23]. In the severe low-V_{DD} operation, the sensitivity of the SRAM cell's parameters to process variations such as line edge roughness (LER) and random dopant fluctuation (RDF) increases, which may lead to V_{th} mismatch between adjacent transistors in the cell [20]. Furthermore, increased manufacturing process, voltage, and temperature (PVT) variations at severe low-V_{DD} further degrade the SRAM cell's stability [25]. The conventional 6T SRAM cell suffers from poor SNM induced by read current disturbance and therefore cannot operate at severe low-V_{DD} [13]. Furthermore, it offers undesirable read SNM (RSNM) and write SNM (WSNM), as a measure of read stability and writability, respectively, at low-V_{DD}, which increase the probability of operational failure [27]. These issues are further worsened by contradicting requirements for RSNM and WSNM [13, 24].

Therefore, it is necessary to design a highly stable and robust SRAM cell that can overcome the aforementioned challenges and work well at low-V_{DD} to gain the advantages of the V_{DD} scaling. Various configurations of SRAM cells have been proposed in the literature over the years to achieve better performance than conventional design. SRAM cells proposed in [17, 22, 27] utilize the read decoupling technique to isolate the data storing nodes from the reading access path during the read operation to overcome conflicting read/write requirements induced by the conventional 6T SRAM cell. This technique improves the cell's RSNM to be as high as hold SNM (HSNM). The conventional 8T SRAM cell presented in [15] improves the RSNM by application of two extra read-access transistors, one read bitline, and one read wordline to form the isolated read path. This improvement is achieved at the cost of leakage in the read path, which is further pronounced with technology scaling. To reduce this

leakage and also to increase the RSNM, a modified version of the isolated read path has been individually used in the design of SRAM cell proposed in [17]. This reduction is attributed to data-independent read port leakage. Due to offering better voltage transfer characteristics (VTCs) as a direct consequence of the feedback mechanism, the normal inverter has been replaced by the Schmitt-trigger (ST)-based inverter to form the cell core of the SRAM cells designed in [20, 21] to improve both RSNM and WSNM simultaneously. Moreover, these designs are tolerant to PVT variations and modulate the V_{th} of the latch transistors to compensate for the variations. However, the read-disturbance problem is still sensed in these SRAM cells.

Various SRAM cells have been presented in the literature [2, 6, 22, 27] to achieve the low-power operation. This is due to the application of single bitline to reduce the switching activity factor of the bitline ($\alpha_{bitline}$) to less than half during the read/write operation. Other SRAM cells proposed in [7, 9] employ separate bitlines to perform read and write operations. In these designs, α_{bitline} also reduces to less than 0.5; consequently, power consumption reduces. However, single-ended SRAM cells suffer highly from writing '1' ability degradation without any write-assist techniques, leading to a writing '1' failure [27]. To solve this problem, a feedback-cutting NMOS transistor or transmission gate is inserted inside the cell core of the SRAM cells proposed in [2, 10, 27] to remove the feedback path of the cross-coupled inverters pair during the write operation, resulting in WSNM improvement. The single-bitline 11T SRAM cell projected in [22] employs power-gated transistors to cut the power rails off from the data storing node Q or QB during the write operation to improve the WSNM. Furthermore, the connection of several access transistors to the same bitline increases overall bitline capacitance, and therefore, the 11T cell [22] shows longer read delay and higher dynamic power. To mitigate the read disturbance, a one-sided ST-based 9T SRAM cell was proposed in [16]. In this cell, the power rails are cut from the internal storage node Q during the write operation to increase the WSNM. Another technique to eliminate the writing '1' issue in the single-ended SRAM cells is to use data-aware power cutoff (DAPC) write-assist mechanism. The 11T [3] SRAM cell uses this technique to improve the WSNM but suffers from high dynamic power due to increased bitline capacitance.

Therefore, this paper proposes a highly stable and robust 10T SRAM cell appropriate for low-power portable applications such as mobile phones and medical instruments like pacemaker to solve the above-mentioned challenges. The proposed 10T SRAM cell will be called New10T, hereafter. The main characteristics of the proposed SRAM cell are as follows:

1. A normal inverter is combined with ST inverter to form the cell core of the proposed cell, resulting in HSNM enhancement.
2. Furthermore, the application of the read decoupling technique improves the RSNM.
3. The writing '1' issue is eliminated by the New10T SRAM cell through inserting a feedback-cutting NMOS transistor inside the cell core, therefore resulting in WSNM enhancement.
4. The dynamic power consumption is reduced by the proposed design due to the use of single-ended structure.

5. The presence of stacked transistors in the cell core along with a double-length pull-up transistor in the ST inverter minimizes the leakage power dissipated by the proposed cell.

The rest of this paper is organized as follows. Section 2 introduces the New10T SRAM cell. The simulation results and discussion are presented in Sect. 3. Finally, Sect. 4 concludes this paper.

2 The New10T Sram Cell

The schematic of the New10T SRAM cell is shown in Fig. 1. The normal inverter with a stacked NMOS transistor (MNL1, MNL2, and MPL), gated by *PQ* node, and the ST-based inverter (MNR1, MNR2, MNR3, and MPR), gated by *QB* node, make the cell core of the proposed design to maintain the cell content. The write-access transistor WAT, driven by the write wordline (*WWL*), establishes a write path to write a desired data into the cell by the column-based write bitline (*WBL*). Due to single-ended writing structure, a feedback-cutting transistor FCT, controlled by the columnar selection line (*CSL*) control signal, is inserted inside the cell core of the proposed design. This transistor is at OFF state during the write operation to eliminate the feedback path of the cell core to ensure that a successful write '1' operation is performed. Furthermore, in the ST-based inverter, the source of the feedback transistor MNR3 is connected to the *CSL*. As the *CSL* is grounded during the write operation, the feedback action from the feedback transistor MNR3 in the ST-based inverter is removed, which in turn helps to increase the writing speed. The columnar read bitline (*RBL*) is accessed to the cell by the read-access transistor (RAT), gated by the read wordline (*RWL*), to perform a read operation. The read path does not include the true internal data storing nodes *Q* and *QB*. Moreover, during the read operation, an increase in voltage of the *PQB* and *QB* nodes has no harmful effects on the *Q* node because the voltage trip level of the

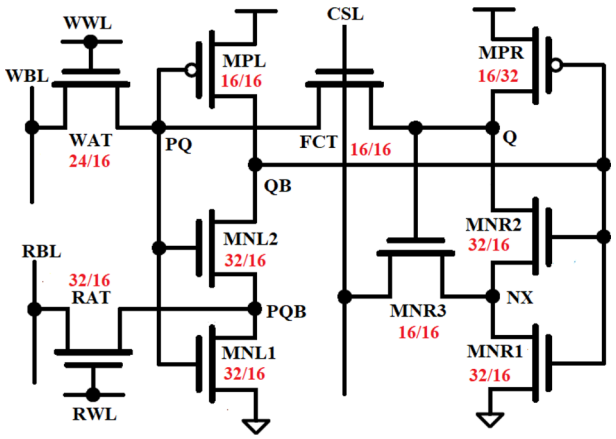

Fig. 1 The schematic of the New10T SRAM cell annotated with channel width-to-channel length ratio (*W*/*L*) in nm

Table 1 Control signals for the New10T SRAM cell

	Operations			
Signals	Hold	Read	Write '0'	Write '1'
WBL	1	1	0	1
RBL	1	1	1	1
WWL	0	0	1	1
RWL	0	1	0	0
CSL	1	1	0	0

ST inverter is higher than the normal inverter, and thus, the *QB* node never reaches it. Therefore, the read-disturbance issue is removed by the proposed design. Table 1 gives the status of the control signals used in the proposed design for the hold, read, and write operations.

3 Cell Performance and Comparison

In this section, various performance parameters of the New10T SRAM cell are extracted using HSPICE and 16-nm CMOS technology node [28]. To estimate the relative strength of the proposed cell, it is compared with existing SRAM cells such as conventional 6T [19], transmission-gate 9T (TG9T) [27], differential writing 10T (10T-P1) [17], and single-bitline 11T (SB11T) [22], as shown in Fig. 2, in terms of major design metrics. The size of each transistor is annotated in Fig. 2.

In advanced technology, the impact of PVT variations becomes a series issue. Therefore, we analyzed their impact on the SRAM cells' performance using Monte Carlo (MC) simulations with 10,000 samples. For this reason, we take into consideration the changes in the various process and device parameters including channel length (L), channel width (W), channel doping concentration (NDEP), oxide thickness (T_{ox}), threshold voltage (V_{th}), mobility (μ_0), and supply voltage (V_{DD}). All the above-mentioned parameters are assumed to have an independent normal Gaussian distribution with a 3σ variation of 10% [2].

A comparison of different performance metrics for under-test SRAM cells is presented in the following subsections.

3.1 Read-Access Time

As shown in Fig. 3a, b, to read the stored data in the cell, the *RBL* is precharged to V_{DD}. The *WBL* and *WWL* are kept at V_{DD} and GND, respectively. Therefore, the write-access transistor WAT is turned off as the *WWL* is grounded, to remove the write path. The *CSL* is set to V_{DD} to establish the feedback path of the cell core and to activate the feedback mechanism of the ST-based inverter offered by the MNR3 transistor. The *RWL* is raised high to turn on the read-access transistor (RAT). Depending upon

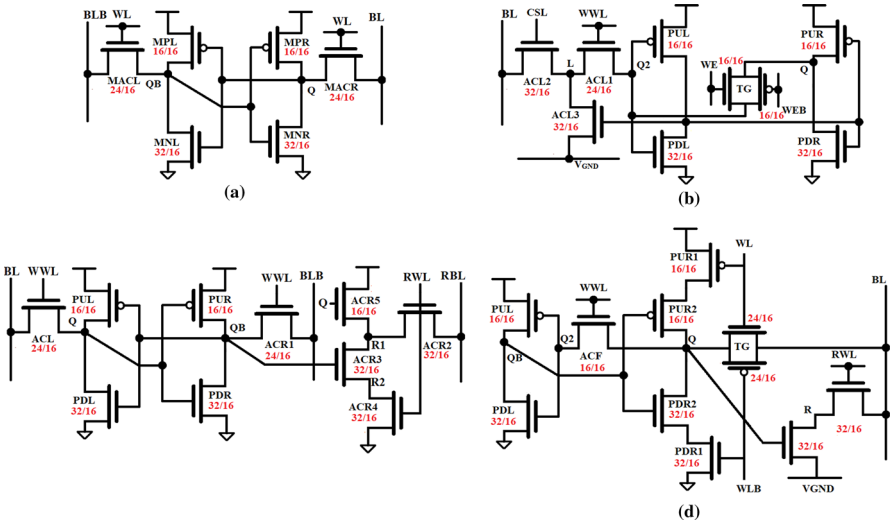

Fig. 2 The schematic of the considered SRAM cells with *W*/*L* ratio in nm. **a** 6T [19], **b** TG9T [27], **c** 10T-P1 [17] and **d** SB11T [22]

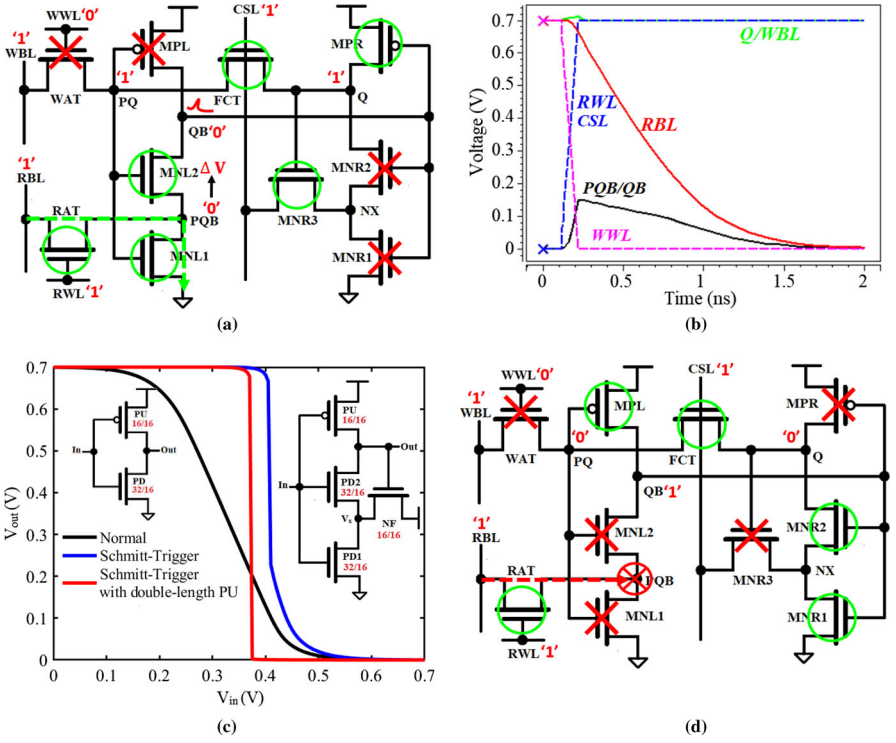

Fig. 3 **a** read '0' operation **b** transient response during read '0' operation **c** VTC of the normal- and ST-based inverters and **d** read '1' operation of the New10T SRAM cell

the content of the data storing node Q or QB, the *RBL* either discharges to GND through the pass transistors comprising RAT and MNL1 or remains at its initial high precharged value (V_{DD}).

To show the read '0' operation of the New10T SRAM cell (Fig. 3a), let us consider the case in which the storage node Q/QB is storing '1'/'0' logic value. The transistors MNL1 and MNL2 of the normal inverter are turned on as storage node Q stores '1'. Then, a discharging path formed by RAT and MNL1 is created for the *RBL*. As the *RBL* is discharging to the ground through this path, the voltage level of the *PQB* node is raised from zero to the positive value, which is almost equal to 0.15 V based on the transient response of the proposed design during the read '0' operation when subjected to PVT variations (worst-case sample), as shown in Fig. 3b. An increase in the *PQB* node voltage leads to an increase in the *QB* node voltage, as MNL2 is at *ON* state. However, the MNL2 is an n-type MOSFET and cannot pass the strong '1' logic value. On the other hand, the voltage level of the *QB* node never reaches the trip voltage level of the ST-based inverter (see Fig. 3c, blue curve) to flip the Q node state. Therefore, the *RBL* discharges to the ground without flipping the content of the cell, resulting in the read-disturbance removal. This issue increases the cell's RSNM to be equal to HSNM. However, as shown in Fig. 3c, when the output voltage of ST inverter is high ($V_{out} = V_{DD}$), NF is turned on, and therefore, charges V_x node. This issue makes it hard to change the high value of V_{out}. Therefore, we have doubled the channel length of the PUR (*i.e.,* $L_{PUR} = 2 \times L_{min} = 32$ nm) in the ST inverter to equalize '0' and '1' margins. Its voltage transfer characteristics (VTC) are shown in Fig. 3c as the red curve.

Now, assume that the data storing node Q/QB is initially storing '0'/'1' logic value. The pull-down network of the normal inverter is at OFF state because data stored at Q node is '0'. Therefore, the *RBL* remains at its initial high precharged value (V_{DD}), which shows that the Q node is storing '0' (Fig. 3d).

The read delay (T_{RA}) is a measure of the speed of the SRAM cell during the read operation. The definition of the T_{RA} for single-ended and differential SRAM cells is different. For differential reading structure, the T_{RA} is calculated as the time when the voltage difference of two bitlines becomes 50 mV right after wordline activation [11, 12]. For single-ended reading structure, on the other hand, the T_{RA} is defined as the time when read bitline is discharged from V_{DD} to its half immediately after assertion of wordline [18]. Figure 4 shows the comparison of the T_{RA} of the investigated SRAM cells at different V_{DD} values. SRAM cells including TG9T, 10T-P1, SB11T, and New10T utilize single-ended reading structure, and therefore, their T_{RA} is higher than that of 6T SRAM cell, which is using differential reading structure. Due to the connection of several transistors to the same bitline, which increases overall bitline capacitance, the SB11T SRAM cell shows the highest T_{RA} among all the SRAM cells. The read path of 10T-P1 SRAM cell constitutes three NMOS access transistors, resulting in T_{RA} increase. Due to the same read path, formed by two NMOS access transistors, SRAM cells such as TG9T and New10T show equal T_{RA} and lower than those of aforementioned SRAM cells. The New10T SRAM cell exhibits 2.76X/1.54X lower and 3.92X higher T_{RA} compared with SB11T/10T-P1 and 6T SRAM cells, respectively, at $V_{DD} = 0.7$ V.

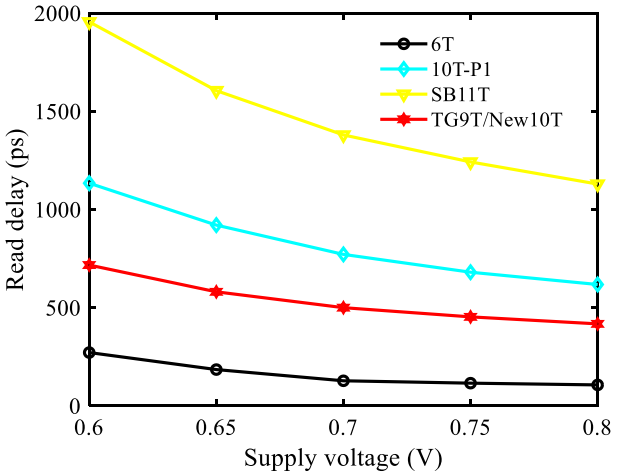

Fig. 4 T_{RA} of the tested SRAM cells versus V_{DD}

3.2 Write-Access Time

The write operation in the New10T SRAM cell performs as follows. As shown in Fig. 5a, b, the *CSL* is set to GND to turn off the FCT. This in turn removes the feedback path of the cross-coupled normal- and ST-based inverters pair to eliminate writing '1' issue in the proposed single-ended design and to facilitate the write '1' operation. Furthermore, by pulling down the *CSL*, there will be no feedback action offered by MNR3 in the ST-based inverter, helping to increase writing speed. The *RBL* is kept at V_{DD} and *RWL* is forced to GND to turn off the RAT to remove the read path. The *WWL* is raised high to turn on the WAT to create the writing path. Depending upon whether '1'/'0' or '0'/'1' is to be written to *Q*/*QB*, the *WBL* is either maintained at V_{DD} or GND.

Let us consider the case in which the '1'/'0' logic value is to be written into the '0'/'1' storing node *Q*/*QB*. Thus, a '1' is applied to the *WBL*. The '1' logic value is transferred to *PQ* node through the WAT. By raising the voltage level of the *PQ* node, the MNL1 and MNL2 are turned on, which invert the content of the *QB* node from '1' to '0' logic value. By pulling down the *QB* node, the MPR is turned on, which charges the *Q* node. Finally, a write '1' operation is successfully performed, as shown in Fig. 5a. To write '0' into the '1' storing node *Q* as shown in Fig. 5b, a complementary process takes place where *WBL* is set to GND.

The write delay (T_{WA}) estimates the swiftness of the SRAM cell to flip the data stored in its internal storing nodes during the write operation. Since the proposed design is a single-ended cell and writing '1' process is difficult than writing '0' one, we compared T_{WA} for writing '1' into the '0' storing node *Q* of all the compared SRAM cells at different V_{DD} values, as shown in Fig. 6. The T_{WA} for writing '1' is measured as the time required by *Q* node, which initially stores '0,' to reach 90% of V_{DD} right after asserting wordline [3, 18]. Due to the use of the single-ended writing structure,

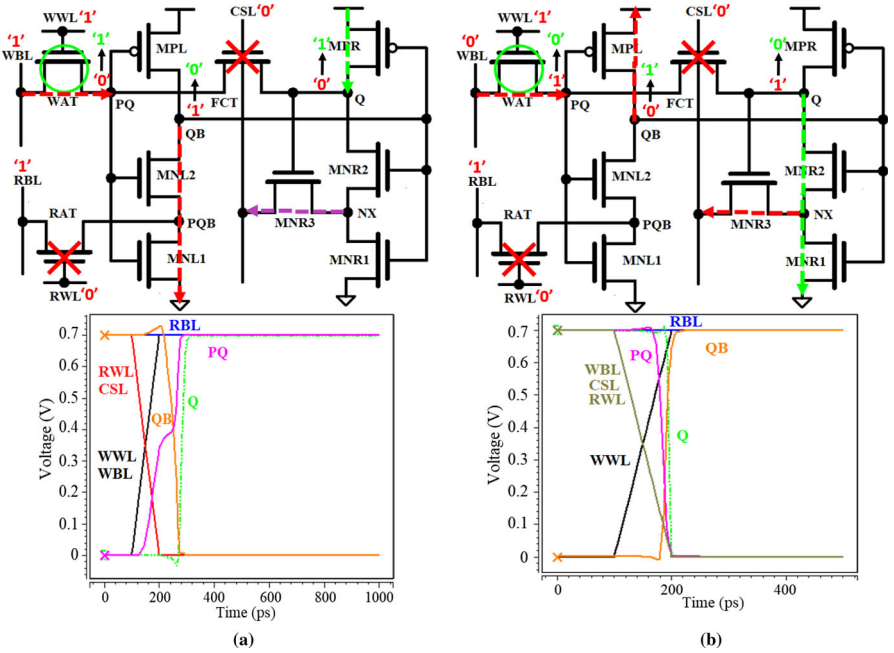

Fig. 5 **a** write '1' operation and **b** write '0' operation of the New10T SRAM cell along with their transient response

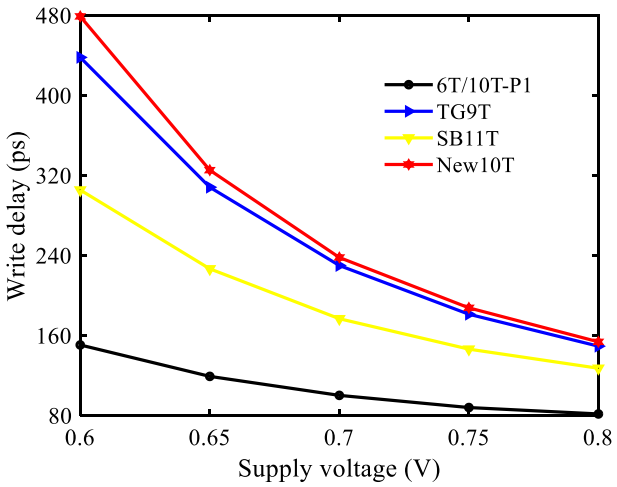

Fig. 6 T_{WA} of the tested SRAM cells versus V_{DD}

SRAM cells such as TG9T, SB11T, and New10T show higher T_{WA} than those of 6T and 10T-P1 SRAM cells with differential writing structure. The conventional 6T and 10T-P1 SRAM cells show the same and least T_{WA} among all the SRAM cells due to having a simple differential writing structure along with an NMOS write-access transistor in write paths. The SB11T SRAM cell uses a TG in its write path, which passes both strong '1' and '0' logic values, showing lower T_{WA} than that of the TG9T and New10T SRAM cells. The feedback-cutting transistor used in the TG9T and New10T SRAM cells increases the T_{WA}. This is due to the formation of two cascaded inverters in which one of them is followed by another one. These SRAM cells show the highest-T_{WA} among the compared SRAM cells. The New10T SRAM cell exhibits 2.37X higher T_{WA} compared with the best SRAM cell, that is conventional 6T.

3.3 Hold Static Noise Margin

In the hold mode of the New10T SRAM cell, the *WWL*/*RWL* is forced to ground to disable the write-/read-access transistor WAT/RAT. This removes the reading and writing paths. Moreover, the *CSL* is set to V_{DD} to establish the feedback path of the cell core and the feedback mechanism of the ST-based inverter offered by MNR3. Both *WBL* and *RBL* are kept at high. Therefore, the cell core is fully isolated from the read/write bitline; consequently, the cell state is maintained reliably by the cell core, as shown in Fig. 7.

The hold stability is gauged by hold static noise margin (HSNM). The HSNM is defined as the maximum DC noise voltage at each storage node that can be tolerated without altering the status of stored data during the hold operation [18]. Figure 8a, b shows the HSNM of the various SRAM cells at $V_{DD} = 0.7$ V and versus V_{DD}, respectively. It is graphically measured as the side length of the biggest square that can be embedded inside the smallest wing of the butterfly curves during the hold operation [1]. Combining the normal inverter with the ST inverter to form the cell core of the

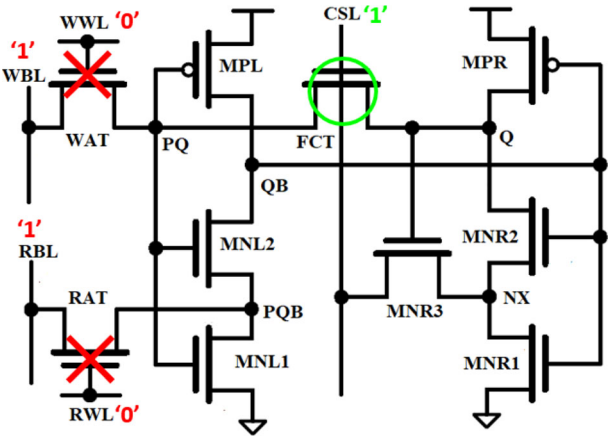

Fig. 7 Hold operation of the New10T SRAM cell

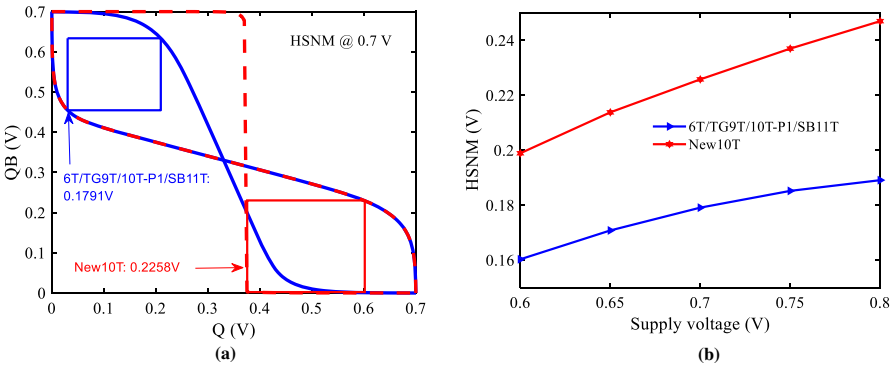

Fig. 8 HSNM of the various SRAM cells **a** at $V_{DD} = 0.7$ V and **b** versus V_{DD}

New10T SRAM cell enhances the HSNM. SRAM cells including 6T, TG9T, 10T-P1, and SB11T use normal cross-coupled inverters pair in their cell core and, therefore, show the lower HSNM compared with the proposed design. The New10T SRAM cell offers 1.26X higher HSNM compared with the above-mentioned SRAM cell at $V_{DD} = 0.7$ V.

3.4 Read Static Noise Margin

The read stability is evaluated by read static noise margin (RSNM). The RSNM is delineated as the maximum DC noise voltage at each storage node that can be sustained without altering the status of stored data during the read operation [8, 18]. Figure 9a shows the RSNM of the various SRAM cells at $V_{DD} = 0.7$ V, and Fig. 9b plots the RSNM of those SRAM cells versus V_{DD}. The RSNM is graphically obtained as the length of a side of the largest square that can be inserted inside the smallest wing of the butterfly curves during the read operation [1, 2]. The conventional 6T SRAM cell suffers from the read disturbance; hence, its RSNM is lower than HSNM. Other

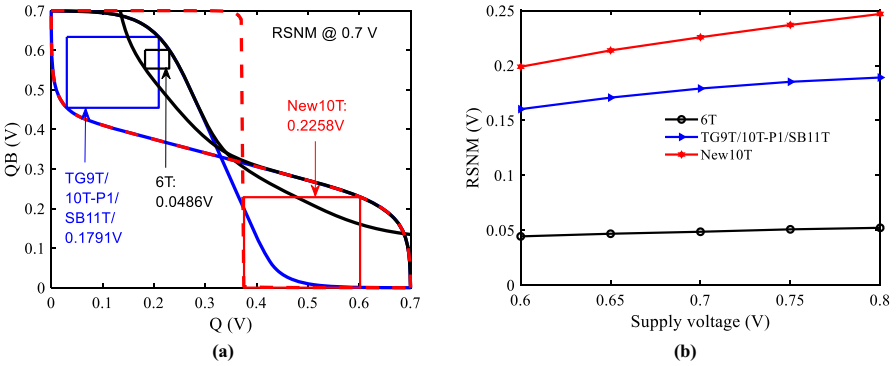

Fig. 9 RSNM of the various SRAM cells **a** at $V_{DD} = 0.7$ V and **b** versus V_{DD}

SRAM cells employ read decoupling technique in which internal data storing nodes are isolated from bitlines during the read operation, resulting in RSNM improvement. In these SRAM cells, the RSNM is almost equal to HSNM. The cell core of the proposed design constitutes a strong cross-coupled structure of the normal- and ST-based inverters. This along with the separated read path, which does not include the true storage nodes Q and QB, eliminates the read-disturbance issue; consequently, the RSNM improves. The New10T SRAM cell offers 4.65X/1.26X higher RSNM compared to the conventional 6T/TG9T SRAM cell at $V_{DD} = 0.7$ V.

3.5 Writability Analysis

The writability of an SRAM cell is characterized by write static noise margin (WSNM). The WSNM is defined as the ability of an SRAM cell to pull-down (up) a '1' ('0') storing node to a voltage lower (higher) than the switching threshold (V_{th}) of the other inverter '0' ('1') storing node, resulting in successful flipping the state of the cell [2]. To find the WSNM value, first, the read VTC of an SRAM cell, which is obtained in the previous section, should be combined with the write VTC of that cell, and then, the side length of the smallest square that can be inscribed between and lower-half of these two VTCs provides the WSNM [5]. Figures 10 and 11a show WSNM of the various SRAM cells at $V_{DD} = 0.7$ V and different V_{DD} values, respectively. SRAM cells such as TG9T, SB11T, and New10T use a single-ended writing structure. In these SRAM cells, writing '1' is difficult, and hence, a write-assist technique is required. The SB11T and TG9T/New10T SRAM cells use power-gated and feedback-cutting write-assist techniques, respectively, to eliminate the writing '1' issue. With the presence of two series-connected NMOS access transistors in its write path compared to SB11T SRAM cell, the TG9T SRAM cell shows considerably lower (1.05X) WSNM. The New10T SRAM cell shows the highest WSNM (1.65X higher than 6T cell) among all the tested SRAM cells at all supply voltage values considered for comparison. This

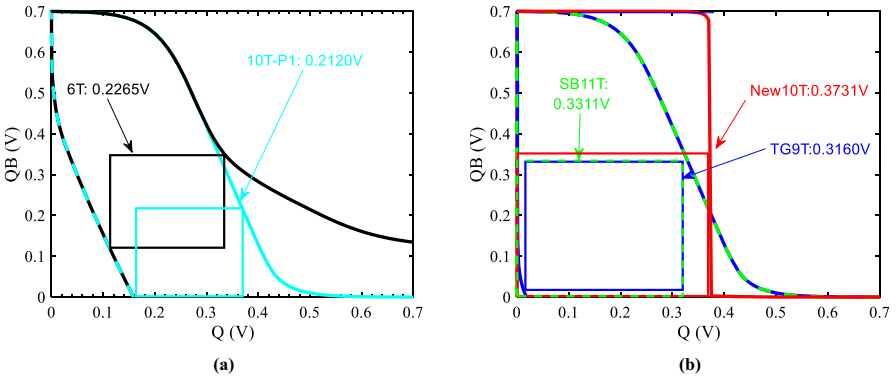

Fig. 10 WSNM of the various SRAM cells at $V_{DD} = 0.7$ V. **a** Differential writing bitcells and **b** single-ended writing bitcells

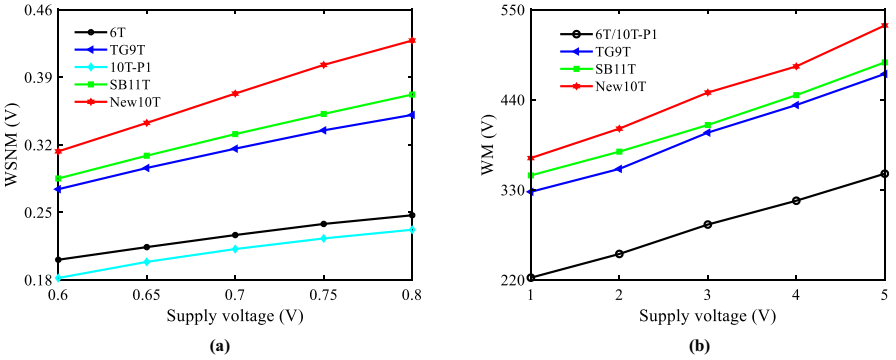

Fig. 11 **a** WSNM and **b** WM of the various SRAM cells versus V_{DD}

is due to the use of the write-assist mechanism along with a strong cross-coupled structure of the normal- and ST-based inverters.

Another metric to quantify the write-ability of an SRAM cell is the write margin (WM). Recent studies have shown that the WM technique is more appropriate than the traditional butterfly static noise margin to estimate the write-ability of an SRAM cell [2, 9]. To measure the WM, first, the desired data are applied on bitlines and then wordline (WL) is swept from zero to the power supply voltage (V_{DD}). The WM is defined as the voltage difference between V_{DD} and WL while flipping the internal storage nodes Q and QB [2]. Figure 11b shows the WM of the studied SRAM cells at different V_{DD} values. Due to the same reasons, the New10T SRAM cell shows the highest WM among all the SRAM cells. The WM of the New10T SRAM cell at V_{DD} = 0.7 V is 1.56X higher than that of the conventional 6T SRAM cell.

3.6 Dynamic Power Consumption

Dynamic power (P_{Dyn}) is defined as power consumed by an SRAM cell when it is accessed [27]. The P_{Dyn} has two main components including dynamic read power and dynamic write power. The dynamic write power consumption is the large percentage of the total dynamic power consumption due to fully discharging the bitlines capacitance during the write operation [2, 3]. Hence, we compared the dynamic power consumption of the different SRAM cells during the write operation, as shown in Fig. 12. Due to the existence of a direct relation between the switching activity factor of bitlines ($\alpha_{bitline}$) and P_{Dyn}, SRAM cells with differential writing structure consume higher P_{Dyn} compared with single-ended writing bitcells. The SB11T SRAM cell shows the highest P_{Dyn} among all the tested SRAM cells due to the connection of several transistors to the same bitline, which increases overall bitline capacitance. The New10T SRAM cell offers the lowest P_{Dyn} due to its single-ended writing structure and its highest write delay. The P_{Dyn} of the proposed design is 1.64X lower than that of the conventional 6T SRAM cell at V_{DD} = 0.7 V.

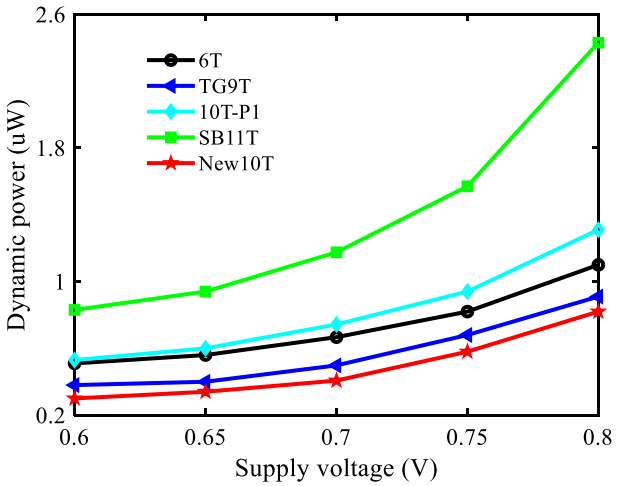

Fig. 12 Dynamic power of the various SRAM cells versus V_{DD}

3.7 Leakage Power Dissipation

As technology nodes scale down to a deep submicron regime, the subthreshold leakage in embedded memory has turned into a crucial concern [12]. The leakage power (P_{Leak}) of an SRAM cell is the main contributor to its total power in the advanced technology because a major part of the cache remains in the hold mode most of the time [2, 3]. Figure 13 shows the comparison of P_{Leak} of the different SRAM cells at different V_{DD} values. The SB11T and 10T-P1 SRAM cells exhibit higher P_{Leak} than that of the conventional 6T SRAM cell due to higher bitline capacitance and higher count of

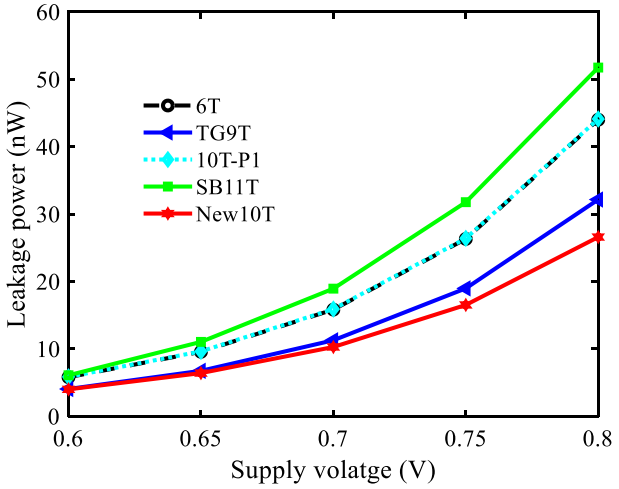

Fig. 13 Leakage power of the various SRAM cells versus V_{DD}

bitlines, respectively. The New10T SRAM cell shows the least P_{Leak} (1.54X lower than 6T cell). This improvement in P_{Leak} of the New10T SRAM cell is due to the presence of stacking of transistors during both hold '0' and hold '1' state and its single-ended structure. The double-length pull-up transistor in the ST-based inverter further reduces P_{Leak}.

3.8 Monte Carlo (MC) Simulation of PVT variations

In advanced technologies, the impact of PVT variations on the various performance metrics of an SRAM cell becomes significant, especially in low-V_{DD} domain. Therefore, it is necessary to design an SRAM cell that can overcome severe PVT variations. In this section, we perform Monte Carlo (MC) simulations with 10,000 samples to take into account the impact of severe PVT variations on the static noise margin (SNM) of the studied SRAM cells during the hold, read, and write operations. Figure 14 shows the Gaussian distribution plots of HSNM, RSNM, and WM for all the studied SRAM cells. In this comparison, the WM is used because it is more appropriate than the WSNM to show the ability of an SRAM cell during the write operation [4]. In the New10T SRAM cell, the cell core is formed by combining normal- and ST-based

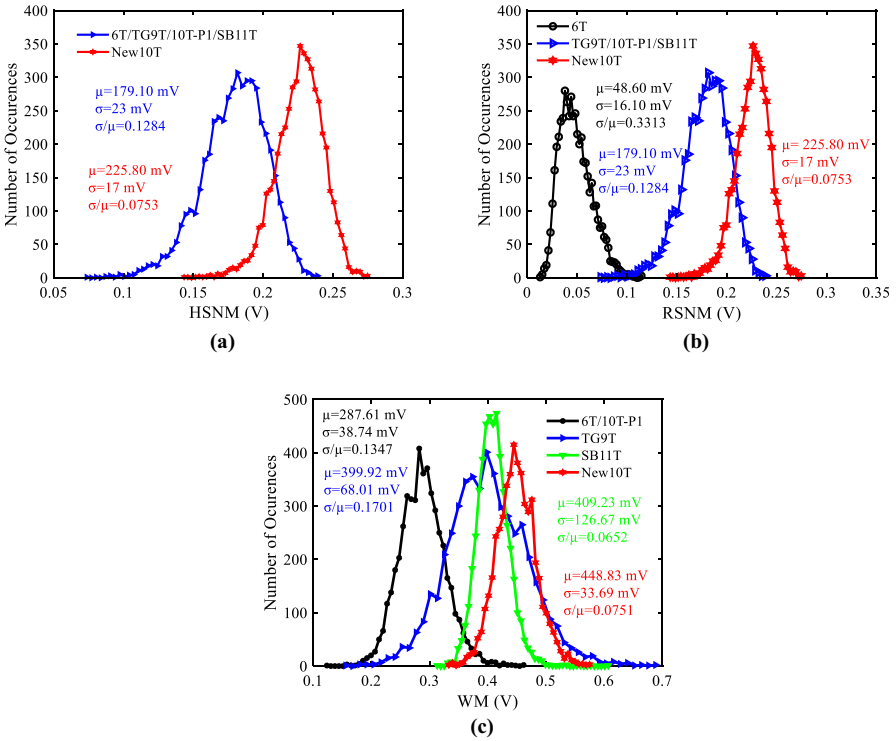

Fig. 14 Distribution plots of **a** HSNM, **b** RSNM, and **c** WM for different SRAM cells at $V_{DD} = 0.7$ V

inverters, resulting in PVT variation mitigation. The proposed design shows 1.71X lower variability in HSNM compared with the conventional 6T SRAM cell.

It is observed from Fig. 14b, which shows the Gaussian distribution plots of RSNM, that the conventional 6T SRAM cell suffers highly from the read disturbance, showing higher RSNM variability than those of other remaining SRAM cells in which data storing nodes are decoupled from bitline(s) during the read operation. The New10T SRAM cell exhibits 4.40X lower variability in RSNM compared with the conventional 6T SRAM cell due to the same reasons for HSNM.

The Gaussian distribution plots of WM for different bitcells are shown in Fig. 14c. Due to the use of ST-based inverters and high-WM, the New10T SRAM cell overcomes PVT variations, resulting in WM variability reduction. SRAM cells including TG9T and SB11T utilize normal inverter and write-assist technique and therefore show lower variability in WM. Based on the obtained results, the New10T SRAM cell has 1.79X lesser variability in WM than that of the conventional 6T SRAM cell.

3.9 Layout Area and Comprehensive Metric

Figure 15 shows the layout of the New10T SRAM cell. The conventional 6T SRAM cell has a compact and simple structure with a minimum count of transistors, and therefore, it occupies 0.81X lesser area compared to New10T SRAM cell. The thirteenth row of Table 2 reports the SRAM cells' area normalized to that of conventional 6T SRAM cell. It can be observed that the proposed design is the second-best SRAM cell based on layout area.

Due to the existence of a trade-off among various design metrics of an SRAM cell, a comprehensive metric is required to estimate the overall quality of that SRAM cell [12]. The proposed figure of merit (FOM) defined as Eq. (1) and reported in the last row of Table 2 implies that the proposed cell is the best design among all the studied SRAM cells. Therefore, the New10T SRAM cell can be a good choice for low-power portable applications.

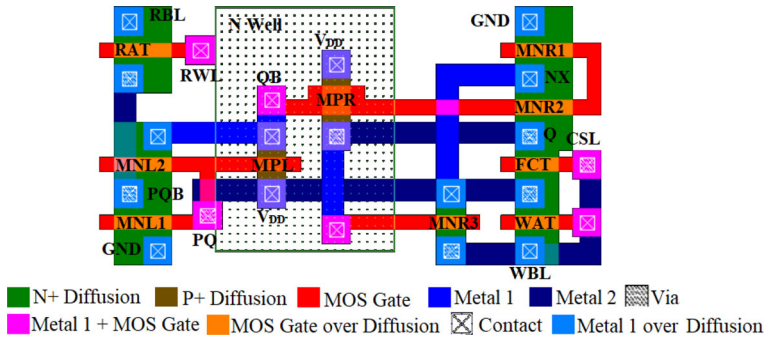

Fig. 15 Layout of the New10T SRAM cell

Table 2 Design metrics comparison of the various SRAM cells at $V_{DD} = 0.7$ V

Design metrics	6T [19]	TG9T [27]	10T-P1 [17]	SB11T [22]	New10T (This work)
HSNM (mV)	179.10	179.10	179.10	179.10	225.80
RSNM (mV)	48.60	179.10	179.10	179.10	225.80
WSNM (mV)	226.50	316.0	212.0	331.10	373.10
WM (mV)	287.61	399.92	287.61	409.23	448.83
σ/μ of HSNM	0.1284	0.1284	0.1284	0.1284	0.0753
σ/μ of RSNM	0.3313	0.1284	0.1284	0.1284	0.0753
σ/μ of WM	0.1347	0.1701	0.1347	0.0652	0.0751
T_{RA} (ps)	127.60	500.01	771.35	1379.70	500.01
T_{WA} (ps)	100.23	230.02	100.23	176.84	238.04
Dynamic power (μW)	0.667	0.498	0.743	1.175	0.407
Leakage power (nW)	15.83	11.28	15.91	18.94	10.28
Normalized Area	1	1.48	1.43	1.57	1.24
Normalized FOM	1	1.48	0.98	0.44	26.90

$$FOM = \frac{(HSNM \times RSNM \times WM}{\left(\frac{\sigma}{\mu} HSNM \times \frac{\sigma}{\mu} RSNM \times \frac{\sigma}{\mu} WM\right)} \times \frac{1}{(T_{RA} \times T_{WA} \times P_{Dyn} \times P_{Leak} \times Area)}. \tag{1}$$

4 Conclusion

In this paper, a highly stable and robust 10T SRAM cell is proposed, which is appropriate for low-power portable applications. The cell core of the New10T is formed by a normal inverter with a stacked transistor and a Schmitt-trigger (ST)-based inverter. Separate bitlines are used to perform read and write operations. The read disturbance is eliminated by the proposed design due to the use of an isolated read path along with a strong cell core. Furthermore, the writing '1' issue in the proposed single-ended design is removed with the aid of a feedback-cutting write-assist technique. Based on the obtained results given in Table 2 at $V_{DD} = 0.7$ V, the New10T design offers the highest HSNM/RSNM/WSNM (WM). Due to the single-ended reading/writing structure, the New10T SRAM cell shows 3.92X/2.37X higher read/write delay compared with the 6T SRAM cell. The dynamic/leakage power of the proposed cell is 1.64X/1.54X lower than that of 6T SRAM cell. This improvement is achieved due to its single-ended nature and the presence of stacked transistors in its cell core. Though the proposed cell consumes a 1.24X higher area compared with the 6T SRAM cell, it

shows the highest proposed FOM among all the SRAM cells, making it a good choice for low-power portable applications.

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Data Availability The associated data will be made available on reasonable request.

References

1. E. Abbasian, M. Gholipour, A variation-aware design for storage cells using Schottky-barrier-type GNRFETs. J. Comput. Electron. **19**, 987–1001 (2020). https://doi.org/10.1007/s10825-020-01529-y
2. E. Abbasian, M. Gholipour, Design of a Schmitt-Trigger-based 7T SRAM cell for variation resilient low-energy consumption and reliable internet of things applications. AEU-Int. J. Electron. Commun. **138**, 153899 (2021). https://doi.org/10.1016/j.aeue.2021.153899
3. E. Abbasian, M. Gholipour, Single-ended half-select disturb-free 11T static random access memory cell for reliable and low power applications. Int. J. Circuit Theory Appl. **49**(4), 970–989 (2021). https://doi.org/10.1002/cta.2954
4. E. Abbasian, M. Gholipour, A low-leakage single-bitline 9T SRAM cell with read-disturbance removal and high writability for low-power biomedical applications. Int. J. Circuit Theory Appl. (2022). https://doi.org/10.1002/cta.3231
5. E. Abbasian, M. Gholipour, F. Izadinasab, Performance evaluation of GNRFET and TMDFET devices in static random access memory cells design. Int. J. Circuit Theory Appl. **49**(11), 3630–3652 (2021). https://doi.org/10.1002/cta.3108
6. E. Abbasian, S. Birla, M. Gholipour, A 9T high-stable and Low-Energy Half-Select-Free SRAM Cell Design using TMDFETs. Analog Integr. Circuit Sig. Process. **11**, 1–9 (2022). https://doi.org/10.1007/s10470-022-02036-9
7. E. Abbasian, S. Birla, M. Gholipour, Ultra-low-power and stable 10-nm FinFET 10T sub-threshold SRAM. Microelectron. J. (2022). https://doi.org/10.1016/j.mejo.2022.105427
8. E. Abbasian, M. Gholipour, S. Birla, A single-bitline 9T SRAM for low-power near-threshold operation in FinFET technology. Arab. J. Sci. Eng. (2022). https://doi.org/10.1007/s13369-022-06821-6
9. E. Abbasian, F. Izadinasab, M. Gholipour, A reliable low standby power 10T SRAM cell with expanded static noise margins. IEEE Trans. Circuits Syst. I Regul. Pap. **69**(4), 1606–1616 (2022). https://doi.org/10.1109/TCSI.2021.3138849
10. E. Abbasian, E. Mani, M. Gholipour, M. Karamimanesh, M. Sahid, A. Zaidi, A Schmitt-Trigger-based low-voltage 11 T SRAM cell for low-leakage in 7-nm FinFET technology. Circuits Syst. Signal Process. **41**, 3081–3105 (2022). https://doi.org/10.1007/s00034-021-01950-z
11. S. Ahmad, M.K. Gupta, N. Alam, M. Hasan, Single-ended Schmitt-trigger-based robust low-power SRAM cell. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **24**(8), 2634–2642 (2016). https://doi.org/10.1109/TVLSI.2016.2520490
12. S. Ahmad, M.K. Gupta, N. Alam, M. Hasan, Low leakage single bitline 9T (SB9T) static random access memory. Microelectron. J. **62**, 1–11 (2017). https://doi.org/10.1016/j.mejo.2017.01.011
13. S. Ahmad, B. Iqbal, N. Alam, M. Hasan, Low leakage fully half-select-free robust SRAM cells with BTI reliability analysis. IEEE Trans. Device Mater. Reliab. **18**(3), 337–349 (2018). https://doi.org/10.1109/TDMR.2018.2839612
14. D. Anh-Tuan, J.Y.S. Low, J.Y.L. Low, Z.-H. Kong, X. Tan, K.-S. Yeo, An 8T differential SRAM with improved noise margin for bit-interleaving in 65 nm CMOS. IEEE Trans. Circuits Syst. I Regul. Pap. **58**, 1252–1263 (2011). https://doi.org/10.1109/TCSI.2010.2103154
15. L. Chang, D.M. Fried, J. Hergenrother, J.W. Sleight, R.H. Dennard, R.K. Montoye, et al., Stable SRAM cell design for the 32 nm node and beyond, in *Dig. Tech. Pap. 2005 Symp. VLSI Technol. 2005* (2005), pp. 128–129. https://doi.org/10.1109/.2005.1469239.
16. K. Cho, J. Park, T.W. Oh, S.-O. Jung, One-Sided Schmitt-Trigger-based 9T SRAM Cell for near-threshold operation. IEEE Trans. Circuits Syst. I Regul. Pap. **67**(5), 1551–1561 (2020). https://doi.org/10.1109/TCSI.2020.2964903

17. S. Gupta, K. Gupta, B.H. Calhoun, N. Pandey, Low-power near-threshold 10T SRAM bit cells with enhanced data-independent read port leakage for array augmentation in 32-nm CMOS. IEEE Trans. Circuits Syst. I Regul. Pap. **66**(3), 978–988 (2018). https://doi.org/10.1109/TCSI.2018.2876785
18. Y. He, J. Zhang, X. Wu, X. Si, S. Zhen, B. Zhang, A half-select disturb-free 11T SRAM cell with built-in write/read-assist scheme for ultralow-voltage operations. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **27**(10), 2344–2353 (2019). https://doi.org/10.1109/TVLSI.2019.2919104
19. M.R. Jan, C. Anantha, N. Borivoje, *Digital integrated circuits—a design perspective* (Prentice-Hall, Upper Saddle River, 2003)
20. J.P. Kulkarni, K. Roy, Ultralow-voltage process-variation-tolerant Schmitt-trigger-based SRAM design. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **20**(2), 319–332 (2012). https://doi.org/10.1109/TVLSI.2010.2100834
21. J.P. Kulkarni, K. Kim, K. Roy, A 160 mV robust Schmitt trigger based subthreshold SRAM. IEEE J. Solid-State Circuits **42**(10), 2303–2313 (2007). https://doi.org/10.1109/JSSC.2007.897148
22. R. Lorenzo, R. Pailly, Single bit-line 11T SRAM cell for low power and improved stability. IET Comput. Digit. Tech. **14**(3), 114–121 (2020). https://doi.org/10.1049/iet-cdt.2019.0234
23. N. Maroof, B.-S. Kong, 10T SRAM using Half-V_{DD} precharge and row-wise dynamically powered read port for low switching power and ultralow RBL leakage. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **25**(4), 1193–1203 (2016). https://doi.org/10.1109/TVLSI.2016.2637918
24. M. Nabavi, M. Sachdev, A 290-mV, 3.34-MHz, 6T SRAM with pMOS access transistors and boosted wordline in 65-nm CMOS technology. IEEE J. Solid-State Circuits **53**(2), 656–667 (2017). https://doi.org/10.1109/JSSC.2017.2747151
25. D. Nayak, D.P. Acharya, K. Mahapatra, A read disturbance free differential read SRAM cell for low power and reliable cache in embedded processor. AEU-Int. J. Electron. Commun. **74**, 192–197 (2017). https://doi.org/10.1016/j.aeue.2017.02.012
26. T.W. Oh, H. Jeong, K. Kang, J. Park, Y. Yang, S.-O. Jung, Power-gated 9T SRAM cell for low-energy operation. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **25**(3), 1183–1187 (2016). https://doi.org/10.1109/TVLSI.2016.2623601
27. S. Pal, S. Bose, W.-H. Ki, A. Islam, Characterization of half-select free write assist 9T SRAM cell. IEEE Trans. Electron Devices **66**(11), 4745–4752 (2019). https://doi.org/10.1109/TED.2019.2942493
28. Predictive Technology Model (PTM), [Online], Available: http://ptm.asu.edu/.