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High Energy Efficiency and Linearity Switching Scheme Without Reset Energy for SAR ADC

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Abstract

A high energy efficiency and linearity switching scheme is proposed for the successive approximation register (SAR) analog-to-digital converter (ADC). With the tri-level switching scheme, the capacitor area is reduced by 75% compared with the conventional switching scheme. In addition, the proposed switching scheme also combines the most significant bit (MSB) splitting method and the monotonic switching scheme for linearity and energy efficiency improvement. Furthermore, by inserting a connection switch between the MSB splitting capacitors and the least significant bit (LSB) capacitors, the reset energy can be avoided. The MATLAB simulation results show that compared to the monotonic switching scheme, the proposed switching scheme achieves a 93.29% reduction in average switching energy and 50% capacitor area saving without the reset energy when the parasitic capacitance is taken into consideration. Meanwhile, the linearity is enhanced by $\sqrt{2}\times$ from the Monte Carlo simulation. The post-simulation results indicate that a 10-bit SAR ADC with the proposed switching scheme can achieve a signal-to-noise distortion ratio (SNDR) of 57.81 dB and a spurious-free dynamic range (SFDR) of 68.63 dB at the sampling rate of 1 MS/s in a 180-nm CMOS process. The SAR ADC consumes 15.25 μW power at a 1 V supply, resulting in a figure of merit (FoM) of 24.03 fJ/conv.-step. The active area of this ADC is only 0.057 mm^2.

Keywords SAR ADC · High energy efficiency · No reset energy · High linearity

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1 Introduction

Recently, charge redistribution successive approximation register (SAR) analog-to-digital converter (ADC) has been a dominant implementation in biomedical electronics, wireless sensor networks, and wearable detection devices due to its low power consumption and digital-like structure [1, 9, 20, 24, 25]. The power consumption of the digital circuit is significantly diminished, but the switching energy of the capacitive digital-to-analog converter (DAC) array is still not satisfactory even in the advanced process.

Different switching schemes have been presented to reduce the switching energy [1, 4, 10, 14, 17, 19, 20, 24]. Compared with the conventional switching scheme, the methods based on Hybrid [4, 15], and V_{cm}-based-like scheme [18] dissipate the additional reset energy which occupies a dominant proportion of total switching energy, leading to the average switching energy reduction only to 89.47, 96.50, and 89.07%, respectively. Furthermore, the closed-loop charge recycling method presented in [7] realizes 100% switching energy reduction at the expense of the capacitor area. Tong [16] saves 75% area overhead with only $\sqrt{2}\times$ INL performance enhancement. Besides, the switching energy reduction in [4] and [11] is also attenuated by 0.56 and 0.89% due to the parasitic capacitance, respectively. Overall, it is a challenge to meet the excellent energy efficiency and linearity performance requirement simultaneously when the reset energy and parasitic capacitance are taken into account.

To cope with the above-stated drawbacks, a novel switching scheme is proposed in this paper for the low-power SAR ADC. Taking advantage of the tri-level switching scheme, the capacitor area is decreased by 75% compared with the conventional switching scheme. Besides, the MSB capacitor splitting method and monotonic switching scheme are adopted to improve linearity and energy efficiency. In addition, the reset energy can be avoided by inserting a connection switch between the MSB splitting capacitors and the LSB capacitors. The behavioral simulation results indicate that compared to the monotonic switching method, the proposed switching scheme obtains a 93.29% reduction in average switching energy and 50% capacitor area saving with the parasitic capacitance consideration. The linearity performance has a $\sqrt{2}\times$ improvement from the Monte Carlo simulation. The simulation results are aligned with the theoretical analysis. The post-simulation results show that an SNDR of 57.81 dB and an SFDR of 68.63 dB can be realized in a 10-bit SAR ADC with the proposed switching scheme at the sampling rate of 1 MS/s in a 180-nm CMOS process. The SAR ADC consumes 15.25 μW power at a 1 V supply, resulting in an FoM of 24.03 fJ/conv.-step. The active area of this ADC is only 0.057 mm^2.

The organization of this paper is as follows. Section 2 presents the structure of the proposed switching scheme. Analysis and discussion about the switching scheme and a SAR ADC are demonstrated in Sect. 3. Section 4 gives the simulation results. Finally, the conclusion is drawn in Sect. 5.

2 The Proposed Switching Scheme

The SAR ADC with the proposed switching scheme in Fig. 1 consists of the sample-and-hold circuits (S_{p1}/S_{n1} and S_{p0}/S_{n0}), the connection switches (S_{p2} and S_{n2}), the capacitive DAC array (C_{pm}, C_{pl}, C_{nm}, C_{nl}), a comparator, and a dynamic SAR logic. For an N-bit conventional SAR ADC, 2 N flip-flops are required at least in SAR logic [16]. In this paper, the dynamic SAR control logic in [26] is adopted to reduce power and complexity. The MSB capacitor $128C$ is split into 8 capacitors (64, 32, 16, 8, 4, $2C$, C, C), which have the identical binary form to the LSB capacitors. C_{pl} and C_{nl} are the LSB capacitors, and C_{pm} and C_{nm} are the MSB splitting capacitors.

Figure 2 shows the proposed switching scheme in a 4-bit capacitive DAC array. In the sampling phase, the MSB splitting capacitors and the LSB capacitors are separated by the connection switches S_{p2}/S_{n2}, and they sample the input signal through the switches S_{p1}/S_{n1} and S_{p0}/S_{n0}, respectively. Meanwhile, the bottom plates of the C_{pm}/C_{nm} and C_{pl}/C_{nl} are connected to V_{ref} and V_{cm}, respectively. After the sampling phase, the S_{p2} and S_{n2} are closed, and the MSB bit is obtained immediately. There is no energy consumption during the first comparison. Based on the MSB bit result, if $V_{ip} > V_{in}$, V_{ip} is decreased by $V_{ref}/2$ through switching the bottom plate voltages of the C_{pm} and C_{pl} to V_{cm} and Gnd, respectively. Meanwhile, the voltage V_{in} remains unchanged. Or vice versa in the case of the $V_{ip} < V_{in}$. There is still no energy consumption in this process because the voltage change on each capacitor is 0.

We take MSB bit = 1 as an example and suppose that the top plate voltage of the P-terminal capacitive DAC array is V_1 and V_2 before and after the second comparison, respectively, as shown in Fig. 3. According to the law of charge conservation, there is

$$(V_2 - V_{cm})C_{pm} + (V_2 - 0)C_{pl} = (V_1 - V_{ref})C_{pm} + (V_1 - V_{cm})C_{pl} \tag{1}$$

thus, $V_2 = V_1$-V_{cm} can be obtained. During this conversion process, the reference voltage V_{cm} consumes the energy (E) as follows:

$$E = V_{cm}[(V_{cm} - V_{ref}) - (V_2 - V_1)]C_{pm} = 0. \tag{2}$$

By doing this, the sub-MSB bit can be resolved. According to the sub-MSB bit result, if $V_{ip} > V_{in}$, V_{ip} is diminished by $V_{ref}/4$ through switching the bottom plate

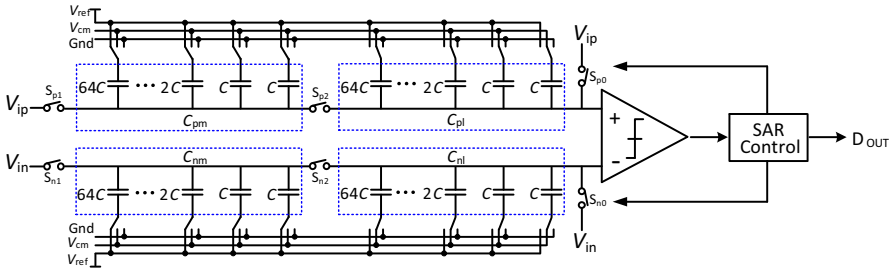

Fig. 1 Block diagram of the SAR ADC with the proposed switching scheme

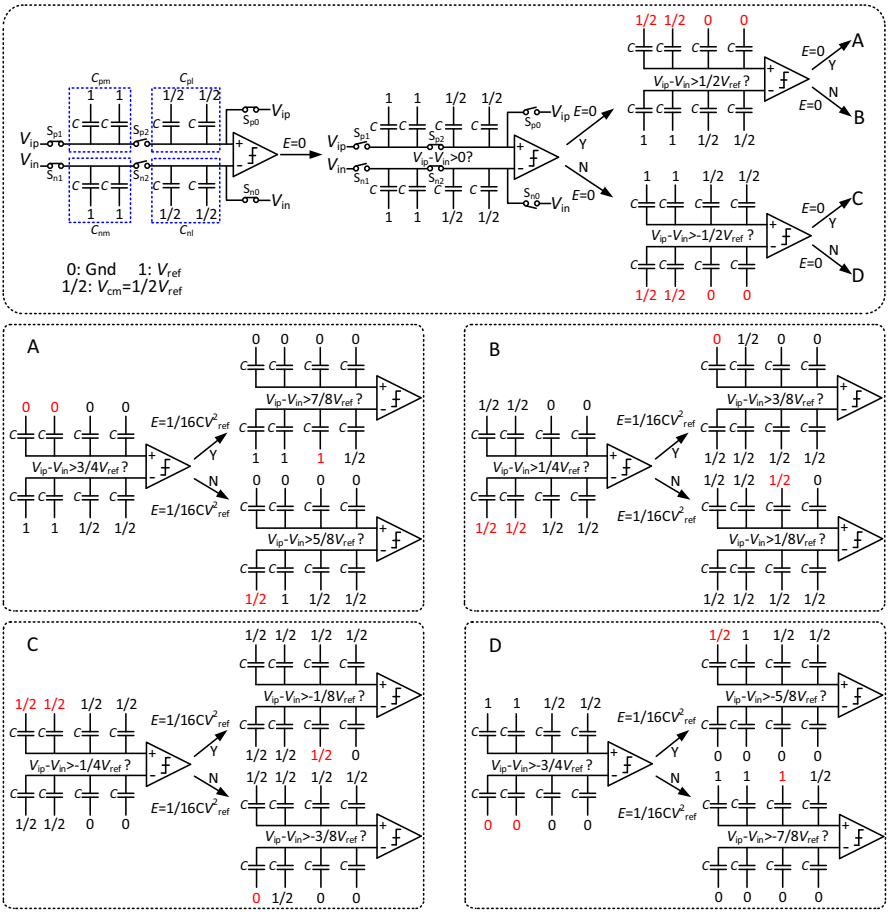

Fig. 2 Proposed SAR ADC switching scheme

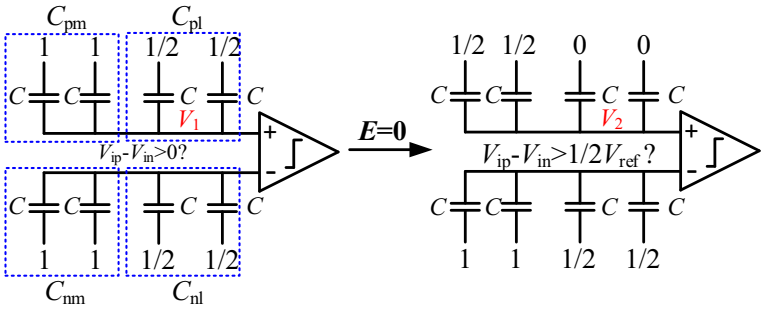

Fig. 3 The generation process of sub-MSB bit when MSB bit is 1

voltage of the C_{pm} from V_{cm} to Gnd (Case: A) or from V_{ref} to V_{cm} (Case: C), respectively. Otherwise, V_{in} is reduced by $V_{ref}/4$ through converting the bottom plate voltage of the C_{nm} from V_{ref} to V_{cm} (Case: B) or V_{cm} to Gnd (Case: D), respectively. The switching energy isn't dissipated during the second conversion process due to the same magnitude and opposite polarity in voltage fluctuation of the MSB splitting capacitors and LSB capacitors. To generate the rest of the bits, only monotonic switching is required and only one capacitor's bottom plate voltage is altered during each comparison until the rest of the bits are obtained. The proposed method is different from the method in [25], further reducing power consumption.

The contributions of the proposed switching scheme have been summarized in terms of power and linearity over other methods. Firstly, compared to the monotonic switching scheme in [9], the proposed switching scheme has the same common-mode voltage variation, but the linearity performance has a $\sqrt{2}\times$ improvement. It achieves good linearity because the generation of the MSB bit and the sub-MSB bit doesn't depend on the capacitor mismatch. The reference voltage of the capacitor bottom plate is not changed during the MSB bit generation and the voltage change on each capacitor is 0 during the sub-MSB bit generation. Secondly, the proposed switching scheme has higher energy efficiency than the monotonic switching scheme. Besides, compared to the switching scheme in [11], switching energy is increased by only $4.57CV_{ref}{}^2$ when the parasitic capacitance is taken into consideration. Thirdly, the tri-level switching scheme in [22] has the common-mode voltage variation from V_{cm} to V_{DD}. Therefore, the noise and static offset of the comparator can become more and more severe because the common-mode voltage is gradually increased during the all-bits generation process. In the proposed switching scheme, this issue is solved and the average switching energy reduction has an obvious advantage over that of the tri-level switching scheme (96.89%). Finally, except for the splitting of the MSB capacitor and the inclusion of the connection switches, the switching scheme combining the tri-level and monotonic switching schemes in [11] has two common-mode voltage variation situations (from V_{cm} to V_{DD} or Gnd) while the proposed switching scheme has a unique common-mode voltage variation situation (from V_{cm} to Gnd). Hence, it relaxes the design requirement of the dynamic comparator.

3 Analysis and Discussion

3.1 Common-Mode Voltage Variation

The dynamic comparator is indispensable for the SAR ADC design. The static offset voltage of the Strong-Arm comparator in Fig. 4 only can shrink the dynamic range while the dynamic offset caused by the common-mode voltage variation can worsen the linearity and bring in distortions. The common-mode voltage variation of the proposed switching scheme in the conversion process varies from the common-mode level (V_{cm}) to Gnd in the worst case from Fig. 5.

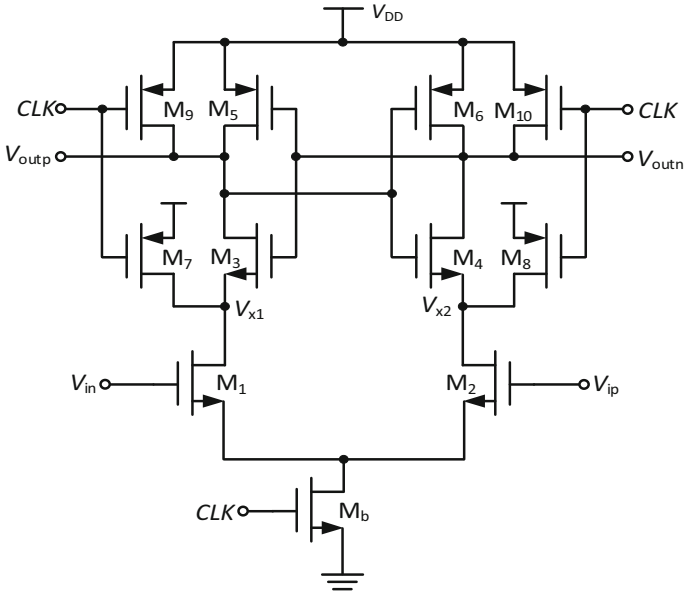

Fig. 4 Dynamic Strong-Arm comparator

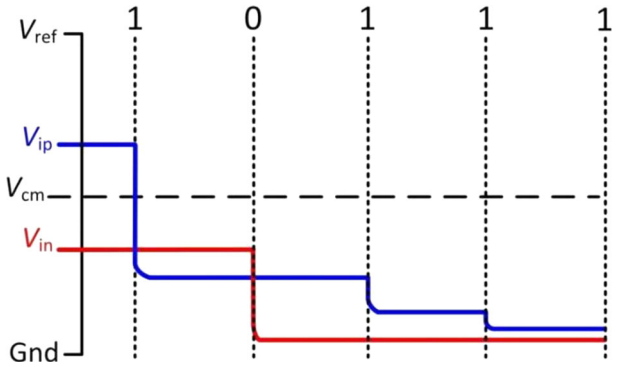

Fig. 5 Output waveform of the capacitor array with the proposed switching scheme

The operation process of the Strong-Arm comparator can be divided into a pre-amplification and a latch. The root mean square (RMS) of the input-referred offset V_{os} and the gain of pre-amplification (G) can be expressed as from [2].

$$\sigma_{os} = \sqrt{\sigma^2_{os,preamp} + \frac{\sigma^2_{os,latch}}{G^2}} \tag{3}$$

$$G = \frac{g_m}{I_D}\left[V_{Tp5,6} + \frac{C_x}{C_o}\left(V_{Tp5,6} + V_{Tp3,4}\right)\right] \tag{4}$$

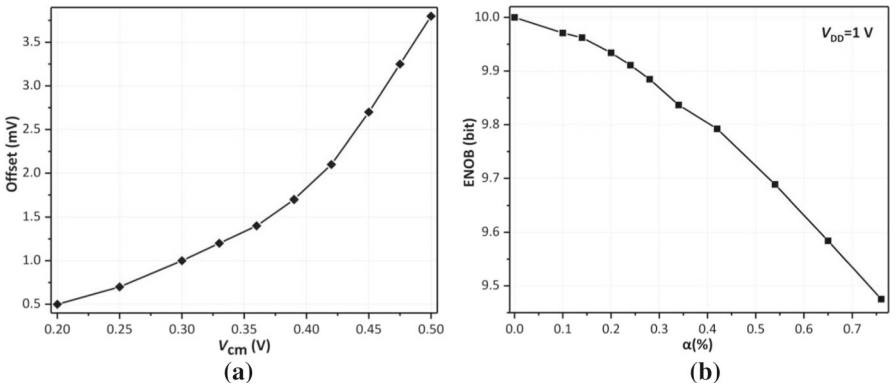

Fig. 6 (**a**) Offset versus V_{cm} and (**b**) ENOB versus influence factor α

where C_x and C_o are the parasitic capacitances at $V_{x1,2}$ node and $V_{outp,n}$ node, respectively.

From the (3) and (4), the gain of pre-amplification can be intensely influenced by the common-mode level, and it is increased with the decline of the common-mode level and the overdrive voltage of the input pair (M_1/M_2) during the conversion process. Thus, the RMS of latch offset voltage ($\sigma_{os,latch}$) can be attenuated, which optimizes the dynamic offset.

Figure 6a shows the variation of the comparator offset voltage with V_{cm} at a 1 V supply. The dynamic offset voltage is decreased with the reduction of V_{cm}. The behavioral model of a 10-bit SAR ADC is used to verify dynamic offset voltage variation sensitivity. Figure 6b delineates that the effective number of bits (ENOB) changes with the influence factor α, which is determined by the comparator dynamic offset.

3.2 Reset Energy

The most of the previous switching schemes only focused on the energy of the capacitive DAC array during the sampling phase and the conversion phase. In fact, the reset energy of many switching schemes is far greater than the switching energy of the conversion phase.

We suppose that the final state of the capacitive DAC array bottom plate is [V_1, $V_2 \ldots V_n$] and the initial state is [V_0, $V_0 \ldots V_0$]. The voltage of the top plate is changed from V_A to V_B by reset operation. According to the law of charge conservation, we can get

$$\sum_{i=1}^{N} (V_0 - V_i)C_i = \sum_{i=1}^{N} (V_A - V_B)C_i. \tag{5}$$

It can be concluded from (5)

$$V_{\mathrm{B}} - V_{\mathrm{A}} = \frac{\sum_{i=1}^{N} (V_0 - V_i) C_i}{\sum_{i=1}^{N} C_i}. \tag{6}$$

The expression of the reset energy is

$$E_{\mathrm{reset}} = V_0 \sum_{i=1}^{N} C_i [(V_0 - V_i) - (V_{\mathrm{A}} - V_{\mathrm{B}})]. \tag{7}$$

By substituting (6) into (7), we can get

$$E_{\mathrm{reset}} = V_0 \left[\sum_{i=1}^{N} C_i (V_0 - V_i) - \sum_{i=1}^{N} C_i \frac{\sum_{i=1}^{N} (V_0 - V_i) C_i}{\sum_{i=1}^{N} C_i} \right] = 0 \tag{8}$$

It can be concluded that if the initial voltages of the bottom plates are the same, there is no reset energy between two sampling cycles, which is independent of the final states of the bottom plates. However, the initial voltages of the bottom plates are different, which leads to nonzero reset energy. Therefore, the scheme shown in Fig. 7 is adopted to avoid the reset energy. After the LSB bit is obtained, the connection switches S_{p2}/S_{n2} are turned off, and then the C_{pm} and C_{pl} are reset to V_{ref} and V_{cm} in Fig. 7b, respectively. The analysis from (5) to (8) shows that the process doesn't consume any energy. To avoid charge redistribution in this procedure, the C_{pm} and C_{pl} sample the input signal individually as shown in Fig. 7c. Once the sampling phase is completed, the connection switches S_{p2}/S_{n2} are turned on and the conversion phase begins. This process is illustrated in Fig. 7d. It can be seen from the above analysis that the reset energy of the proposed switching scheme is zero.

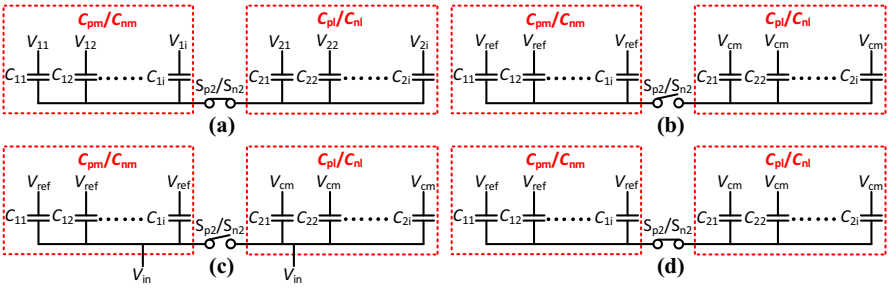

Fig. 7 Description of reset scheme

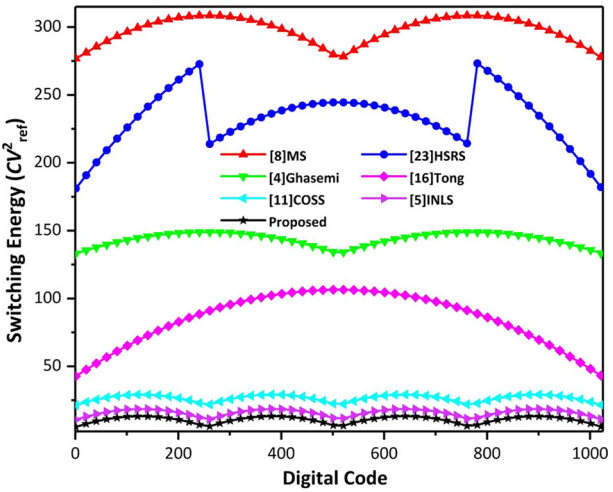

Fig. 8 Switching energy (including reset energy) versus output code for 10-bit SAR ADC

3.3 Switching Energy

The average switching energy of the proposed switching scheme for an N-bit SAR ADC can be calculated as

$$E_{\text{avg}} = CV_{\text{ref}}^2 \sum_{i=4}^{N} (2^{N-i-3} - 2^{N-2i}), \quad (N \geq 4). \tag{9}$$

According to (9), it can be calculated as only $10.54CV^2{}_{\text{ref}}$, which achieves 99.23% and 95.87% average switching energy reduction over the conventional and monotonic schemes, respectively. Figure 8 displays the behavioral simulation of the switching energy (including reset energy) of the proposed switching scheme and other schemes for 10-bit SAR ADC. The proposed method has the lowest average switching energy.

3.4 Parasitic Capacitance Effect on Switching Energy

The parasitic capacitance is a major source of energy consumption. As shown in Fig. 9, when the reference voltage of the bottom plate is switched from [V_{cm}, V_{cm}, Gnd, Gnd] to [V_{cm}, V_{cm}, V_{cm}, Gnd], the switching energy of the ideal case is

$$E_{\text{ideal}} = 2CV_{\text{cm}} \times \left(0 - \frac{1}{8}V_{\text{ref}}\right) + CV_{\text{cm}} \times \left(V_{\text{cm}} - \frac{1}{8}V_{\text{ref}}\right) = \frac{1}{4}CV_{\text{cm}}^2. \tag{10}$$

Due to the existence of parasitic capacitance, the switching energy can be rewritten as:

$$E_{\text{real}} = 2CV_{\text{cm}} \times (V_{\text{A}} - V_{\text{B}}) + CV_{\text{cm}} \times [V_{\text{cm}} + (V_{\text{A}} - V_{\text{B}})] + C_{\text{pb}}V_{\text{cm}}^2 \tag{11}$$

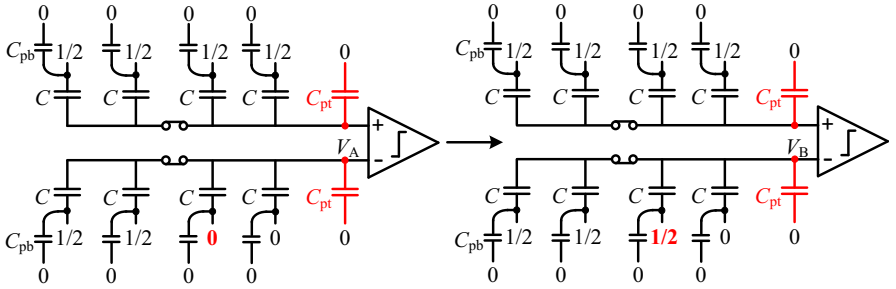

Fig. 9 Analysis of parasitic capacitance

$$V_B = V_A + \frac{C}{4C + C_{pt}} \times V_{cm}. \tag{12}$$

By substituting (12) into (11), Eq. (11) can be calculated as:

$$E_{real} = \frac{C^2 V_{cm}^2}{4C + C_{pt}} + \frac{C}{4C + C_{pt}} C_{pt} V_{cm}^2 + C_{pb} V_{cm}^2 \tag{13}$$

where C, C_{pt}, and C_{pb} represent the unit capacitor, the top plate parasitic capacitance, and the bottom plate parasitic capacitance of the corresponding weight capacitor.

By comparing (10) and (13), it can be concluded that the switching energy is affected by the parasitic capacitance. The top plate parasitic capacitance reduces the switching energy in the down transition, while it increases the switching energy in the up transition. Besides, the bottom plate parasitic capacitance also consumes energy during charging. When the parasitic capacitance is considered, the energy of the proposed switching scheme and previous switching schemes is simulated in Fig. 10 with the assumption that $C_{pt} = 10\%C_{tot}$ (C_{tot} is the total capacitance) and $C_{pb} = 15\%C$. The average switching energy of the proposed switching scheme is only $15.11CV^2_{ref}$, which achieves a 99.10 and a 93.29% energy reduction over the conventional method and monotonic method, respectively. From Table 1, the proposed switching scheme has the highest energy efficiency and area reduction. Moreover, the increasing switching energy is the lowest ($4.57CV_{ref}^2$) when parasitic capacitance is considered except for the monotonic switching scheme [9].

3.5 Parasitic Capacitance Effect on Gain Error

When the bottom plate voltage is switched from Gnd to V_{cm} in Fig. 9, the top plate voltage change of the capacitive DAC array is

$$V_B - V_A = \frac{(V_{cm} - 0)C}{4C + C_{pt}} = \frac{V_{cm}C}{4C} \times \frac{4C}{4C + C_{pt}}. \tag{14}$$

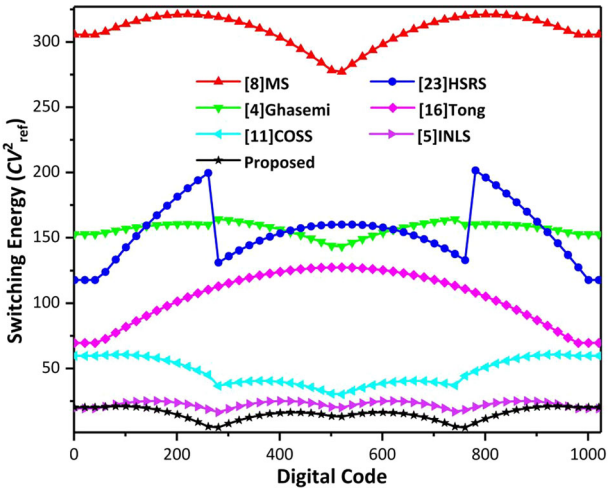

Fig. 10 Switching energy (including reset energy) versus output code for 10-bit SAR ADC with parasitic capacitance

Table 1 Comparison with previous schemes for 10-bit SAR ADC

	Average switching energy (CV_{ref}^2)[a]	Energy saving (%)	Average switching energy (CV_{ref}^2)[b]	Energy saving (%)	Area reduction (%)	Reset energy (CV_{ref}^2)
Conventional	1363.33	Ref	1681.12	Ref	Ref	0
Monotonic [9]	255.42	81.26	225.19	86.61	50	0
Ghasemi [4]	15.86	98.84	28.85	98.28	75	127.75
Tong [15]	15.86	98.84	21.32	98.73	75	31.88
Tong [16]	85.04	93.76	104.52	93.78	75	0
COSS [11]	26.54	98.05	47.68	97.16	75	0
MS [8]	42.40	96.89	53.57	96.81	50	255.51
INLS [5]	15.87	98.83	22.29	98.67	75	0
HSRS [23]	106.11	92.22	155.38	90.76	50	0
Proposed method	10.54	99.23	15.11	99.10	75	0

[a] $C_{pt} = C_{pb} = 0\%$
[b] $C_{pt} = 0.1C_{tot}$, $C_{pb} = 0.15C$

Therefore, the gain error is obtained as:

$$\text{Gain} = \frac{4C}{4C + C_{pt}}. \tag{15}$$

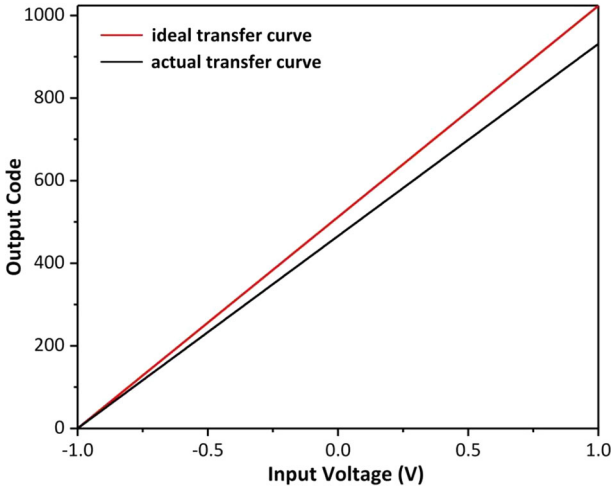

Fig. 11 10-bit SAR ADC transfer curve

Assuming that the ratio of parasitic capacitance to total capacitance is $\beta = 0.1$, the parasitic capacitance can be got as:

$$C_{\mathrm{pt}} = 4C\beta. \tag{16}$$

Therefore, the gain error can be expressed as:

$$\mathrm{Gain} = \frac{1}{1+\beta} = 0.91. \tag{17}$$

Figure 11 shows that parasitic capacitance only causes the gain error, which doesn't affect the linearity.

3.6 Linearity

It is unfair that some switching schemes ignore the linearity requirement in pursuit of low power. To improve energy efficiency and speed, the unit capacitance is expected to be as small as possible. However, the mismatch and the sampling noise limit the unit capacitance size. Therefore, the selection of the unit capacitance should trade off the switching energy, speed, linearity, and sampling noise. Ideally, the capacitors in each capacitive DAC array are binary weighted with $C_i = 2^i C$, $i = 0, 1 \ldots N\text{-}4$.

To analyze the linearity of the proposed switching scheme, we assume that the capacitor mismatch obeys Gaussian distribution with the normal variance $\sigma^2{}_0$, where σ_0 represents the standard deviation of the unit capacitor. The variation of error related to capacitor C_i can be expressed as $2^i\sigma^2{}_0$.

The generation of the MSB bit and sub-MSB bit is not affected by the capacitor mismatch. Thus, the worst case of INL and DNL occurs at $1/8V_{\mathrm{ref}}$, $3/8V_{\mathrm{ref}}$,

$5/8V_{\mathrm{ref}}$, and $7/8V_{\mathrm{ref}}$, which means that the code transition happens at [00011…11] to [00100…00], [01011…11] to [01100…00], [10011…11] to [10100…00], and [11011…11] to [11100…00]. For a specific digital code, the analog output of DAC is:

$$V_{\mathrm{DAC}}(x) = \frac{\sum_{i=1}^{N-3}\left(2^{i-1}C+\delta_i\right)b_i + \sum_{i=1}^{N-3}\left(2^{i-1}C+\delta_{i,\mathrm{split}}\right)b_{i,\mathrm{split}} + (C+\delta_0)b_0 + \left(C+\delta_{i,0}\right)b_{0,\mathrm{split}}}{C_{\mathrm{tot}}} \tag{18}$$

where b_i, $b_{i,\mathrm{split}}$, b_0, $b_{0,\mathrm{split}}$ are composed of Gnd, V_{ref}, and V_{cm}. By neglecting the mismatch of the total capacitance, we can get the following results:

$$C_{\mathrm{tot}} = 2^{N-2}C \tag{19}$$

$$\mathrm{LSB} = \frac{V_{\mathrm{ref}}}{2^N} \tag{20}$$

$$\mathrm{INL} = V_{\mathrm{DAC,real}}(x) - V_{\mathrm{DAC,ideal}}(x) \tag{21}$$

$$\mathrm{INL}(x) = \frac{\sum_{i=1}^{N-3}\delta_i b_i + \sum_{i=1}^{N-3}\delta_{i,\mathrm{split}}b_{i,\mathrm{split}} + \delta_0 b_0 + \delta_{i,0}b_{0,\mathrm{split}}}{2^{N-2}C}V_{\mathrm{ref}} \tag{22}$$

$$\sigma^2_{\mathrm{INL}}(x) = \frac{\sum_{i=1}^{N-3}(\delta_i b_i)^2 + \sum_{i=1}^{N-3}\left(\delta_{i,\mathrm{split}}b_{i,\mathrm{split}}\right)^2 + (\delta_0 b_0)^2 + \left(\delta_{i,0}b_{0,\mathrm{split}}\right)^2}{2^{2N-4}C^2}V^2_{\mathrm{ref}} \tag{23}$$

$$\sigma^2_{\mathrm{INL,MAX}}(x) = \frac{2^{N-1}\sigma_0^2}{C^2}\mathrm{LSB}^2 \tag{24}$$

$$\mathrm{DNL} = \mathrm{INL}(x) - \mathrm{INL}(x-1) \tag{25}$$

$$\mathrm{DNL}(x) = \frac{\sum_{i=1}^{N-3}\delta_i \Delta b_i + \sum_{i=1}^{N-3}\delta_{i,\mathrm{split}}\Delta b_{i,\mathrm{split}} + \delta_0 \Delta b_0 + \delta_{i,0}\Delta b_{0,\mathrm{split}}}{2^{N-2}C}V_{\mathrm{ref}} \tag{26}$$

$$\sigma^2_{\mathrm{DNL}}(x) = \frac{\sum_{i=1}^{N-3}(\delta_i \Delta b_i)^2 + \sum_{i=1}^{N-3}\left(\delta_{i,\mathrm{split}}\Delta b_{i,\mathrm{split}}\right)^2 + (\delta_0 \Delta b_0)^2 + \left(\delta_{i,0}\Delta b_{0,\mathrm{split}}\right)^2}{2^{2N-4}C^2}V^2_{\mathrm{ref}} \tag{27}$$

$$\sigma^2_{\mathrm{DNL,MAX}}(x) = \frac{2^{N-1}\sigma_0^2}{C^2}\mathrm{LSB}^2. \tag{28}$$

The linearity of the monotonic switching scheme can be analyzed with the above method. The RMS INL and RMS DNL can be calculated as follows:

$$\sigma^2_{\mathrm{INL,MAX\_\ monotonic}} = \frac{2^N \sigma_0^2}{C^2}\mathrm{LSB}^2 \tag{29}$$

$$\sigma^2_{\mathrm{DNL,MAX\_\ monotonic}} = \frac{2^N \sigma_0^2}{C^2}\mathrm{LSB}^2. \tag{30}$$

Figure 12 presents the 500-run Monte Carlo simulation results of the proposed switching scheme and the monotonic switching scheme with unit capacitor mismatch of $\sigma_0/C = 1\%$. The RMS DNL and the RMS INL of the proposed switching scheme are only 0.152 LSB and 0.161 LSB, respectively. Therefore, the linearity is enhanced by $\sqrt{2}\times$ over the monotonic switching scheme, which can match theoretical analysis. Table 2 compares the linearity of the proposed switching scheme with the other switching schemes. It can be concluded that the proposed switching scheme has the best linearity.

To meet the linearity requirement of N-bit ADC, according to the three-sigma law of normal distribution, there is

$$3\sigma_{\mathrm{DNL,MAX}} < \frac{1}{2}\mathrm{LSB}. \tag{31}$$

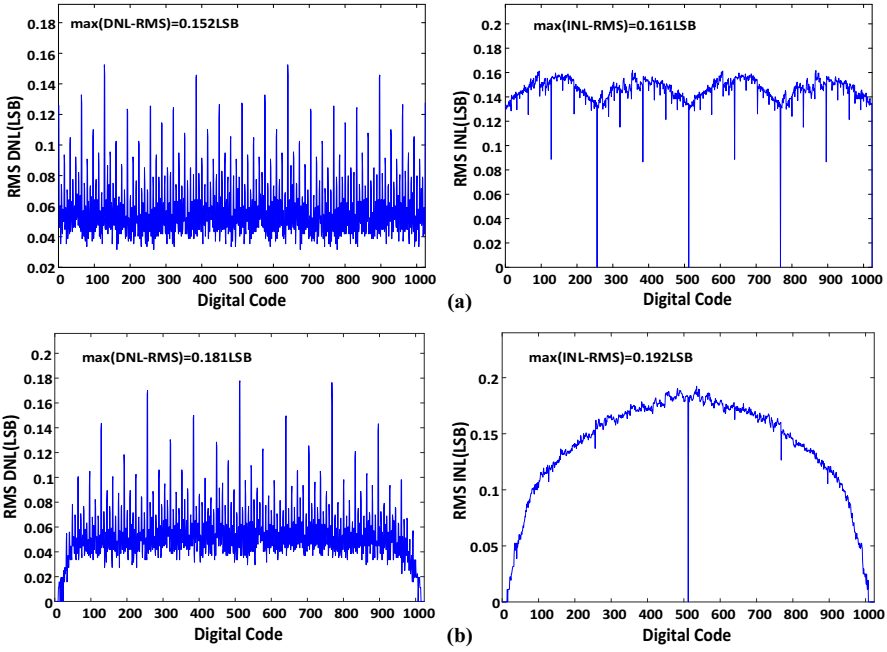

Fig. 12 (**a**) DNL and INL versus output code of the proposed switching scheme and (**b**) DNL and INL versus output code of the monotonic scheme

Table 2 Linearity comparison for 10-bit SAR ADC with $\sigma_0/C = 1\%$

Switching scheme	DNL(LSB)	INL(LSB)
Monotonic [9]	0.181	0.192
Ghasemi [4]	0.17	0.18
Two-step [3]	0.234	0.281
Tri-level [22]	0.165	0.168
Proposed method	0.152	0.161

Combining (28) with (31), we can obtain

$$\frac{\sigma_0}{C} < \frac{1}{6\sqrt{2^{N-1}}}. \tag{32}$$

The capacitor mismatch model is

$$\sigma\left(\frac{\Delta C}{C}\right) = \frac{K_\sigma}{\sqrt{\mathrm{A}}} \tag{33}$$

where $C = K_\mathrm{C} \times \mathrm{A}$, $\sigma(\Delta C/C)$, A, K_σ, and K_C stand for the standard deviation of the capacitor mismatch, the capacitor area, the matching coefficient, and the capacitance density parameter. There is

$$\frac{\sigma_0}{C} = \frac{1}{\sqrt{2}}\sigma\left(\frac{\Delta C}{C}\right). \tag{34}$$

According to (32), (33), and (34), the unit capacitance can be expressed as

$$C = 18K_\sigma^2 K_\mathrm{C} 2^{N-1}. \tag{35}$$

Besides the capacitor mismatch, the capacitance should also be designed to satisfy the sampling noise, which is generally smaller than the quantization noise (e_{rms}^2). The quantization noise power can be expressed as

$$e_{\mathrm{rms}}^2 = \frac{\Delta^2}{12} \tag{36}$$

where $\Delta = V_{\mathrm{ref}}/2^N$, V_{ref} represents the peak-to-peak voltage swing of the input signal.

The relationship between the sampling noise and the quantization noise can be expressed as

$$\frac{kT}{C} \le e_{\mathrm{rms}}^2 \tag{37}$$

where k is the Boltzmann constant, T is the Kelvin temperature.

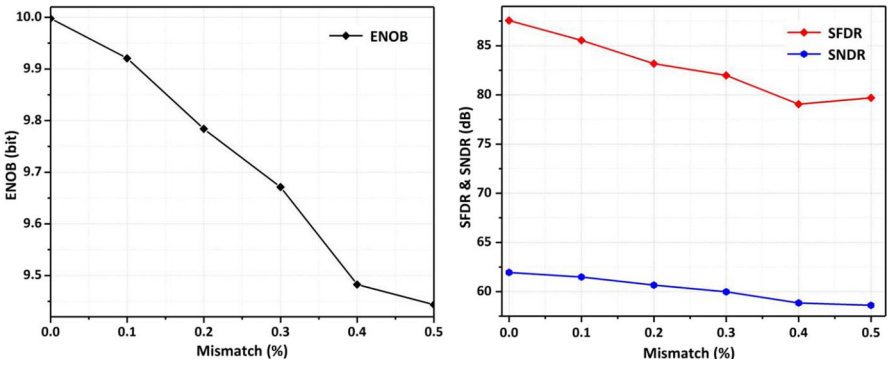

Fig. 13 The effect of V_{cm} mismatch on dynamic performance

Through (36) and (37), the unit capacitance can be obtained.

$$C = 12kT\left(\frac{2^N}{V_{\mathrm{ref}}}\right)^2. \tag{38}$$

The unit capacitance can be calculated as 5.21 fF with the sampling noise requirement, while it is 17.44 fF for the linearity requirement. Thus, the unit capacitance is selected as 17.44 fF in our design for 10-bit SAR ADC.

3.7 Sensitive to the V_{cm} Variation

The dynamic performance of the ADC is affected by the accuracy of the reference voltage V_{cm}. To illustrate the impact of the reference voltage accuracy on the dynamic performance, Fig. 13 shows the FFT analysis after the 500-run Monte Carlo simulation of 10-bit SAR ADC with a V_{cm} mismatch range of 0–0.5%. Figure 13 illustrates that dynamic performance decreases as the V_{cm} mismatch increases. When the V_{cm} mismatch is 0.5%, the SFDR and SNDR are reduced by 7.87 and 3.34 dB, respectively. Fortunately, in the ADC measurement process, the reference voltage can be regulated by the off-chip low-dropout regulator (LDO).

3.8 Logical Complexity and Non-Ideal Factors

In the conversion process, except for the first three conversions, the other conversions adopt the monotonic switching scheme, and only the bottom plate voltage of one capacitor is changed in each conversion. Therefore, logical complexity is acceptable.

The connection switches S_{p2} and S_{n2} can bring non-ideal factors such as charge injection, clock feed-through, and clock jitter, which can deteriorate the total harmonic distortion (THD) and SNDR. The differential structure can suppress the non-ideal factors significantly [3, 21].

4 Simulation Results

4.1 MATLAB Simulation Results

To verify the influence of different noise sources and non-ideal factors, a 10-bit SAR ADC model is established in MATLAB. There are almost no spurs and harmonics in the ideal model from Fig. 14a. Hence, the SFDR has a high value while the SNDR is limited to 61.95 dB due to the intrinsic quantization noise. The SFDR is affected by spurs and harmonics, and the SNDR is affected by noise and harmonics. Compared to Fig. 14a, the SFDR remains nearly unchanged and the SNDR is decreased to 61.92 dB in Fig. 14b and 61.19 dB in Fig. 14c. When the capacitor mismatch (1%), V_{cm} mismatch (0.1%), and V_{ref} mismatch (0.1%) are added to the ideal model further, the SFDR and SNDR are decreased to 78.46 and 60.65 dB, respectively.

Figure 15 also shows the SFDR and SNDR with different input signal frequencies at the sampling rate of 1 MS/s from the 500-run Monte Carlo simulation. Figure 15a, b, and c shows the ideal model, the model with kT/C noise, the model with kT/C and comparator noise, the SNDR is decreased because the kT/C and the comparator noise

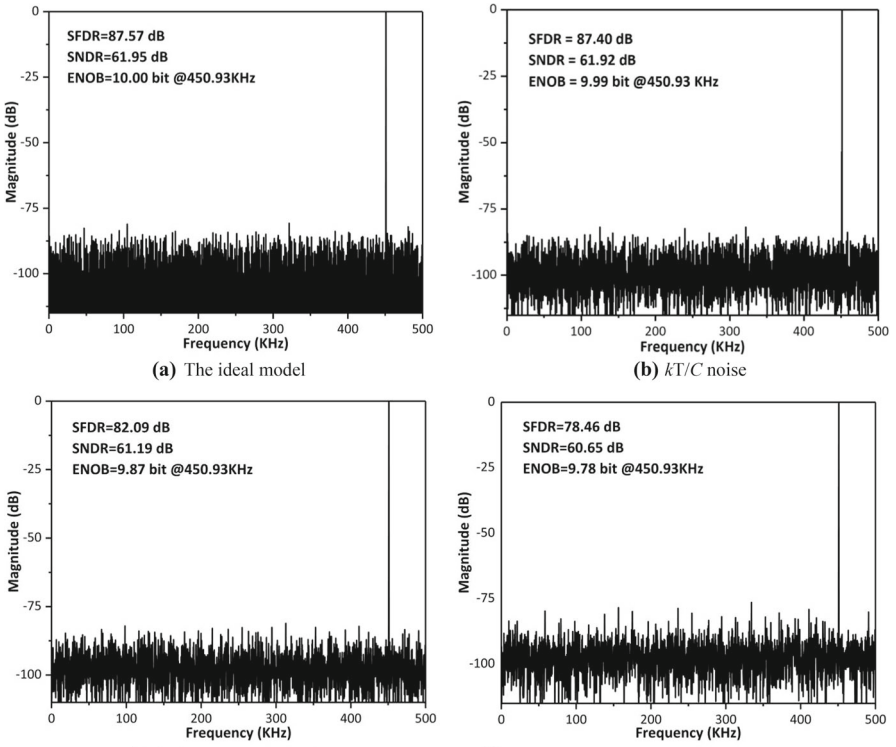

Fig. 14 FFT spectrum at the sampling rate of 1 MS/s

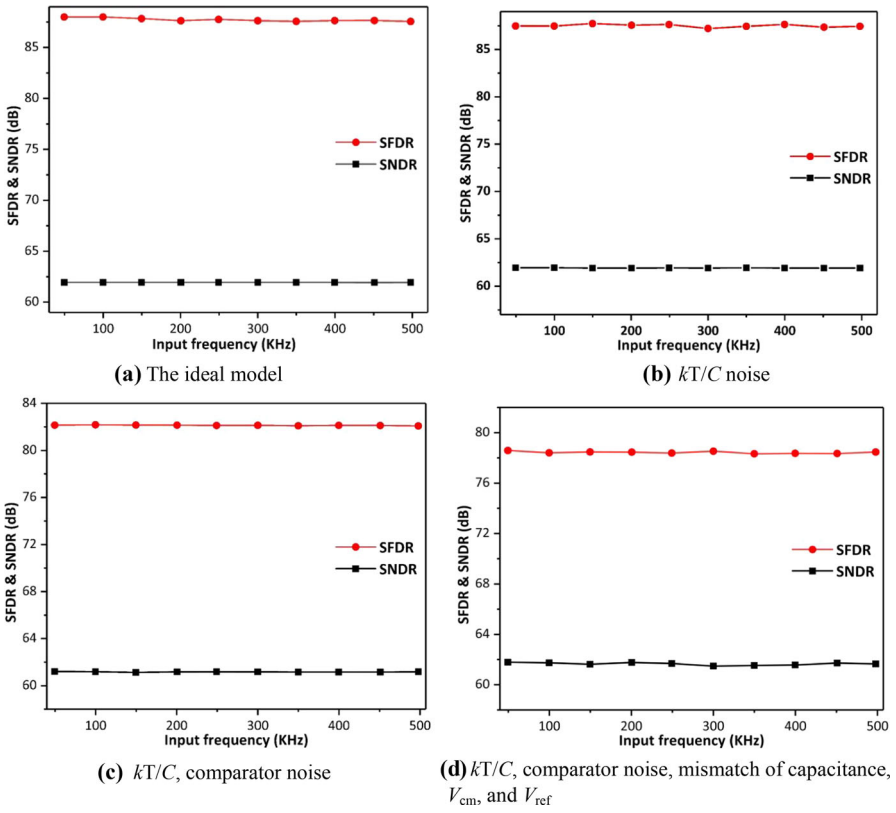

Fig. 15 SNDR and SFDR versus input frequency at the sampling rate of 1 MS/s

raise the noise floor. The SFDR is almost unchanged in Fig. 15a and b. Furthermore, the SFDR in Fig. 15c is significantly decreased because common-mode voltage variation brings in harmonics. In addition, the SFDR and SNDR are further decreased in Fig. 15d because of the distortions caused by the reference voltage mismatch and the capacitor mismatch. The results are also consistent with Fig. 14.

4.2 Post-simulation Results

The SAR ADC with the proposed switching scheme is designed in a 180-nm CMOS process at a 1 V supply. Figure 16 shows the SAR ADC layout, which occupies an active area of 0.057 mm^2. The custom unit metal–oxide–metal (MOM) capacitor is 17.46 fF from the parasitic extraction and the single-side total capacitor is 4.47 pF. Figure 17 shows the power consumption of each block for the proposed SAR ADC. The total power is 15.25 μW, where the power of the S/H circuit, the comparator, the DAC array, and the digital circuit is 0.31, 2.35, 6.05, and 6.54 μW, respectively. Figure 18 shows the relationship between sampling rate and power consumption. It can be concluded that power consumption has a nearly linear relationship with the sampling rate.

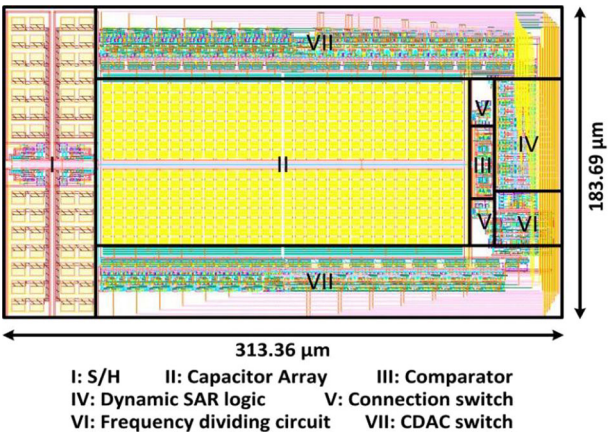

Fig. 16 Layout of the proposed SAR ADC

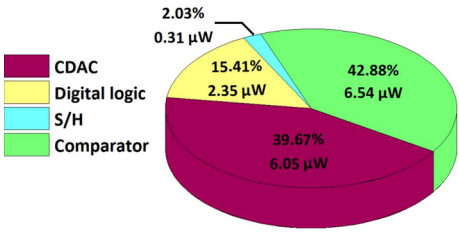

Fig. 17 Breakdown of power consumption for each block

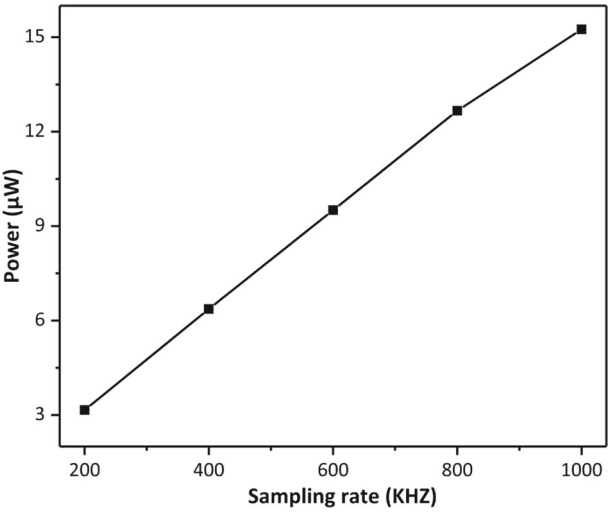

Fig. 18 Power versus sampling rate

The post-simulation results show that the comparator dynamic offset due to common-mode voltage variation and the capacitor mismatch affects the linearity. The SFDR, SNDR, and ENOB are 68.63, 57.81 dB, and 9.31 bit at the Nyquist input frequency in Fig. 19, respectively. Figure 20 presents the variation of the SNDR and SFDR with different input signal frequencies at the sampling rate of 1 MS/s. When the input signal frequency varies from low frequency to the Nyquist frequency, the SFDR is over 68.63 dB, and the SNDR is over 57.81 dB, which means that the ENOB is over 9.31 bit.

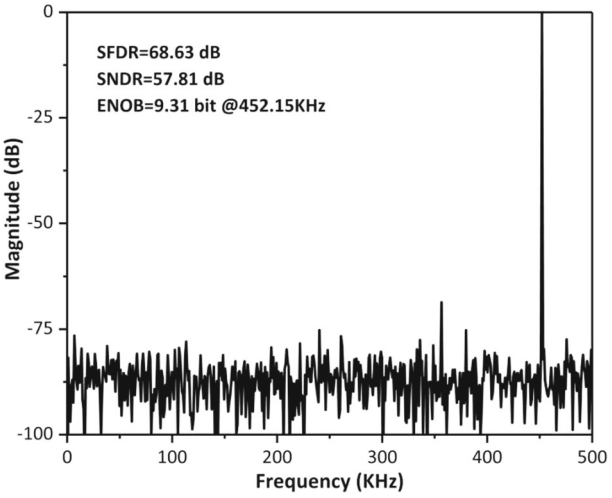

Fig. 19 FFT spectrum at the sampling rate of 1 MS/s

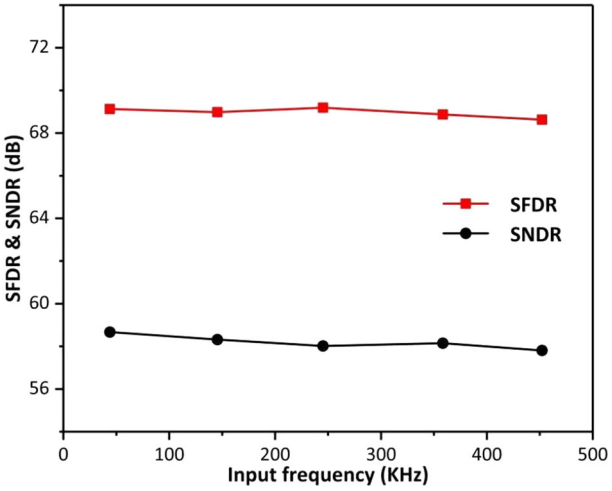

Fig. 20 SNDR and SFDR versus input frequency at the sampling rate of 1 MS/s

Table 3 Comparison with previous works

Specification	[4]* MEJ	[16]+ CSSP	[13]+ JSSC	[12]+ TCAS-I	[6]+ CSSP	This work*
Year	2017	2019	2020	2020	2021	**2022**
Technology (nm)	180	180	40	130	40	**180**
Resolution (bit)	10	10	10	10	10	**10**
Supply (V)	1.8	1	1.2	0.8	1.1	**1**
Active area (mm^2)	0.194	0.124	0.023	0.2	0.139	**0.057**
f_s (MS/s)	1	0.12	120	14	80	**1**
Power(μW)	35.3	2.97	1120	175.8	990	**15.25**
SFDR (dB)	79.8	67.4	76.1	69.2	69.5	**68.63**
SNDR (dB)	61	58.26	54.9	54.3	50.7	**57.81**
ENOB (bit)	9.84	9.39	8.83	8.72	8.13	**9.31**
FoM (fJ/conv.-step)	38.52	36.89	20.51	29.76	44.17	**24.03**

Bold values indicate key performance of our work
*Simulation +Measured

Table 3 summarizes the proposed SAR ADC performances and compares key metrics with several previous works. The FoM is defined as below [16]:

$$\text{FoM} = \frac{\text{Power}}{f_s \times 2^{\text{ENOB}}} \tag{39}$$

where f_s is the sampling rate, and ENOB is the effective number of bits at the Nyquist input frequency. The proposed SAR ADC achieves an FoM of 24.03 fJ/conv.-step. It can be concluded that the proposed SAR ADC has a small active area and a competitive FoM.

5 Conclusion

The SAR ADC with the proposed switching scheme has been designed in a 180-nm CMOS process. Taking advantage of the tri-level scheme, the capacitor area is reduced by 75% compared to the conventional switching scheme. By combining the MSB splitting and monotonic switching schemes, linearity and energy efficiency are enhanced. Moreover, the connection switch between the MSB splitting capacitors and LSB capacitors avoids the reset energy. The average switching energy is $10.54CV^2_{\text{ref}}$, which achieves a 99.23% reduction over the conventional switching scheme. The RMS DNL and RMS INL are only 0.152 LSB and 0.161 LSB, respectively. The post-simulation results show that the power consumption of the proposed SAR ADC is 15.25 μW, and the active area is 0.057 mm^2 at the sampling rate of 1 MS/s. The SAR ADC with the proposed switching scheme can realize an SNDR of 57.81 dB and

an FoM of 24.03 fJ/conv.-step at near Nyquist frequency, which is very suitable for low-power applications.

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Data availability Date sharing is not applicable to this article as no datasets were generated or analyzed during the current study.

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