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A Compact Low-Loss 6-bit DMTL Phase Shifter Using a Novel Three-State Unit Cell

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Abstract

In this paper, a novel small-size, low-loss 6-bit MEMS phase shifter is designed, analyzed, and simulated. The proposed structure includes 17 unit cells, and each unit cell can generate three different phase shifts (i.e., 5.625-, 11.25-, and 22.5-degree phase shifts). The designed unit cell consists of a coplanar waveguide transmission line, a MEMS, and two-pair metal–air–metal bridges. The bridge capacitors are electrically in series and are actuated in three different modes. In each mode, the distributed capacitance of the transmission line and the phase velocity are changed to achieve a phase shift. As the novelty of this design, the number of unit cells is reduced from 64 (which is the case in a conventional 6-bit phase shifter) to only 17. Therefore, the total length of the 6-bit phase shifter is considerably reduced. The designed structure is simulated using Ansoft HFSS and IntelliSuite. Based on the simulation results, the lateral size of the phase shifter is only 8.5 mm; the root-mean-square (RMS) phase error is 1.35, and the average loss is 1.2 dB. A step-by-step fabrication process is also proposed for designing the DMTL phase shifter. The designed phase shifter can be easily scaled to other frequencies for radar and satellite applications that require more bits.

Keywords Phase shifter · RF MEMS · Unit cell · Insertion loss · Return loss

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1 Introduction

Microelectromechanical systems (MEMS) technology is used in micron and submicron devices that use standard integrated circuit fabrication processes, such as photolithography, etching, and bonding. This technology makes it possible to fabricate small-size devices with high functionality, precision, and performance. Based on these properties, MEMS devices and systems are found in many applications such as automobiles, aerospace, medicine, and telecommunication. Radiofrequency (RF) MEMS is one of the critical areas which deals with communication devices and systems. Low-loss performance at high frequencies (up to 100 GHz), high isolation capability, low DC power consumption, and high linearity are the main advantages of RF MEMS devices and systems. These features make RF MEMS devices suitable for special applications such as radar, phased array antennas, satellite communication, and military systems. The main challenge of the RF MEMS devices is their large size [25].

RF MEMS phase shifters are the main component of phased array systems and a key element for modern radar and communication systems. Phase shifters are generally classified into two main groups: analog and digital. Analog phase shifters use either semiconductor varactors [21] or MEMS counterparts [26] and can continuously change the phase from 0° to 360°. Digital phase shifters use either FET or MMIC switches [19, 20] or MEMS switches [22] which provide a discrete set of phase shifts. However, due to the limited control on bridge height before the bridge snap, analog phase shifters have relatively small phase shifts. Digital MEMS phase shifters have resolved this problem. Hence, based on their large phase shift capability and simple operation, digital MEMS phase shifters have been investigated in many research papers. MEMS phase shifters are generally designed and fabricated in four basic types, i.e., reflected type [12, 23, 29], switched line [11, 24], loaded line [18, 30], and distributed MEMS transmission line (DMTL) [5, 6, 8, 9, 14, 27].

Many studies have focused on DMTL phase shifters because of their simple modeling, very wideband performance, and high-frequency operation. This method is based on the capacitive loading of the transmission line (e.g., by using coplanar waveguide) in a periodical manner using a MEMS switch by controlling the switch height. Hence, the distributed capacitance on the transmission line and the phase velocity are varied so that the desired phase shift is achieved. For the first time, DMTL analog phase shifters were introduced by Barker and Rebeiz in 1998 [4]. Their structure includes a coplanar waveguide (CPW) transmission line and a MEMS bridge located on top of the signal line. The bridge displacement changes the line capacitance, and the desired phase shift can be achieved.

Recently, the low-loss compact size designs of MEMS phase shifters have been the main challenge for designers. To fabricate a compact phase shifter, it is necessary to have a significant phase shift per unit cell, which is only possible by increasing the capacitance ratio of the phase shifter. However, a high capacitance ratio increases the return loss and degrades matching. During the past few years, different methods have been utilized to design small-size low-loss DMTL phase shifters. Employing metal–air–metal (MAM) capacitors [15], space-filling curves technique [7], and glass

substrates instead of high resistive silicon (HRS) counterparts [13] has been a significant effort to reduce the losses of DMTL phase shifters. Using both capacitors and inductors in DMTL phase shifters around the resonance frequency is another way to obtain a significant phase shift per unit cell [1, 2]. A miniature DMTL phase shifter that uses both tunable capacitors and inductors was reported by F. Ling [17]. This phase shifter consists of two series ohmic contact switches, a MEMS shunt switch, and two MAM capacitors. When the cell capacitance under the actuation condition is increased to obtain a significant phase shift, the value of the tunable inductor also increases. This keeps the down impedance matched to the port impedance as the phase is further shifted.

To achieve high accuracy in digital phase shifters, DMTL phase shifters with more bits (e.g., with 5 or 6 bits) are required. However, in more-bit phase shifters, the number of unit cells is dramatically increased. Hence, the large size of this type of phase shifter is their main drawback. A small-size, two-state 6-bit phase shifter is proposed by Afrang et al. [3]. Their structure consists of a standard CPW, a MEMS bridge, two additional electrodes near the centerline under the bridge, and two MAM static capacitors; the phase shifter is only 12.8 mm and includes only 32 phase states. The MEMS bridge is actuated twice to create two states (5.625 and 11.25 degrees) in a unit cell. The configuration of two states in a unit cell can reduce the size and loss simultaneously.

Producing a significant phase shift per unit cell is another technique, which is used to decrease the number of unit cells [10]. In this technique, instead of using identical unit cells, three different types of MEMS switches, which can perform various phase shifts, are used. This structure includes only 29 switches instead of 64 switches in a 6-bit phase shifter.

In this paper, a new design of a three-state compact DMTL phase shifter with low actuation voltage and high reliability is proposed. The design is based on three individual switches in a small-size unit cell, which can produce three-phase states per unit cell and reduce the number of unit cells from 64 to 17.

The structure of the designed phase shifter is identical to that of universal DMTL phase shifters if the MAM bridges are excluded. The only difference is the MAM bridges, which are added to the conventional structure to obtain a three-state phase shift using one unit cell. Therefore, this is one of the innovations of the designed structure in which the one-state unit cell has become a three-state unit cell without adding complexity.

The three-state unit cell in the present study has been implemented more quickly than in Ref. [3]. In [3], implanting a stopper increases the fabrication process steps. One of the innovations of our unit cell is its similarity to one-state conventional DMTL phase shifters, so there is no complexity in this design. The only difference is in the number of bridges and actuation voltage. A three-state unit cell can create a phase shift of 22.5°, enabling us to design a compact 6-bit DMTL phase shifter. A universal one-state DMTL phase shifter consists of one MEMS bridge and two static MAM capacitors. When the MEMS bridge is actuated, the desired phase shift is achieved. In two- and three-state unit cells, a significant phase shift can be obtained by the same unit cell size or small increases in the unit cell size. At a particular operating frequency, a large unit cell is required to achieve a significant phase shift. This leads to the rise

in the Bragg frequency and hence a reduction in the phase shifter linearity. Therefore, there is a trade-off between the Bragg frequency and the phase shift linearity. In an appropriate design, the unit cell size is selected so that the linearity of the phase shifter is maintained. In three-state unit cells with a phase shift of 22.5°, the ratio of the Bragg frequency to the operating frequency is 1.97. This ratio for two-state unit cells is 2.4. Hence, the Bragg frequency is one of the challenges in three-state unit cells.

The remainder of this paper includes four sections: The structure of DMTL is presented in Sect. 2. Section 3 consists of the analysis of the proposed structure. Simulation results and the fabrication process of the proposed phase shifter are presented in Sects. 4 and 5, respectively. Finally, the concluding remarks are given in the last section.

2 DMTL Phase Shifter

2.1 Unit Cell Design

A DMTL phase shifter consists of a CPW T-line and several MEMS switches periodically on top of the signal line. When the switches are actuated, they move downward, and the loading capacitance of the transmission line is changed; therefore, the phase velocity is varied, and a phase shift is achieved. The relationship between phase shift and the loading capacitance in a DMTL phase shifter is expressed in Eq. (1) [25]:

$$\Delta\varphi = \frac{360 \times s \times f \times Z_0 \times \sqrt{\varepsilon_{\text{reff}}}}{c}\left(\frac{1}{Z_d} - \frac{1}{Z_u}\right) \tag{1}$$

where s is the distance between the MEMS bridges, Z_0 is the characteristic impedance of the CPW t-line, f is the operating frequency, and c is the light velocity; Z_d and Z_u are the line impedance in, respectively, down- and up-state of the switches.

When a switch is actuated, the line loading capacitance and the line impedance change (Eq. 2).

$$Z_{\text{load}} = \sqrt{\frac{sL_t}{sC_t + C_{\text{load}}}} \times \sqrt{1 - \left(\frac{f}{f_B}\right)^2} \tag{2}$$

where L_t, C_t, C_{load}, and, f_B are the line inductance per unit length, line capacitance per unit length, loading capacitance, and Bragg frequency, respectively.

The main challenge in digital DMTL phase shifters is their large size, i.e., requiring more unit cells, especially in those with more bits. To realize a compact DMTL phase shifter, either the size or the number of unit cells should be decreased. However, based on Eq. (1), if the unit cell size (s) is reduced, the phase shift decreases; furthermore, for a given phase shift, the number of unit cells increases, and the overall size of the device becomes large. To resolve this problem, we proposed a novel three-state unit cell, which is shown in Fig. 1.

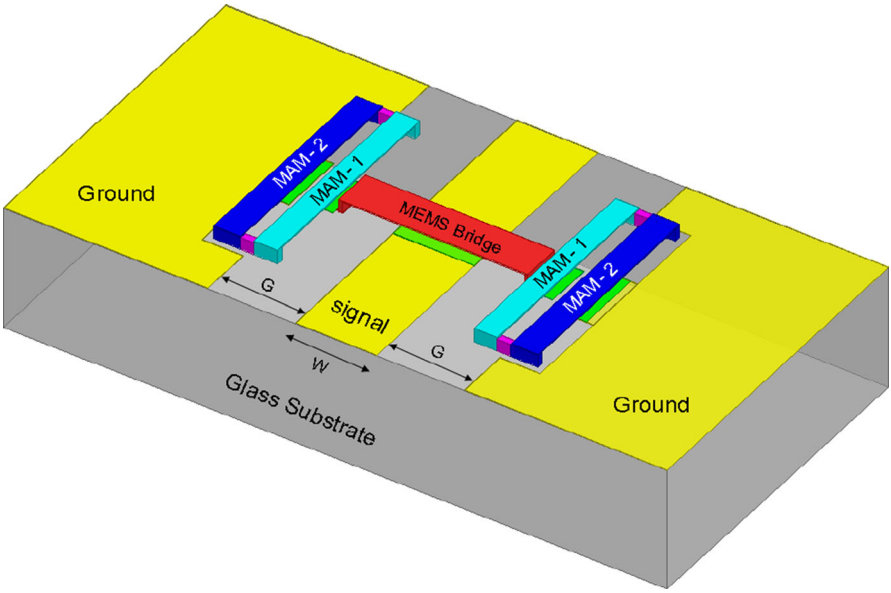

Fig. 1 Proposed unit cell for DMTL phase shifter

According to Fig. 1, the proposed structure includes a CPW T-line, a MEMS bridge on the centerline, and two-pair metal–air–metal (MAM) bridges. One pair of MAM bridges is located on a glass substrate (MAM-2), and another pair is near the ground line (MAM-1). This design employs three different loading capacitances of the transmission line, which produce three other phase states (5.625, 11.25, and 22.5 degrees). This three-state unit cell is used to design a small-size 6-bit DMTL phase shifter. Generally, 64 one-state unit cells are required to realize a 6-bit DMTL phase shifter. In the proposed structure, the number of unit cells needed to implement a 6-bit phase shifter is decreased to 17, so the total length of the phase shifter is considerably reduced (more than 35%). Furthermore, because of using fewer unit cells, the loss of the phase shifter also reduces. Based on our knowledge, the designed 6-bit DMTL phase shifter is the smallest capacitive-type DMTL phase shifter that has been studied so far and is very suitable for phased array antenna applications.

The equivalent circuit of the proposed unit cell is shown in Fig. 2. In this figure, R_t, L_t, and C_t represent the transmission line electrical characteristics; C_b, $C_{MAM\text{-}1}$, and $C_{MAM\text{-}2}$ denote the capacitances of the MEMS bridge, MAM-1, and MAM-2, respectively. These three capacitances are electrically in series and change the line loading capacitance based on the actuation sequence.

2.2 Operating Principle

The three-state unit cell proposed in this study provides three different phase shifts. For a phase shift of 5.625°, the MAM-1 switch is actuated. When the MEMS switch

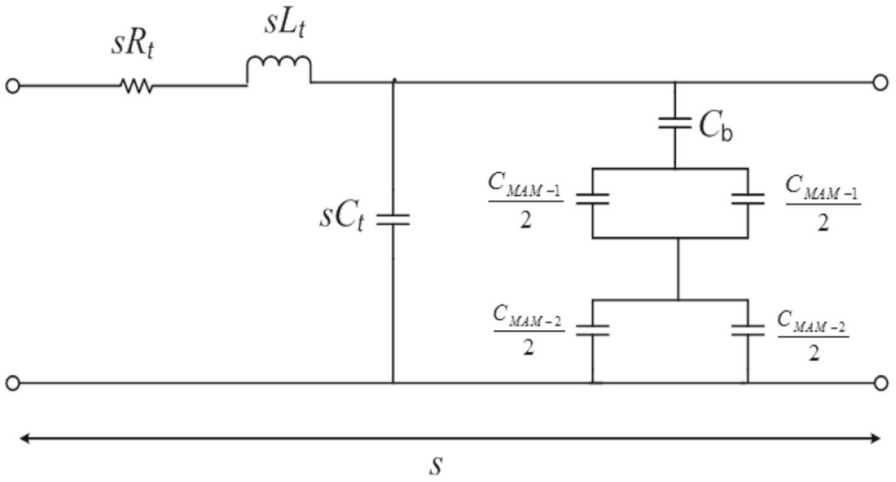

Fig. 2 Equivalent circuit of the proposed unit cell for DMTL phase shifter

is actuated, a phase shift of 11.25° is achieved, and to realize a phase shift of 22.5°, both MEMS and MAM-2 bridges are actuated. Phase shifters with more bits (5- and 6-bit phase shifters) require more switches. Our designed 6-bit phase shifter consists of only 17 unit cells. Unit cells U1 and U17 provide only 5.625° and 11.25° phase shifts, while U2 to U16 create only 11.25° and 22.5° shifts. Hence, the corresponding switches are only actuated to achieve the desired phase shift.

Figure 3 shows the operating principle of the designed unit cell for different phase states.

As shown in Fig. 3a, when the bridges are in the up-states, the phase shifter is in the primary state, called the 0-degree state. In this state, the loading capacitance is C_{up}:

$$C_{up} = \left(\frac{1}{C_b} + \frac{1}{C_{MAM-1}} + \frac{1}{C_{MAM-2}}\right)^{-1} \tag{3}$$

when MAM-1 bridges are actuated, 5.625-degree phase shift is achieved (Fig. 3b). The loading capacitance is the series combination of the two other bridges capacitances (Eq. 4).

$$C_{\text{down1}} = \left(\frac{1}{C_b} + \frac{1}{C_{\text{MAM - 2}}}\right)^{-1} \tag{4}$$

To achieve an 11.25-degree phase shift, only the MEMS bridge is actuated, and the loading capacitance is the series combination of capacitors MAM-1 and MAM-2 (Fig. 3c).

$$C_{\text{down2}} = \left(\frac{1}{C_{\text{MAM}-1}} + \frac{1}{C_{\text{MAM - 2}}}\right)^{-1} \tag{5}$$

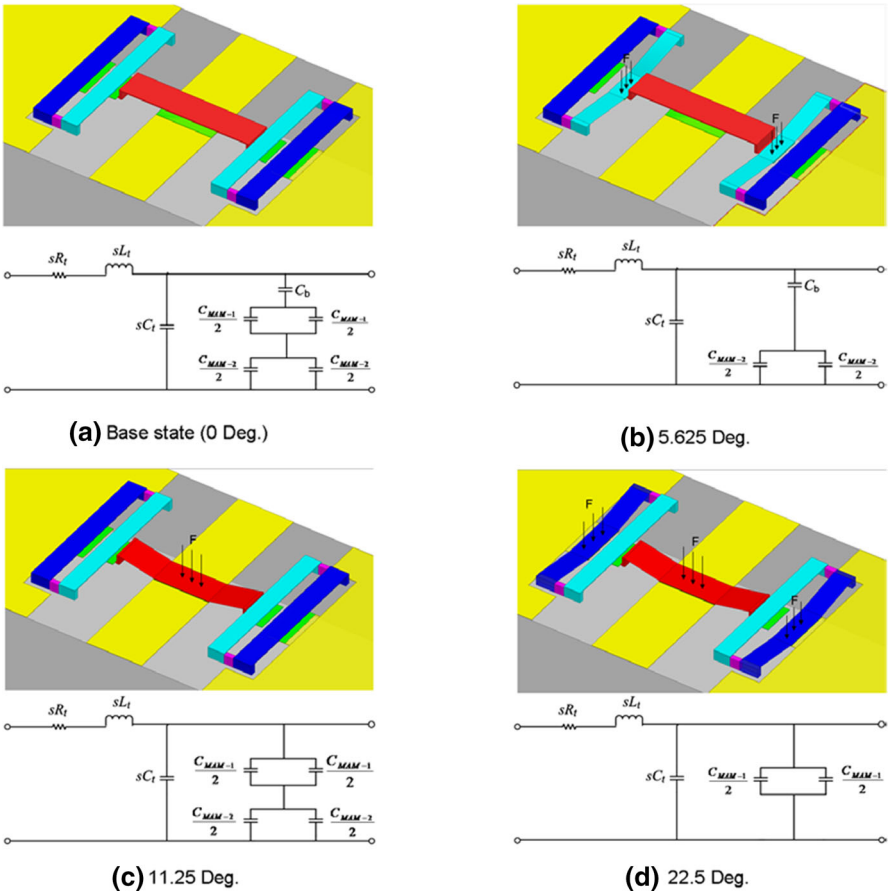

Fig. 3 Operating principle of the proposed DMTL phase shifter. **a** Up-state, **b** 5.625 degrees, **c** 11.25 degrees, and **d** 22.5 degrees

When both MAM-2 and MEMS bridges are actuated, the third state of the designed unit cell is realized, and a 22.5-degree phase shift is obtained (Fig. 3d).

$$C_{\text{down3}} = \left(\frac{1}{C_{\text{MAM}-1}}\right)^{-1} \tag{6}$$

2.3 The Design Process of the Proposed Structure

Generally, in a capacitive-type DMTL phase shifter, when the capacitance of a loaded line increases, the impedance of the transmission line decreases. Hence, the unloaded impedance of the line must be greater than the highest load impedance. Accordingly,

Table 1 Up- and down-state line impedances for different return losses

RL_{max}, dB	Z_u, Ω	Z_d, Ω	$Z_d^{-1} - Z_u^{-1}$, ℧
− 20	55.3	45.2	0.00404
− 18	56.7	44	0.00510
− 15	59.84	41.77	0.00723
− 14	61.2	40.84	0.00814
− 12	64.63	38.68	0.01038
− 10	69.4	36	0.01337

we assume that the designed phase shifter operates in a 50 Ω system. The loaded impedance of the DMTL in this system can be calculated by [23]:

$$Z_{\text{line}} = 50 \times \sqrt{\frac{1 \pm \Gamma_{\text{in}}}{1 \mp \Gamma_{\text{in}}}}, \quad \left(Z_u = 50 \times \sqrt{\frac{1 + \Gamma_{\text{in}}}{1 - \Gamma_{\text{in}}}} \;, \quad Z_d = 50 \times \sqrt{\frac{1 - \Gamma_{\text{in}}}{1 + \Gamma_{\text{in}}}} \right) \tag{7}$$

where Γ_{in} is the input return loss and is defined as:

$$\Gamma_{in} = 10^{\frac{RL_{\max}}{20}} \tag{8}$$

where $RL_{\max}$ denotes the maximum return loss. Table 1 presents the loaded impedances of the up- and down-state positions (Z_u and Z_d) for a given return loss. For an ideal condition, $\Gamma_{\text{in}} = 0$, the system and the loaded transmission line are matched.

To achieve a significant phase shift per unit cell and a low return loss characteristic, we assume $RL_{\max}$ = -14 dB, so the up-state and down-state loading impedances are 61.2 and 40.8 Ω, respectively. According to Table 1, when we choose $RL_{\max} = -$ 14 dB, the largest phase shift corresponds to a unit cell with a significant reflected power loss at the input.

Assuming that the maximum phase shift per unit cell equals 22.5 degrees, the Bragg frequency is 1.97 times the operating frequency based on Eq. (9):

$$\frac{f_B}{f} = \sqrt{\left(\frac{360(Z_u - Z_d)}{\pi \Delta\varphi Z_u} \right)^2 + 1} \simeq \frac{360(Z_u - Z_d)}{\pi \Delta\varphi Z_u} \tag{9}$$

Equation 1 is used to calculate the unit cell size (s), operating frequency (f), and characteristic impedance of the line (Z_0). For a capacitive-type DMTL phase shifter, when the capacitance of a loaded line increases, the impedance of the transmission line decreases. Consequently, the unloaded impedance of the line (Z_0) must be greater than the highest load impedance (Z_u). A glass substrate is selected for this design because of its excellent phase shift/loss property [20]. Assuming $s = 500$ μm and $f =$ 30 GHz, the characteristic impedance (Z_0) is calculated as 99 Ω. Since the proposed unit cell can produce three different phase shifts of 5.625, 11.25, and 22.5 degrees, based on Eq. (1), the loaded impedances of the 5.625° and 11.25° phase shifts are 54 Ω and 49 Ω, respectively.

To determine the capacitance of the loaded line in all states of the proposed unit cell, we consider Eqs. (10)–(14):

$$f_B = \frac{1}{\pi\sqrt{sL_t(sC_t + C_b)}} \tag{10}$$

$$C_u = \frac{\left(Z_0^2 \times x^2 - Z_{up}^2\right)Z_{d3}}{Z_0^2 Z_u^2 \pi\ f_B} \tag{11}$$

$$C_{d1} = \frac{\left(Z_0^2 \times x^2 - Z_{d1}^2\right)Z_{d3}}{Z_0^2 Z_{d1}^2 \pi\ f_B} \tag{12}$$

$$C_{d2} = \frac{\left(Z_0^2 \times x^2 - Z_{d2}^2\right)Z_{d3}}{Z_0^2 Z_{d2}^2 \pi\ f_B} \tag{13}$$

$$C_{d3} = \frac{Z_0^2 \times x^2 - Z_{d3}^2}{Z_0^2 Z_{d3} \pi\ f_B} \tag{14}$$

where $x = \sqrt{1 - \left(\frac{f}{f_B}\right)^2}$; C_u is the capacitance of the loaded line in the up-state position; C_{d1}, C_{d2}, and C_{d3} are the capacitances of the loaded line for 5.625°, 11.25°, and 22.5° phase shifts, respectively. Table 2 shows the results of the loaded line capacitance.

Based on Table 2 and Eqs. (3)–(6), the capacitances of MEMS, MAM-1, and MAM-2 bridges are 56, 88, and 140 fF, respectively (Table 3). Considering Fig. 1 and $Z_0 = 99\ \Omega$, the dimensions of the CPW transmission line are selected at 130/120/130 μm.

Table 2 Calculation results of the loaded capacitance of the proposed unit cell

Phase state	Loaded impedance, Ω	Loaded capacitance, fF
0°	61.2	25
5.625°	54	39
11.25°	49	54
22.5°	40.8	88

Table 3 Calculation results of the bridge capacitances

Bridge	Capacitance (fF)
MEMS	56
MAM-1	88
MAM-2	140

3 Analysis of the Proposed DMTL Phase Shifter

3.1 Frequency Analysis

In this section, the scattering parameters and the phase shift of the designed phase shifter are calculated using MATLAB. For this purpose, the ABCD matrix method is employed. Figure 4 shows the circuit for obtaining the S_{11} of a lossy transmission line. In this figure, Z_{01} is the characteristic impedance of the lossy transmission line and Z_{02} is the matched transmission line impedance. For the matched transmission line, S_{11} can be calculated using ABCD matrix parameters as follows [28]:

$$S_{11} = \frac{A + Y_{02}.B - Z_{02}.C + D}{A + Y_{02}.B + Z_{02}.C + D} \tag{15}$$

The ABCD matrix of a loaded lossy transmission line is calculated as:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh(\gamma.s) & Z_{01}.\sinh(\gamma.s) \\ \frac{1}{Z_{01}}.\sinh(\gamma.s) & \cosh(\gamma.s) \end{bmatrix} \times \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_l} & 1 \end{bmatrix} \tag{16}$$

where Z_l is the loaded impedance, s is the unit cell length, and γ is the complex propagation constant that is expressed as:

$$\gamma = \alpha + j\beta = \frac{sR_t}{2Z_{01}} + j\frac{\omega}{v_p} \tag{17}$$

$$v_p = \frac{s}{\sqrt{sL_t(sC_t + C_b)}} \tag{18}$$

where α is the attenuation constant, β is the propagation constant, Rt is the transmission line resistance per unit length, and vp is the propagation velocity.

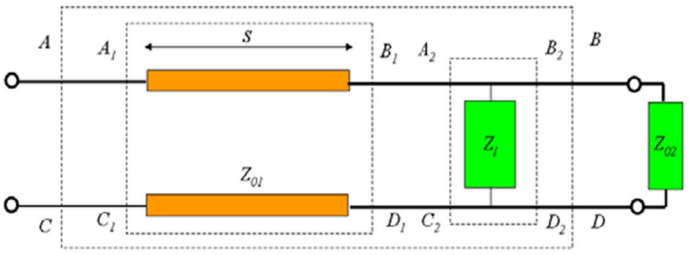

Fig. 4 Circuit model for calculating S_{11}

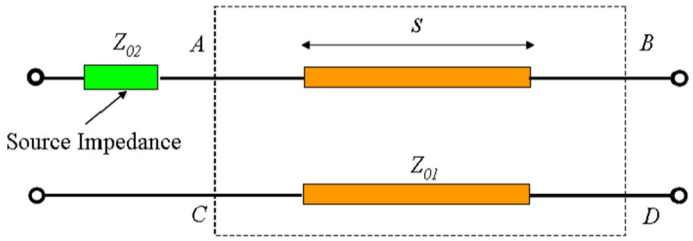

Fig. 5 Circuit model for calculating S_{21}

The inductance per unit length and capacitance per unit length of the CPW transmission line are calculated using Eqs. (19) and (20), respectively; the loaded impedance of the transmission line is calculated from Eq. (21):

$$L_t = \frac{Z_0 \times \sqrt{\varepsilon_{\text{reff}}}}{c} \tag{19}$$

$$C_t = \frac{\sqrt{\varepsilon_{\text{reff}}}}{Z_0\, c} = \frac{L_t}{Z_0^2} \tag{20}$$

$$Z_{01} = Z_l = \sqrt{\frac{sL_t}{sC_t + C_{\text{load}}}} \tag{21}$$

Figure 5 shows a circuit model for calculating S_{21}. To calculate S_{21} from ABCD matrix parameters in Fig. 5, Eq. (22) can be used.

$$S_{21} = \frac{2}{A + Y_{02}.B + Z_{02}.C + D} \tag{22}$$

The phase shift is calculated using the difference between the phase angles of S_{21} in the up- and down-state positions (Eq. 23).

$$\text{Phase Shift} = \text{Phase}\,(S_{21})\big|_{\text{Up - state}} - \text{Phase}\,(S_{21})\big|_{\text{Down - state}} \tag{23}$$

A 6-bit DMTL phase shifter can be implemented using six building blocks, including 5.625°, 11.25°, 22.5°, 45°, 90°, and 180° blocks. The 45°, 90°, and 180° blocks can be realized using 2, 4, and 8 unit cells, respectively. Hence, to implement a 6-bit digital phase shifter, 17 unit cells are required, and the lateral size of the phase shifter is only 8.5 mm.

Figures 6, 7, and 8 illustrate the calculation results of the return loss, insertion loss, and phase shift of the six building blocks of the 6-bit phase shifter.

As shown in Figs. 6 and 7, the calculated insertion loss and return loss of the proposed structure are better than − 10.1 and 0.47 dB, respectively. Moreover, the phase shift is in good agreement with ideal states.

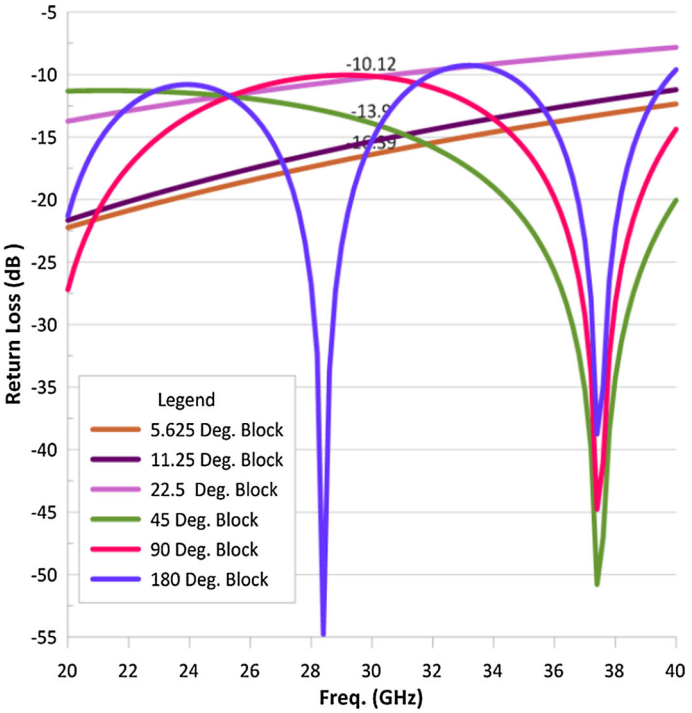

Fig. 6 Calculation results of the return loss of six building blocks of the proposed phase shifter

3.2 Electrostatic Analysis

The actuation voltage of the MEMS and MAM bridges is calculated in this section. Generally, the pull-in voltage of a MEMS switch is presented by Eq. (24):

$$V_{\text{Pull - in}} = \sqrt{\frac{8k}{27\varepsilon_0 A} \cdot {g_0}^3} \tag{24}$$

where k is the spring constant of the structure, A is the overlapping area of the electrodes, g_0 is the gap between the two electrodes, and ε_0 is the air permittivity. The proposed structure includes three fixed–fixed cantilever bridges (Fig. 9) for which the spring constant can be expressed as [25]:

$$k = 32Ew\left(\frac{t}{l}\right)^3 \times \frac{1}{8\left(\frac{x}{l}\right)^3 - 20\left(\frac{x}{l}\right)^2 + 14\left(\frac{x}{l}\right) - 1} \tag{25}$$

where E, w, t, and l are, respectively, Young's modulus, width, thickness, and length of the cantilever beam.

Two factors determine the dimensions of the MEMS and MAM parallel plate capacitors: pull-in voltage and fringing effect. Pull-in voltage is directly proportional to the

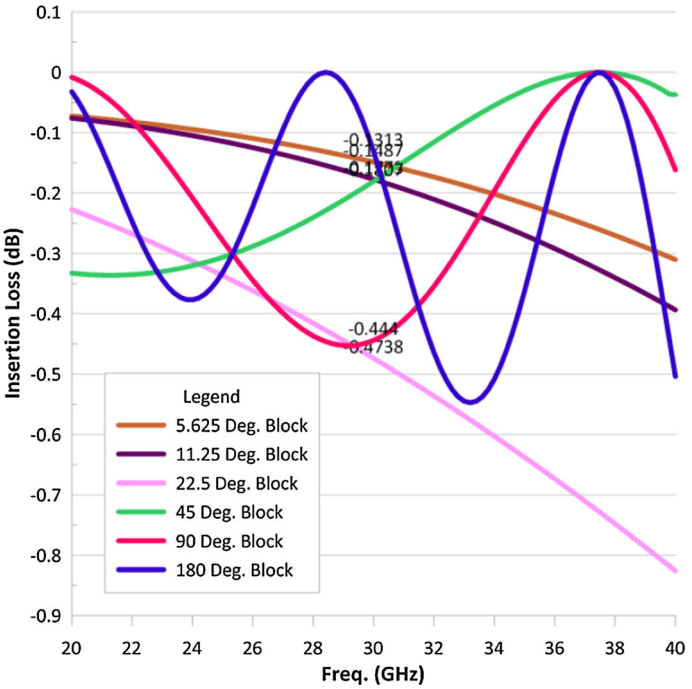

Fig. 7 Calculation results of the insertion loss of six building blocks of the proposed phase shifter

bridge length and width. It is inversely proportional to the bridge thickness, so these parameters are considered in designing MEMS and MAM bridges.

The fringing effect is considered for the bridges in the up-state. The fringing field capacitance of MEMS and MAM capacitors accounts for a substantial portion of the total capacitance. This has a lower impact on bridges that are wider and have a narrower air gap. For a capacitor with a width of 100 μm and an air gap of 4 μm, the fringing capacitance is about 60% of the initial capacitance, while for an air gap of 1.5 μm, this percentage is less than 20% [251]. In our design, the fringing effect is about 10%. The bridges' dimensions are presented in Table 4 and Fig. 10.

Based on Eq. (25) and Table 4, the spring constants of the MEMS, MAM-1, and MAM-2 bridges are 1.964, 0.77, and 1.16 N/m, respectively. Using Eq. (24), the pull-in voltages of these bridges are 3.3, 2.51, and 2.34 V, respectively.

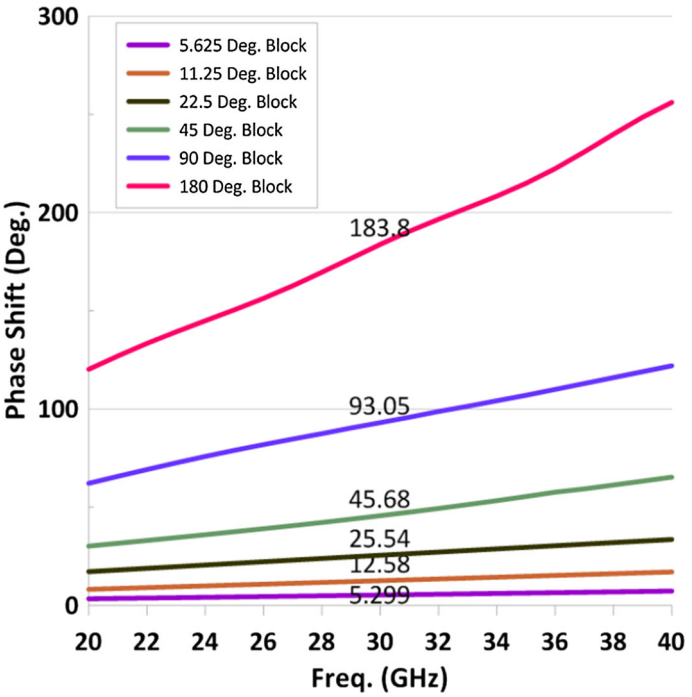

Fig. 8 Calculation results of the phase shift of six building blocks of the proposed phase shifter

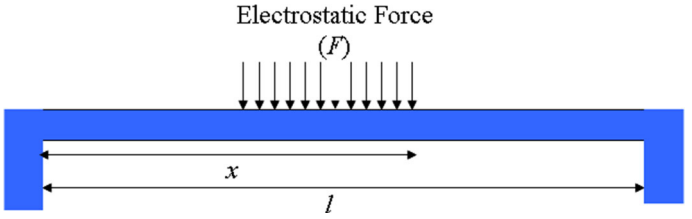

Fig. 9 Fixed–fixed cantilever switch

4 Simulation of the Proposed 6-bit DMTL Phase Shifter

The structure of the proposed DMTL phase shifter is simulated in this section. The scattering parameters, phase shift, and bridges pull-in voltage are calculated in this simulation. To verify the calculations, frequency simulation is carried out using ANSOFT HFSS, and electrostatic simulation is performed using IntelliSuite.

Table 4 Mechanical and electrical properties of MEMS and MAM bridges

Parameter	Symbol	Unit	MEMS bridge	MAM-1 bridge	MAM-2 bridge
Bridge length	L	μm	280	320	320
Bridge width	w	μm	50	35	50
Bridge thickness	t	μm	0.8	0.8	0.8
x distance	x	μm	200	218.5	231
Bridge material	–	–		Gold	
Air gap (μm)	g_0	μm		1	
Dielectric material	–	–		Si_3N_4	
Dielectric thickness (nm)	t_d	nm		100	
Dielectric relative permittivity	ε_r	–		7.1	
Unit cell size (μm)	s	μm		500	
Gold Young's modulus	E	GPa		79	
Gold Poisson patio	υ			0.42	
Gold density (kg/m^3)	ρ	Kg/m^3		19,300	

4.1 Frequency Simulation

Generally, there are two different methods to implement a 6-bit phase shifter: the bit-level and unit-cell-level methods. The bit-level method, also known as the binary-weighted method, is mainly used by designers due to its simplicity in actuating electronic circuits. In this method, six building blocks, i.e., 5.625°, 11.25°, 22.5°, 45°, 90°, and 180°, are connected to form a 6-bit phase shifter. These six building blocks are actuated based on the binary-weighted phase states. Based on the designed three-state unit cell, the 5.625°, 11.25°, and 22.5° blocks can be implemented using three individual unit cells. The 45°, 90°, and 180° blocks consist of 2, 4, and 8 unit cells, respectively (Fig. 11).

Each unit cell in these large phase shift blocks acts in the third state (22.5°). Accordingly, the 6-bit DMTL phase shifter based on the bit-level method consists of only 17 unit cells with an 8.5 mm lateral size, which is considerably small. The return loss, insertion loss, and phase shift simulation results of the six building blocks are shown in Figs. 12 and 13. According to Fig. 12, each of these blocks has good performance. For 64 states of the 6-bit phase shifter, when the blocks with large phase shift unit cells (22.5°, 45°, 90°, and 180°) are actuated to obtain the desired phase shift, the return loss is degraded, and a significant phase shift error occurs. This unwanted problem is the lack of proper impedance matching between the larger block and its side blocks (mainly when the larger block is actuated and its side block is in an un-actuated state). If the three-state unit cell size increases, the impedance matching will be better, and the mentioned problem can be resolved. However, this would contradict the primary goal

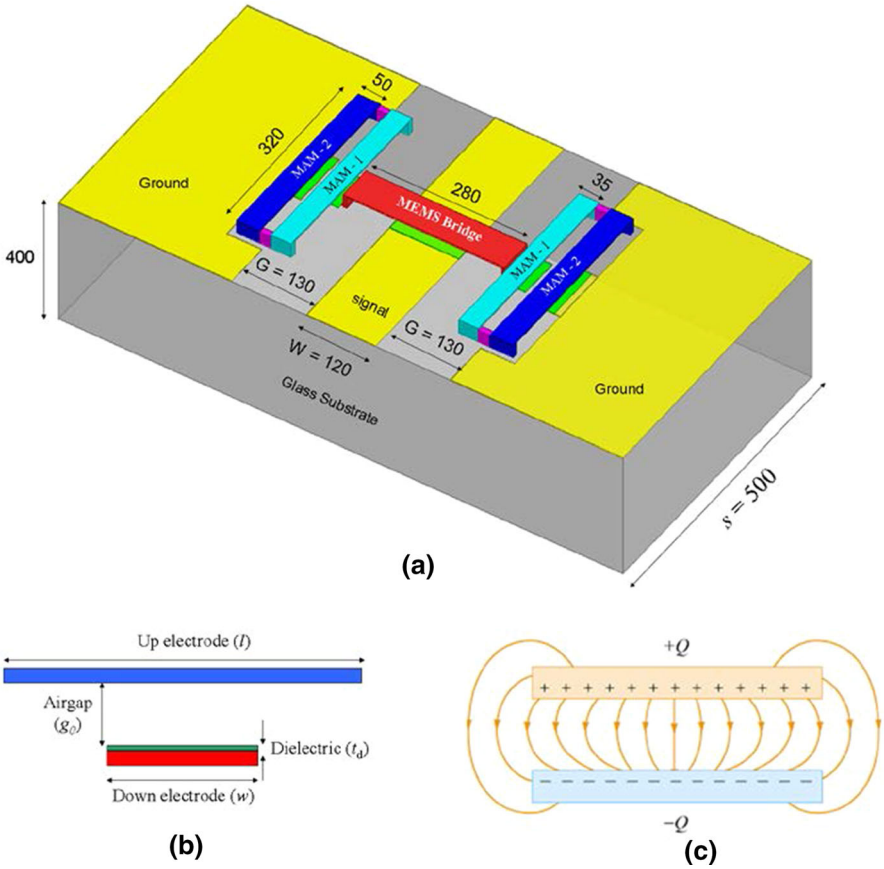

Fig. 10 **a** Dimensions of the proposed three-state unit cell (all sizes are in μm), **b** parallel-plate capacitor, and **c** fringing effect in parallel-plate capacitors

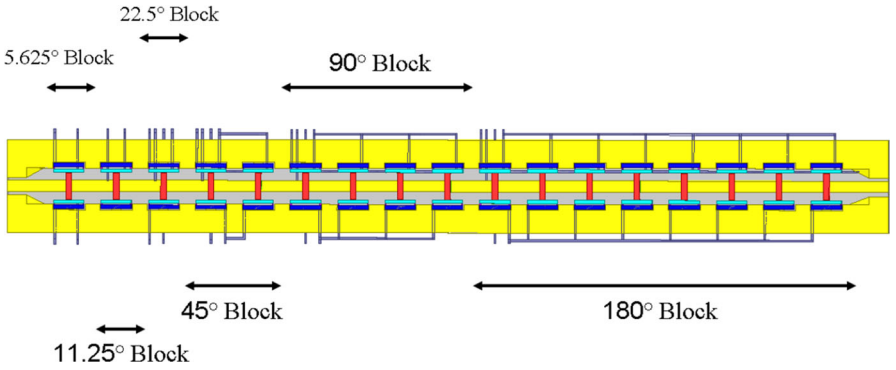

Fig. 11 Bit-level actuation for 6-bit DMTL phase shifter using the proposed three-state unit cell

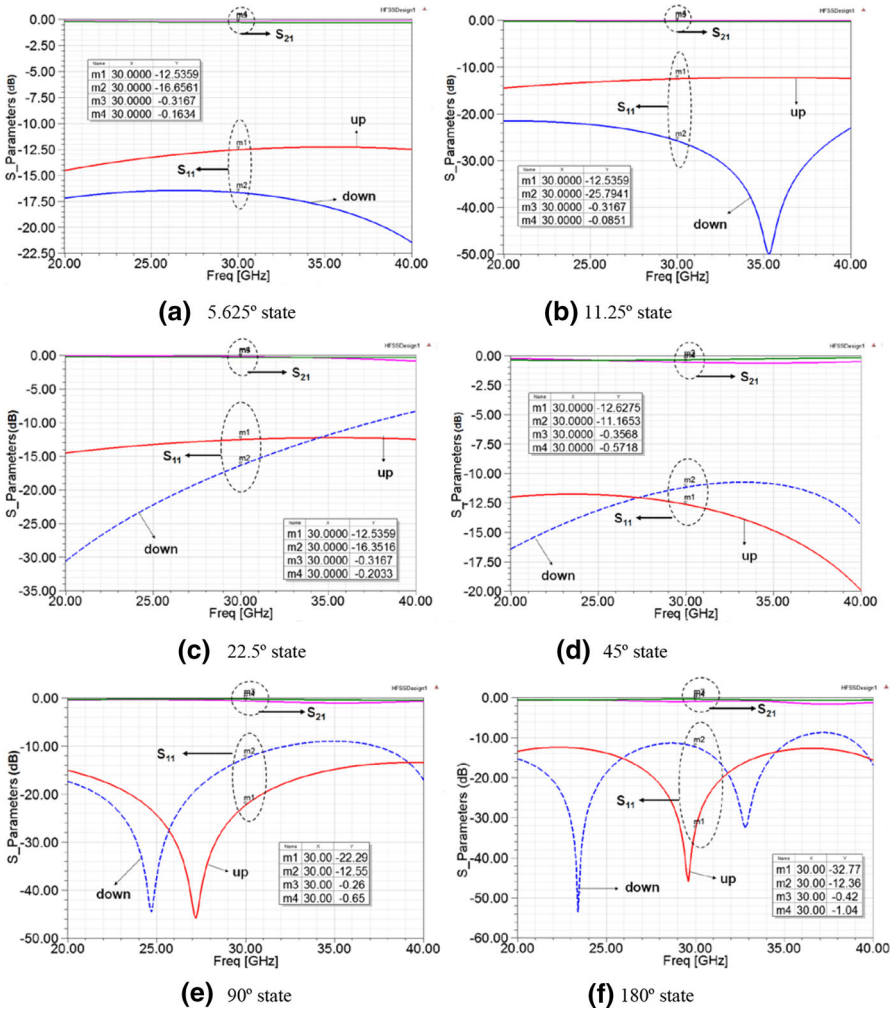

Fig.12 Simulation results of the return loss and insertion loss of six building blocks of the proposed 6-bit DMTL phase shifter

of our design, which is achieving a compact 6-bit phase shifter. It should be mentioned that in 6-bit phase shifters that use one-state unit cells (5.625° cells) or two-state unit cells (11.25° cells), the impedance matching between the building blocks is easily achieved. However, due to a large number of unit cells (64 unit cells in one-state and 32 in two-state designs), the total size is large.

In the present study, the unit-cell-level method is used (instead of the binary-weighted method) to achieve appropriate return losses for all 64 states and increase the accuracy of phase shifts by maintaining the same number of cells (17 cells). In this method, to implement each of 64 states of the 6-bit phase shifter, the unit cells are used first in minor phase shift modes (5.625° and 11.25°). Unit cells U1 and U17

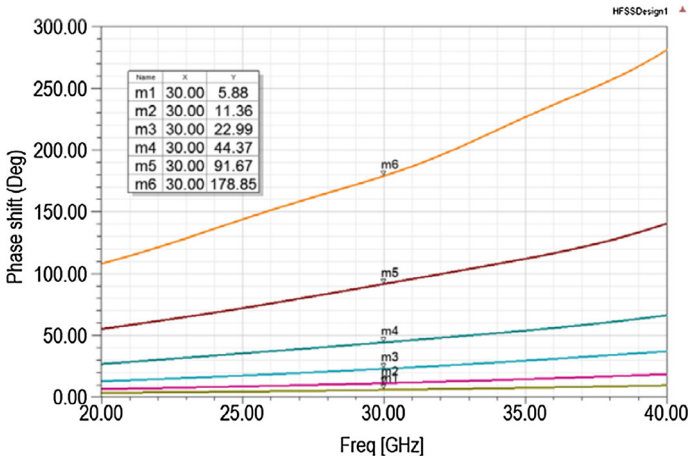

Fig. 13 Simulation results of phase shift of six building blocks of the proposed phase shifter

are only actuated in 5.625° and 11.25° phase shift modes, and the other unit cells (U2 to U16) are actuated in 11.25° and 22.5° modes (Fig.14). Table 5 shows the sequence for unit cells actuation. In this table, the subscripts 1, 2, and 3 indicate, respectively, 5.625°, 11.25°, and 22.5° phase shifts of a unit cell.

To obtain an appropriate impedance matching between unit cells and hence a low return loss and low phase shift error for the designed phase shift, the priority of unit cells U2-U16 is to provide a 11.25º phase shift. A phase shift of 22.5° is the second priority of unit cells to achieve the desired phase state (Table 5). For example, to implement phase state no. 6 (28.125°), we can use two 11.25° and one 5.625° unit cells instead of one 22.5° and one 5.625° unit cells. As another example, for obtaining a 45° shift, four 11.25° unit cells are implemented instead of two 22.5° unit cells, so a good impedance matching is realized. Table 6 compares some phase states of a 6-bit phase shifter using the two different methods.

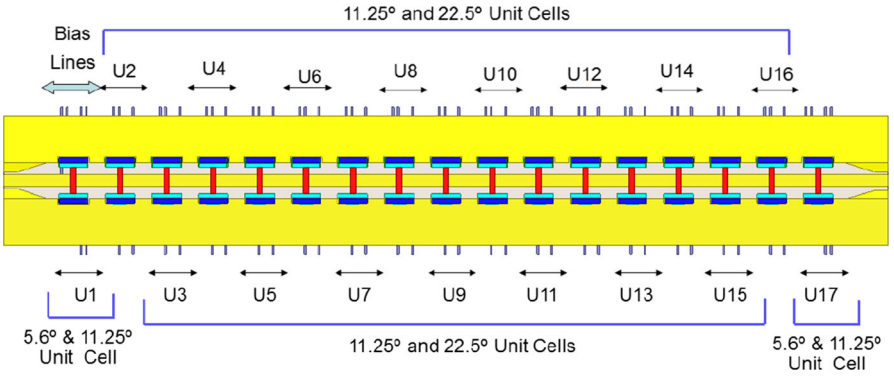

Fig. 14 Unit-cell-level actuation for the proposed 6-bit DMTL phase shifter using three-state unit cells

Table 5 Unit cell actuation sequence for 64 phase states

State No.	1	2	3	4	5	6		62	63	64
State phase (°)	0	5.625	11.25	16.875	22.5	28.125		343.125	348.75	354.375
U1	–	1	2	1	2	1		2	2	3
U2	–	–	–	2	2	2		2	3	3
U3	–	–	–	–	–	2		3	3	3
U4	–	–	–	–	–	–		3	3	3
U5	–	–	–	–	–	–		3	3	3
U6	–	–	–	–	–	–	000	3	3	3
U7	–	–	–	–	–	–		3	3	3
U8	–	–	–	–	–	–		3	3	3
U9	–	–	–	–	–	–		3	3	3
U10	–	–	–	–	–	–		3	3	3
U11	–	–	–	–	–	–	000	3	3	3
U12	–	–	–	–	–	–		3	3	3
U13	–	–	–	–	–	–		3	3	3
U14	–	–	–	–	–	–		3	3	3
U15	–	–	–	–	–	–		3	3	3
U16	–	–	–	–	–	–		2	2	2
U17	–	–	–	–	–	–		1	2	1

Table 6 Comparison of different implementations of phase states

Phase state	28.125°	28.125°	45°	45°
Implementation method	Binary-weighted 5.625° and 22.5° blocks	Unit cell level U1 = 5.625° U2 = 11.25° U3 = 11.25°	Binary-weighted 45° block (two 22.5° unit cells)	Unit cell level U1–U4 = 11.25 °
Return loss (dB)	− 6.5	− 10.5	− 9.3	− 22.6
Phase shift	30.5°	29.5°	42.7°	46.1°
Phase error	− 2.375°	− 1.38°	2.3°	− 1.1°

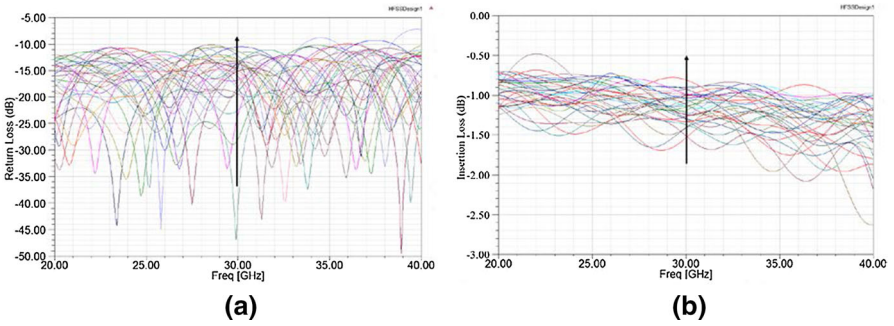

Fig. 15 Scattering parameters of 64 states of the proposed 6-bit DMTL phase shifter. **a** Return loss, **b** insertion loss

The proposed 6-bit DMTL phase shifter is simulated using ANSOFT HFSS to investigate frequency response. Figure 15 shows the insertion loss and return loss of the 64 states of the 6-bit phase shifter. The phase shift errors for various cases are given in Table 7, and the RMS phase error is shown in Fig. 16. Based on the frequency simulation results, the average loss is 1.2 dB, and the RMS phase error is 1.35°.

4.2 Electrostatic Simulation

An electrostatic simulation is performed in IntelliSuite to verify the pull-in voltage results calculated for the MEMS and MAM bridges of the designed unit cell. Table 8 presents the mechanical and electrical properties of the bridges.

The three bridges used in the designed three-state unit cell are clamped–clamped microbeams that are located on the substrate. For better illustration, the bridges are simulated, and anchors specify the boundary conditions. The pull-in voltage, stress distribution, and charge density of the MEMS, MAM-1, and MAM-2 bridges are shown in Figs. 17, 18, and 19, respectively. Based on the simulation results, the maximum stress distribution on the bridges is significantly smaller than the maximum yield stress of the bridge material (gold). The electrostatic simulation results are compared with the calculation results in Table 8.

Table 9 compares the performance of the proposed DMTL phase shifter and the previous state-of-the-art DMTL phase shifters. Based on our knowledge, the designed 6-bit DMTL phase shifter is the smallest phase shifter that has been designed so far.

5 Fabrication Process

Usually, there are two mismatches in MEMS phase shifters. The first mismatch is desired and creates a significant phase shift. The second mismatch is due to MEMS process variations, including different unit cells and unsuitable bridge air gap. The mismatch between different unit cells can be resolved using an appropriate actuation voltage. The air gap of the bridge determines the loading capacitance and phase shift

Table 7 Phase shift error of 64 states of the proposed 6-bit DMTL phase shifter

Phase state (°)	Phase shift (°)	Phase error (°)	Phase state (°)	Phase shift (°)	Phase error (°)	Phase state (°)	Phase shift (°)	Phase error (°)	Phase state (°)	Phase shift (°)	Phase error (°)
0	0	0	90	91.66	− 1.66	180	182.24	− 2.24	270	268.75	1.25
5.625	4.17	1.455	95.625	96.8	− 1.175	185.625	188.25	− 2.625	275.625	274.25	1.375
11.25	11.75	− 0.5	101.25	99.67	1.58	191.25	191.73	− 0.48	281.25	282.2	− 0.95
16.875	17.37	− 0.495	106.875	106.7	0.175	196.875	196.36	0.515	286.875	287.5	− 0.625
22.5	24.09	− 1.59	112.5	110.61	1.89	202.5	204.61	− 2.11	292.5	293.3	− 0.8
28.125	29.51	− 1.385	118.125	119.4	− 1.275	208.125	207.66	0.465	298.125	297.25	0.875
33.75	34.6	− 0.85	122.75	124.01	− 1.26	213.75	212.33	1.42	303.75	304.4	− 0.65
39.325	40.41	− 1.085	129.375	131.11	− 1.735	219.325	221.25	− 1.925	309.375	308.25	1.125
45	46.1	− 1.1	135	136.41	− 1.41	225	225.95	− 0.95	315	316.3	− 1.3
50.625	52.29	− 1.665	140.625	141.16	− 0.535	230.625	230.95	− 0.325	320.625	322.25	− 1.625
56.25	57.73	− 1.48	146.5	148.01	− 1.51	236.25	234.81	1.44	326.5	328	− 1.5
61.875	62.14	− 0.265	151.875	153.91	− 2.035	241.875	240.61	1.265	331.125	332.5	− 1.375
67.5	68.85	− 1.35	157.5	158.25	− 0.75	247.5	248.3	− 0.8	337.5	335.4	2.1
73.125	74.31	− 1.185	163.125	164.1	− 0.975	253.125	253.8	− 0.675	343.125	344.75	− 1.625
78.75	80.66	− 1.91	168.75	171.51	− 2.76	258.75	259.6	− 0.85	348.75	349.4	− 0.65
84.375	85.2	− 0.825	174.375	176.76	− 2.385	264.375	263.45	0.925	354.375	354.75	− 0.375

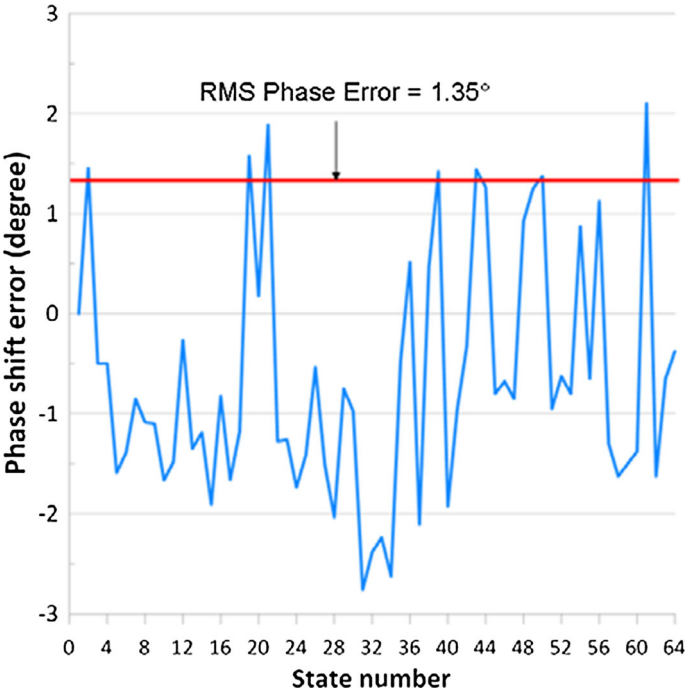

Fig. 16 Phase shift error of 64 states of the proposed 6-bit DMTL phase shifter

Table 8 Comparison of the results of electrostatic calculation and simulation of bridges

	Spring constant MAM-1 (N/m)	Spring constant MAM-2 (N/m)	Spring constant MEMS (N/m)	Pull-in voltage MAM-1 (V)	Pull-in voltage MAM-2 (V)	Pull-in voltage MEM7S (V)
Calculation	0.77	1.16	1.964	2.51	2.34	3.3
Simulation	–	–	–	3.8	2.8	3.2

accuracy. Any mismatch in the air gap leads to a significant phase error in MEMS phase shifters. In practice, to resolve this problem, the air gap is considered a little larger than required. Therefore, an offset voltage is first applied to the bridge to adjust the air gap at the desired value. Then, the bridge is ready for the actuation to create a phase shift. This issue is considered in the present paper. The structure of the designed three-state unit cell is similar to conventional DMTL phase shifters, and the only difference is in the number of bridges and pull-in voltage. Therefore, there are no more mismatch cases in the designed structure compared to general structures.

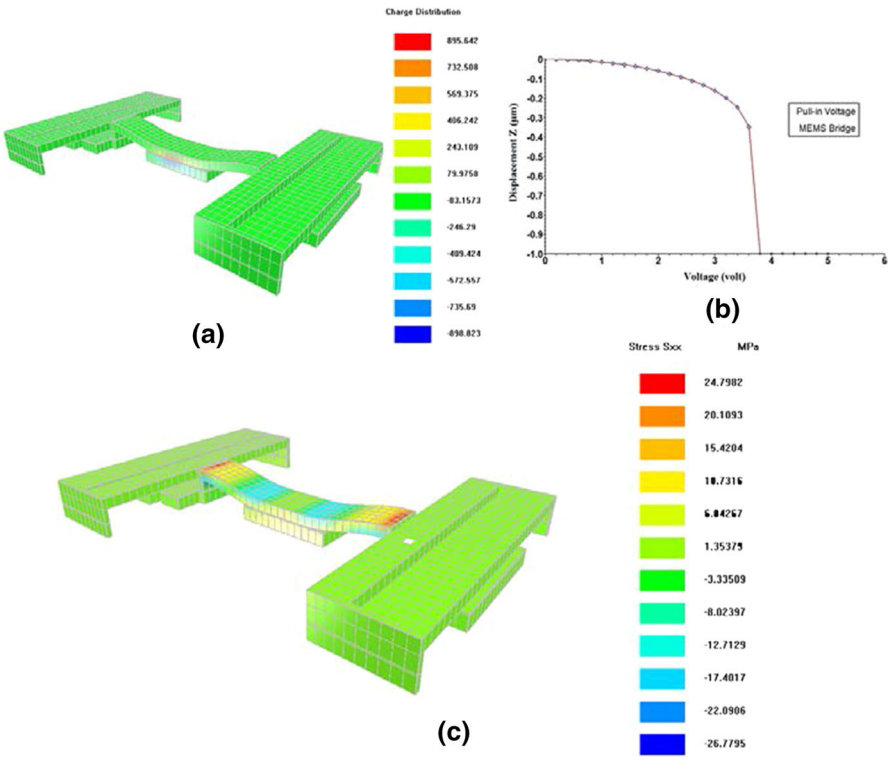

Fig. 17 Electrostatic simulation results of the MEMS bridge. **a** Charge density, **b** pull-in voltage, and **c** stress distribution

The MEMS technology has fully matured and evolved in recent years. Therefore, by following the fabrication process presented in this section, the measurement results will undoubtedly agree with the analysis and the simulation results [16]. The proposed fabrication process of the designed unit cell for the DMTL phase shifter is shown in Fig. 20. In the first step, a 0.2-μm SiCr layer was sputtered on a glass substrate using a lift-off process to conform the biased lines for three bridges (Fig. 20a). Next, to define the CPW lines, MAM lower electrodes and bridge anchors, first, a 1000Å thin Cr layer and, then, a 3000 Å thin gold layer were sputtered and patterned using the lift-off process (Fig. 20b). To form a dielectric layer on the bottom plate of the MAM and MEMS bridges, 0.1-μm Si_3N_4 was deposited and patterned using plasma-enhanced chemical vapor deposition (PECVD) (Fig. 20c). The next step was to increase the height of the MAM and MEMS bridges, which was done by defining and then electroplating (Fig. 20d). Then, the photoresist was deposited and patterned as the sacrificial layer to create the gap of MAM and MEMS capacitors (Fig. 20e). To build the bridges, 300/1000/1000 Å Cr/Au/Ti seed layer was first deposited and patterned, followed by 1 μm Au electroplating (Fig. 20f). The final step was to remove the sacrificial layer by isotropic plasma etching (Fig. 20g).

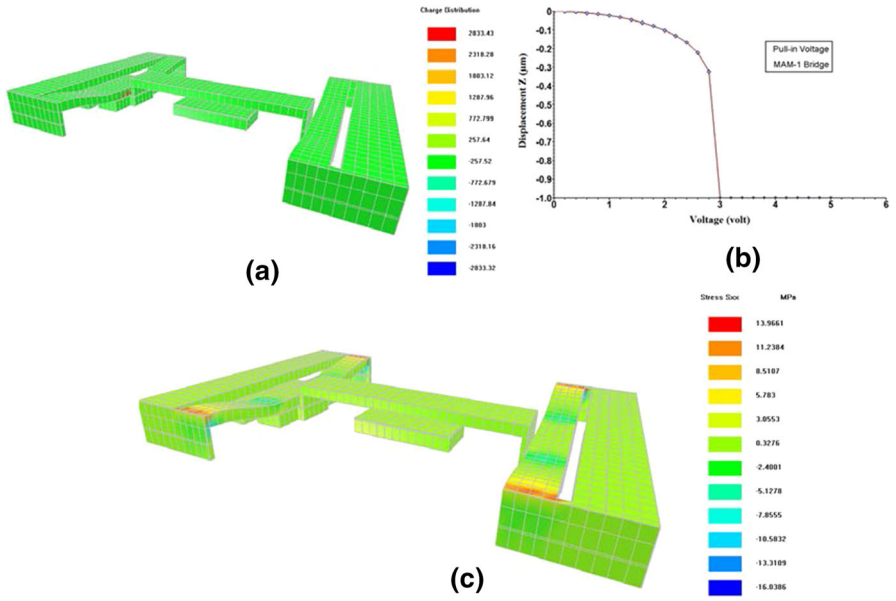

Fig. 18 Electrostatic simulation results of the MAM-1 bridge. **a** Charge density, **b** pull-in voltage, and **c** stress distribution

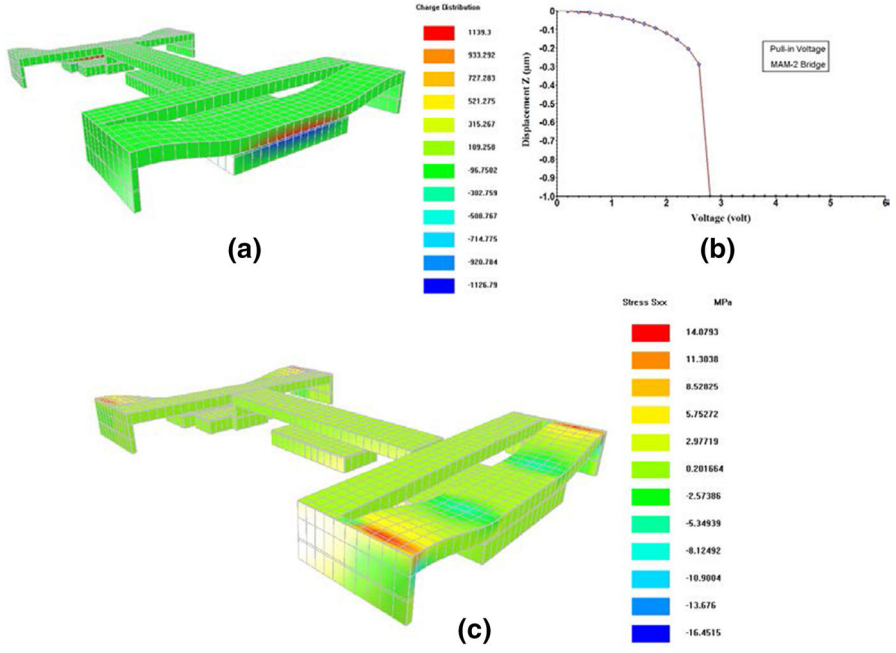

Fig. 19 Electrostatic simulation results of the MAM-2 bridge. **a** Charge density, **b** pull-in voltage, and **c** stress distribution

Table 9 Comparison of the proposed DMTL phase shifter and the current state-of-the-art phase shifters

Refs.	Bit num	Cell num	Unit cell state	Unit cell size (μm)	Operating freq. (GHz)	RMS phase error (°)	Max. return loss (dB)	Min. insertion loss (dB)	Pull-in voltage (V)	Total length (mm)
[14]*	2	21	1	400	37.7	1	− 11.5	− 1.5	20	8.4
[5]*	3	14	1	780	26	8.5	− 7	− 1.7	60	11
[27]	3	28	1	200	15	N/A	− 14.23	− 0.82	7.75	5.6
[8]	4	15	1	400	30	3.98	− 10	− 1.37	N/A	12
[9]	5	31	1	1300	10	1.73	− 13.6	− 1.7	30.1	20.46
[3]	6	32	2	400	30	2.1	− 11	N/A	6.8 – 3.4	12.8
[10]	6	32	1	586	18	1.4	− 10.5	− 1.8	13	18.5
This work	6	17	3	500	30	1.35	− 10.57	− 1.6	2.8–3.2–3.8	8.5

*Measurement

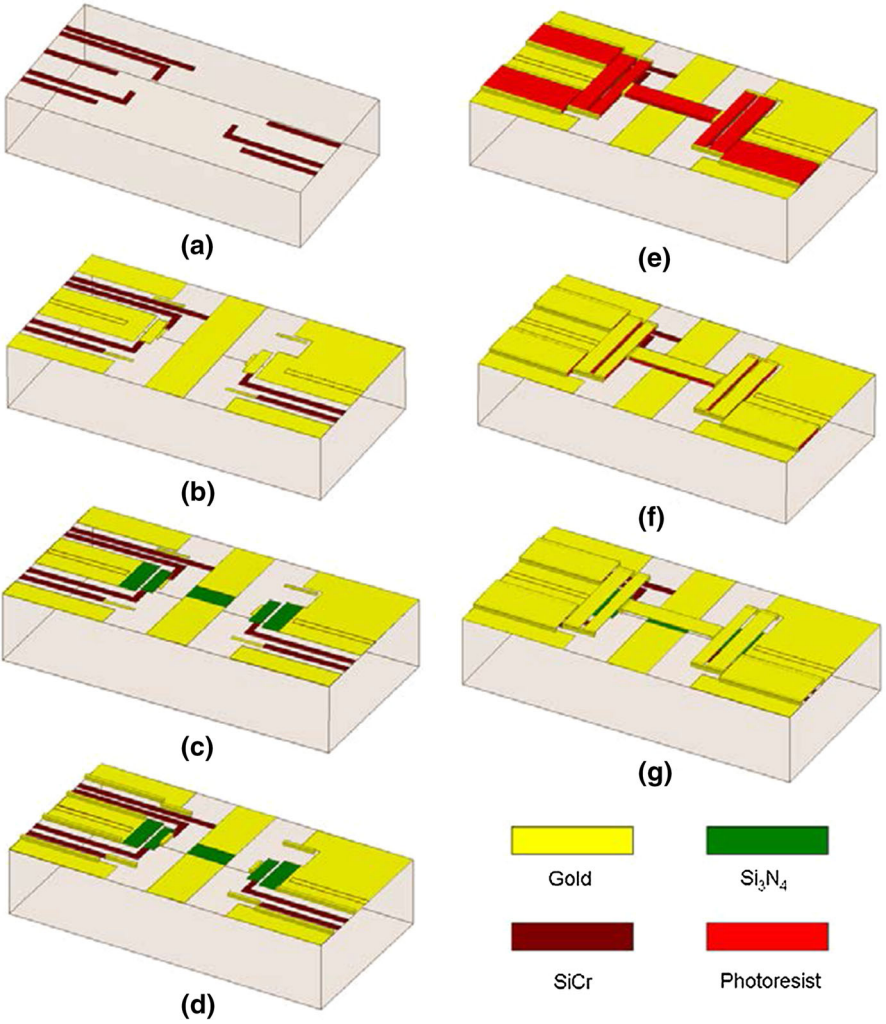

Fig. 20 Proposed fabrication process of the designed unit cell for the DMTL phase shifter

6 Conclusion

A novel three-state unit cell for a compact, low-loss 6-bit DMTL phase shifter was designed, analyzed, and simulated in this study. The designed unit cell structure consisted of a coplanar waveguide transmission line, a MEMS, and two-pair metal–air–metal bridges. The bridge capacitors were electrically in series and were actuated in three different modes; in each mode, the distributed capacitance on the transmission line and the phase velocity were changed to achieve a phase shift. The novelty of this design is that the number of unit cells is reduced from 64 (which is the case in a conventional 6-bit phase shifter) to only 17. Therefore, the overall size

of the 6-bit phase shifter is considerably reduced. Due to the very small size of the proposed phase shifter, the loss also decreases. The designed structure was simulated using Ansoft HFSS and IntelliSuite. Based on the simulation results, the lateral size of the phase shifter is only 8.5 mm; the root-mean-square (RMS) phase error is 1.35°, and the average loss is 1.2 dB. The main advantages of the designed MEMS phase shifter are its compact size, low RMS phase error, low loss, and low pull-in voltage. A step-by-step fabrication process was also proposed for designing the DMTL phase shifter. This means that the feasibility of the proposed design was investigated using the proposed fabrication process. Based on the fact that MEMS technology has fully matured characteristics, in the case of measuring, the results will certainly be in good agreement with the analysis and simulation results.

Data Availability Data sharing is not applicable to this article as no datasets were generated or analyzed during the current study.

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