Circuits, Systems, and Signal Processing (2022) 41:2541–2565
https://doi.org/10.1007/s00034-021-01924-1

Analysis and Design of an Efficient 8-Bit 2b/Cycle SAR ADC with Multiple Calibration Techniques

Yushi Chen[1] · Yuan Yuan[2] · Hualian Tang[1] · Yiqi Zhuang[1]

Received: 20 August 2021 / Revised: 24 November 2021 / Accepted: 25 November 2021 /
Published online: 23 January 2022

Abstract

This paper presents a low-power asynchronous 8-bit 500MS/s 2b/cycle successive-approximation-register (SAR) analog-to-digital converter (ADC) in 40 nm CMOS process. The proposed ADC shows high energy efficiency and good performance against process–voltage–temperature (PVT) variations by a background offset mismatch calibration technique, a supply voltage calibration technique and an efficient 2b/cycle switching scheme. The background offset mismatch calibration eliminates the effect of offset mismatches of the comparator array without any extra phase. The supply voltage calibration is presented to monitor the conversion speed of the ADC and adjust the speed of comparators to ensure the ADC can work properly at different process corners. The improved switching scheme helps cut down the switch times and simplifies the switch logic, which saves 87.8% switching energy compared with conventional V_{CM}-based scheme. The proposed SAR ADC simulated a signal-to-noise plus distortion ratio (SNDR) of 45.8 dB and a spurious-free dynamic range (SFDR) of 55.5 dB for a near-Nyquist input while consuming a total power of 2.59 mW, culminating in a Walden figure of merit (FoM) of 32 fJ/conversion-step.

Keywords 2b/cycle SAR ADC · Background offset mismatch calibration · Supply voltage calibration · Process–voltage–temperature (PVT)

✉ Hualian Tang
hltang@xidian.edu.cn

Yushi Chen
yushichen001@outlook.com

Yuan Yuan
2410545265@qq.com

Yiqi Zhuang
yqzhuang@xidian.edu.cn

[1] School of Microelectronics, Xidian University, Xi'an 710071, People's Republic of China

[2] Science and Technology on Low-Light-Level Night Vision Laboratory, Xi'an 710076, People's Republic of China

1 Introduction

With rapid development of wireless communications, high-speed and medium-resolution analog-to-digital converters (ADCs) are in high demand for related applications [4, 16, 21]. Normally, flash and pipeline architectures are the first choice to meet these specifications. However, as the supply voltage decreases, the design of analog circuits becomes more difficult with the demand for low power consumption. In recent years, the development of manufacturing processes and research of speed accelerated structure make other kind of ADC meet the above requirements, such as successive-approximation-register (SAR) ADC. Compared with conventional high-speed ADC, SAR ADC shows better performance in analog complexity and power efficiency [12, 15, 17, 28].

Many researchers have devoted their effort to enhancing the conversion speed of SAR ADCs [2, 3, 5, 7–9, 11, 22, 24, 25, 29, 30]. Time-interleaving (TI) SAR ADC presents a tempting solution to achieving high speed and low power consumption. However, any TI-ADC array suffers from the path-mismatch errors (gain, offset, and timing skew) that can severely limit the spectral performance of the ADC [3, 25, 30]. The two-step pipeline SAR is another structural extension to the conventional SAR ADC for breaking the speed limit. In a two-step SAR ADC, an accurate amplifier is needed to transfer the conversion residue from the first stage to the second. Typically, the achievable bandwidth and power efficiency of the residue amplifier limits the performance of the whole ADC. Thus, the design of an accurate residue amplifier is the key point for two-step approach [7, 24, 29]. 2-bit per cycle conversion scheme is also a popular method in recent years. The 2b/cycle SAR ADC speeds up the conversion by resolving 2-bit in each comparison, which needs fewer comparisons compared with the 1b/cycle scheme. However, this method needs extra hardware and logic units, leading to a higher PVT sensitivity on the conversion speed. Also, the offset among the comparators requires calibration [5, 8, 22]. The reference settling time is also a speed limiting factor. As CMOS technology scales down and the speed of SAR increases, reference settling limitation becomes even more significant. In [2], a passive charge sharing SAR ADC was proposed to achieve shorter reference settling time. The passive charge sharing SAR ADC is a new type, which is different from the traditional charge redistribution. The charge redistribution uses a fixed voltage reference to supply any charge required to rebalance the sampled signal. The passive charge sharing uses pre-sampled reference charge to rebalance the sampled signal. One maintains a fixed voltage and supplies variable charge, while the other begins with a fixed charge and needs to deal with a variable voltage.

In this paper, an asynchronous 2b/cycle SAR ADC with multiple calibration techniques is proposed. A background offset mismatch calibration technique based on dynamic element matching (DEM) technique is proposed to eliminate the effect of offset mismatch of comparator array. A supply voltage calibration technique is designed to monitor and adjust the speed of ADCs, which helps to make ADCs perform better against PVT variations. In order to reduce switching energy, an efficient 2b/cycle switching scheme is also introduced in this paper. The organization of the remaining part of this paper is as follows. Section 2 presents the architecture of the proposed

SAR ADC. Section 3 describes the simulation results, and Sect. 4 gives a discussion about challenges for silicon implementation. The conclusion is given in Sect. 5.

2 Architecture of the Proposed SAR ADC

The structure of the proposed 2b/cycle SAR ADC is shown in Fig. 1, which mainly consists of fully differential reference DAC array (REF_DAC) and signal DAC array (SIG_DAC), comparator array with supply voltage calibration module and offset mismatch calibration module, bootstrapped switches and SAR logic. Figure 2a shows the REF_DAC along with the waveforms of control signals EN1-4. EN1-4 and their inverse signals are generated by SAR logic, which are used to control the switch of REF_DAC to provide references for comparator array. The differential structured REF-DAC generates $\pm$ 1/2V_{REF}, $\pm$ 1/8V_{REF}, $\pm$ 1/32V_{REF}, and $\pm$ 1/128V_{REF} four group references, respectively. The operation of the REF_DAC is as follows: during the sampling period, the sampling switches controlled by the sampling signal allow the top plates of capacitors to be connected to V_{CM}. EN1-4 and their complementary

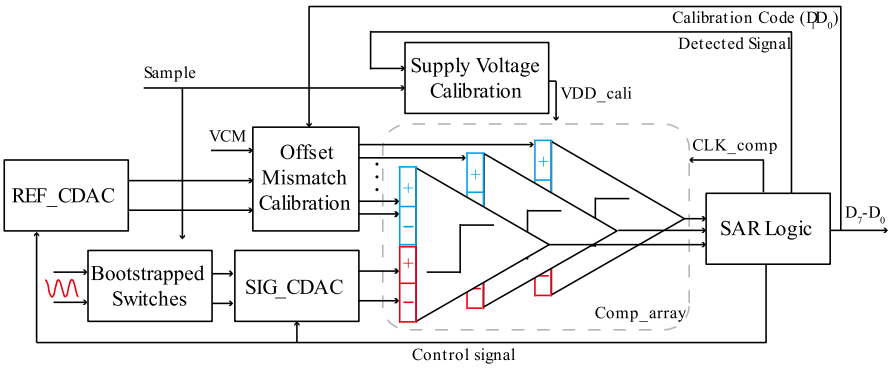


Fig. 1 Block diagram of the proposed SAR ADC

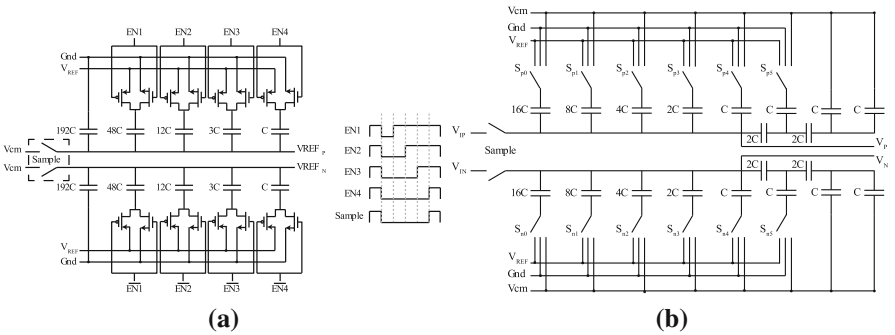


Fig. 2 The structure of **a** REF_DAC and **b** SIG_DAC

signals control bottom plates of the P capacitor array and N capacitor array connected to Gnd and V_{REF}, respectively. After the sampling phase, the sampling switches turn off, the following operations follow the timing diagram shown in Fig. 2a to generate the references to the comparators. During the operation, the bottom plates of the MSB capacitors are always connected to Gnd. In the design of SIG_DAC, two C-2C capacitors are added to cut down 70.3% number of capacitors compared with conventional V_{CM}-based scheme which is shown in Fig. 2b. The illustration of the operation of SIG_DAC will be given in later section.

2.1 An Efficient 2b/Cycle Switching Scheme

In order to save switching energy, an improved switching scheme for 2b/cycle SAR ADC is proposed based on V_{CM}-based switching method [27]. Figure 3 uses a 4-bit DAC to illustrate the proposed switching scheme. When D_3D_2 is 00 and 11, the proposed scheme is consistent with the traditional V_{CM}-based scheme. The proposed switching scheme simplified switch times when D_3D_2 is 10 and 01. In traditional scheme, both of the two capacitors with the highest weight need to switch to different references according to the quantization results. In the proposed scheme, on the premise of maintaining charge conservation, the two-time switches are combined into one-time, only one capacitor needs to switch to new reference and the other remains constant. We take $D_3D_2 = 01$ as an example to explain the difference between the conventional and the improved methods. Equations (1) and (2) explain the voltage changes of capacitor array for the conventional and the improved methods, respectively. V_P and V_N are the initial voltage of the top plate of the capacitor array. V_{PC}' and V_{NC}' are the voltage of conventional method after conversion. V_{PI}' and V_{NI}' are the voltage of improved method after conversion.

$$\begin{aligned}
&(V_P - V_{CM}) \cdot 8C = (V_{PC'} - V_{CM}) \cdot 2C + (V_{PC'} - V_{\mathrm{REF}}) \cdot 4C + (V_{PC'} - \mathrm{Gnd}) \cdot 2C \\
&(V_N - V_{CM}) \cdot 8C = (V_{NC'} - V_{CM}) \cdot 2C + (V_{NC'} - V_{\mathrm{REF}}) \cdot 2C + (V_{NC'} - \mathrm{Gnd}) \cdot 4C \\
&V_{PC'} - V_P = 1/8V_{\mathrm{REF}} \\
&V_{NC'} - V_N = -1/8V_{\mathrm{REF}}
\end{aligned} \tag{1}$$

$$\begin{aligned}
&(V_P - V_{CM}) \cdot 8C = (V_{PI'} - V_{CM}) \cdot 6C + (V_{PI'} - V_{\mathrm{REF}}) \cdot 2C \\
&(V_N - V_{CM}) \cdot 8C = (V_{NI'} - V_{CM}) \cdot 6C + (V_{NI'} - \mathrm{Gnd}) \cdot 2C \\
&V_{PI'} - V_P = 1/8V_{\mathrm{REF}} \\
&V_{NI'} - V_N = -1/8V_{\mathrm{REF}}
\end{aligned} \tag{2}$$

Equations (1) and (2) verify that the voltage changes of capacitor array for the two methods are the same, which means that the improved method is correct. Equations (3) and (4) explain the switching energy for the conventional and the improved methods, respectively.

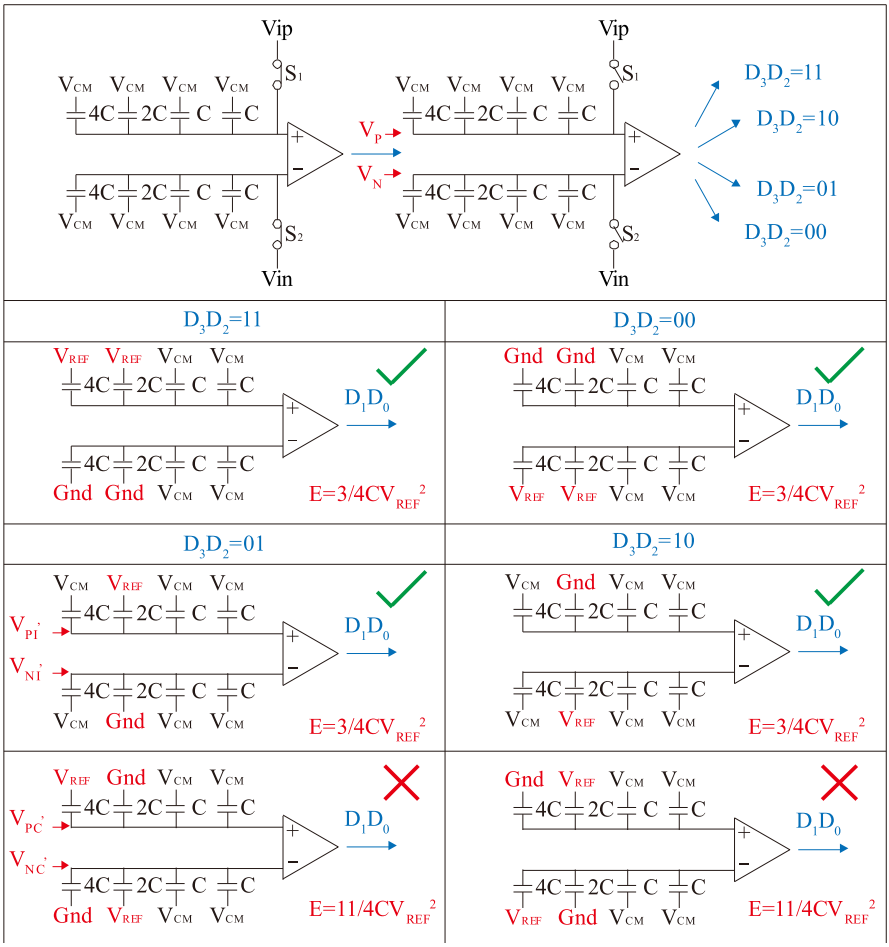


Fig. 3 Proposed DAC switching scheme of 4-bit DAC

$$E_C = V_{\mathrm{REF}} \cdot 4C \cdot [(V_P - V_{CM}) - (V_{PC'} - V_{\mathrm{REF}})] + V_{\mathrm{REF}} \cdot 2C \cdot [(V_N - V_{CM}) - (V_{NC'} - V_{\mathrm{REF}})] = 11/4CV_{\mathrm{REF}}^2 \quad (3)$$

$$E_I = V_{\mathrm{REF}} \cdot 2C \cdot [(V_P - V_{CM}) - (V_{PI'} - V_{\mathrm{REF}})] = 3/4CV_{\mathrm{REF}}^2 \quad (4)$$

As shown in Eq. (3) and (4), the switching energy is cut down from $11/4CV_{REF}{}^2$ to $3/4CV_{REF}{}^2$. The conversion when $D_3D_2 = 10$ is similar to $D_3D_2 = 01$. Hence, the improved method reduces the switching times and power consumption and simplifies the control logic of the switch.

The behavior simulations of an 8-bit SAR ADC based on some published switching schemes [6, 13, 23, 26, 27, 31] and the proposed scheme are performed in MATLAB.

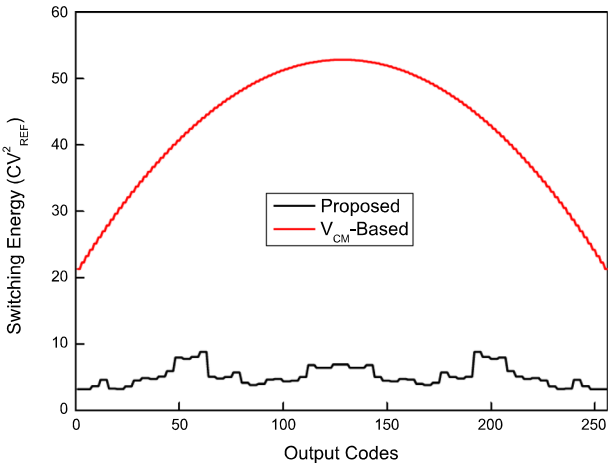


Fig. 4 Switching energy against output codes

Table 1 Comparison of main features between different schemes for 8-bit SAR ADC

Switching scheme	Average switching energy (CV_{REF}^2)	Energy saving	Total number of unit capacitors	Area reduction
Conventional	340.82	Reference	512	Reference
Ginsburg [6]	214.72	37%	256	50%
Monotonic [13]	63.88	81.26%	256	50%
V_{CM}-based [27]	42.54	87.52%	256	50%
Tri-level [26]	10.61	96.89%	128	75%
VMS [31]	7.97	97.66%	128	75%
Wang [23]	6.64	98.05%	128	75%
Proposed	5.17	98.48%	76	85.16%

Figure 4 shows a comparison of switching energy between V_{CM}-based switching scheme and the proposed scheme, which consumes 42.54 CV_{REF}^2 and 5.17 CV_{REF}^2 average switching energy, respectively. Table 1 summarizes main features of different switching schemes, which shows that the proposed scheme has good performance in energy reduction and area reduction compared with published schemes.

For the proposed ADC, it takes four comparison cycles to obtain 8-bit digital output code. After each comparison, the DAC array operates according to the switching method. After the last comparison, the output code is got directly and there is no need switching the switches connected to the DAC array. Therefore, it only needs to change

Table 2 The logic circuits designed for proposed 8-bit SAR ADC

	Switch logic for P array	Switch logic for *N* array
3 pairs of (i, i-1) (7, 6) (5, 4) (3, 2)	$\mathrm{Gnd(i)} = \overline{N_i + N_{i-1}}$	$\mathrm{Gnd(i)} = \overline{P_{i-1} + \overline{N_i}}$
	$V_{\mathrm{CM}}(\mathrm{i}) = \overline{N_i + N_{i-1}} + \overline{P_i + \overline{N_{i-1}}}$	$V_{\mathrm{CM}}(\mathrm{i}) = \overline{P_{i-1} + \overline{N_i}} + \overline{N_i + N_{i-1}}$
	$V_{\mathrm{REF}}(\mathrm{i}) = \overline{N_i} + P_{i-1}$	$V_{\mathrm{REF}}(\mathrm{i}) = \overline{P_i} + N_{i-1}$
	$\mathrm{Gnd(i\ -1)} = \overline{N_i}$	$\mathrm{Gnd(i\ -1)} = \overline{P_i}$
	$V_{\mathrm{CM}}(\mathrm{i\ -1}) = \overline{N_i} + \overline{P_i}$	$V_{\mathrm{CM}}(\mathrm{i\ -1}) = \overline{N_i} + \overline{P_i}$
	$V_{\mathrm{REF}}(\mathrm{i\ -1}) = P_i$	$V_{\mathrm{REF}}(\mathrm{i\ -1}) = N_i$

the references connected to P terminal and N terminal capacitor arrays for three times to obtain 8-bit binary digital code.

The switching process is as follows: ADC gets MSB and MSB-1 after the first comparison, namely D_7 and D_6. Then ADC gets D_5 and D_4 after the second comparison, D_3 and D_2 after the third comparison, and D_1 and D_0 after the fourth comparison. There is no need to switch the switches after D_1 and D_0 are obtained, the bottom plates of capacitors corresponding to D_1 and D_0 are always connected to V_{CM}, so the logic circuits are only required for the 6 capacitors corresponding to D_7-D_2.

The logic circuits designed in this paper are shown in logical expression, which is given in Table 2. It is divided into three groups according to the switching times. It can be seen that the control logic of each capacitor is relatively simple. Because of the differential capacitor array, the switching logic is divided into two types, controlling P terminal and N terminal capacitor arrays, respectively. P_{i} and N_{i} are the output results of the register corresponding to quantization result of each bit and they are opposite signals to each other. Since this switching method is based on V_{CM}-based, three references (Gnd, V_{CM} and V_{REF}) are required. Gnd(i), V_{CM}(i) and V_{REF}(i) correspond to the control logic of three references connected to each capacitor respectively. According to the simulation, the power consumption of logic circuits for the V_{CM}-based scheme and the proposed method are 684.7uW and 512.6uW, respectively, and the proposed method reduces the power consumption by 25.1%.

2.2 Background Offset Mismatch Calibration

Figure 5 gives the structure of the proposed high-speed comparator, which is designed based on the double-tail structure because of its better performance in low-voltage applications. The proposed comparator consists of the first dynamic amplifying stage and the second dynamic latching stage. The operation of the proposed comparator is divided in reset phase and regeneration phase. When CLK is low, the comparator is in reset phase and the tail transistors of both stages are switched off, consuming no static power. During this phase, transistors M_6 and M_7 are on and pulling terminals V_1 and V_2 are at V_{DD}. Terminals V_1' and V_2' are pulled down to ground by the inverters. The transistors M_{12} and M_{15} are switched on, resetting the terminals $\mathrm{OUT_P}$ and $\mathrm{OUT_N}$ to

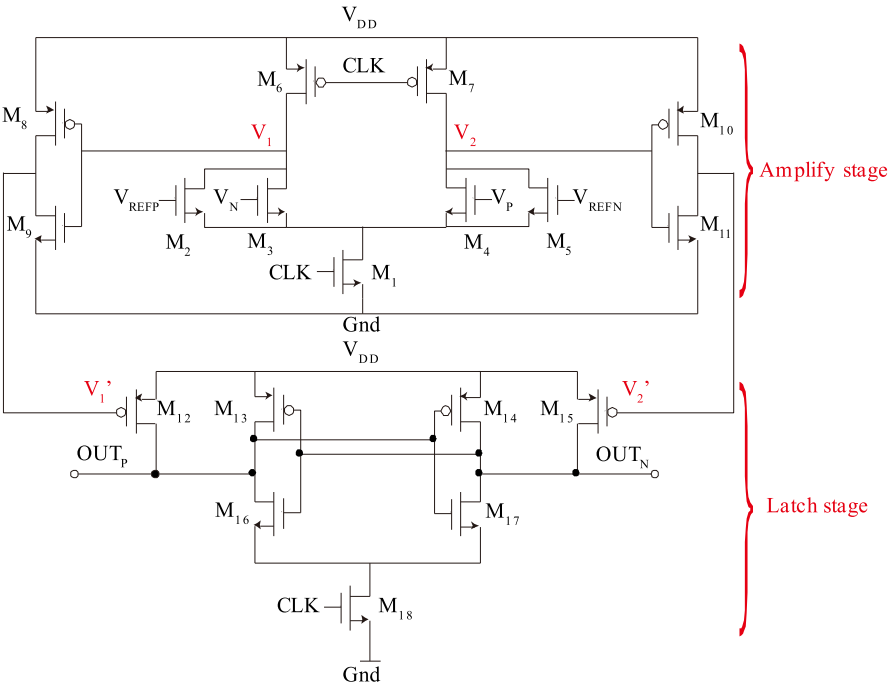


Fig. 5 Four-input high-speed comparator

V_{DD}. When the CLK is high, the comparator enters into regeneration phase. In this phase, the tail transistors turn on, while transistors M_6 and M_7 are switched off. V_1 and V_2 will discharge with different speeds depending on the corresponding input voltages. Then the positive feedback of the latch starts, forcing two outputs to reach V_{DD} and ground, respectively. Differ from traditional double-tail dynamic comparator needing a differential pair of clock signals, the proposed comparator only needs single clock signal during the comparison and reset process. This improvement is benefit to simplifying the structure and saving power consumption. The use of the single clock signal in the proposed comparator also has the advantages of the removal of the timing requirement between Clk and Clkb, which are differential pair of clock signals used in traditional comparators.

In order to give a comparison of the proposed comparator and some published papers, Table 3 lists some main features of different comparators. All circuits have been implemented and simulated in the same CMOS technology with an input of the comparator (V_P-V_N)-(V_{REFP}-V_{REFN}) is set as 1LSB. The delay, power and power delay product (PDP) are the basic performance parameters of the comparator. PDP is derived by multiplying delay and power, the detailed illustration is given in [18]. According to the table, the proposed comparator has better performance than other published papers.

In the conventional SAR ADC, the offset will affect the decision of the comparator. For 2b/cycle SAR ADCs, there are offset mismatches between the three comparators

Table 3 Comparison of main features between the comparators with different structures

Architecture	Delay (ps)	Power (uW)	PDP (fJ)
Double-tail [19]	67.2	74.4	5.0
Elzakker [20]	84	72.5	6.09
Jeon [10]	58	55.2	3.2
Savani [18]	56	54	3.02
Babayan [1]	78	89.2	6.95
Proposed	43.7	60	2.62

during the manufacturing process, which needs to be calibrated in the design. In this paper, a background offset mismatch calibration based on dynamic element matching technique is proposed to eliminate the influence of offset mismatches on ADC performance.

The random rotation-based binary-weighted selection (RRBS) [14] is presented to correct the current source mismatch in the current-steering DAC. Based on the concept of RRBS, this paper proposes a background calibration technique, which rotates three comparators randomly in the conversion of ADC to alleviate the influence of the offset mismatches. As shown in Fig. 6, the whole unit mainly consists of three comparators, four rotators and a module which generates the rotation code. $Comp_{0\text{-}2}$ are three identical four-input comparators, the red ports (signal ports) and the blue ports

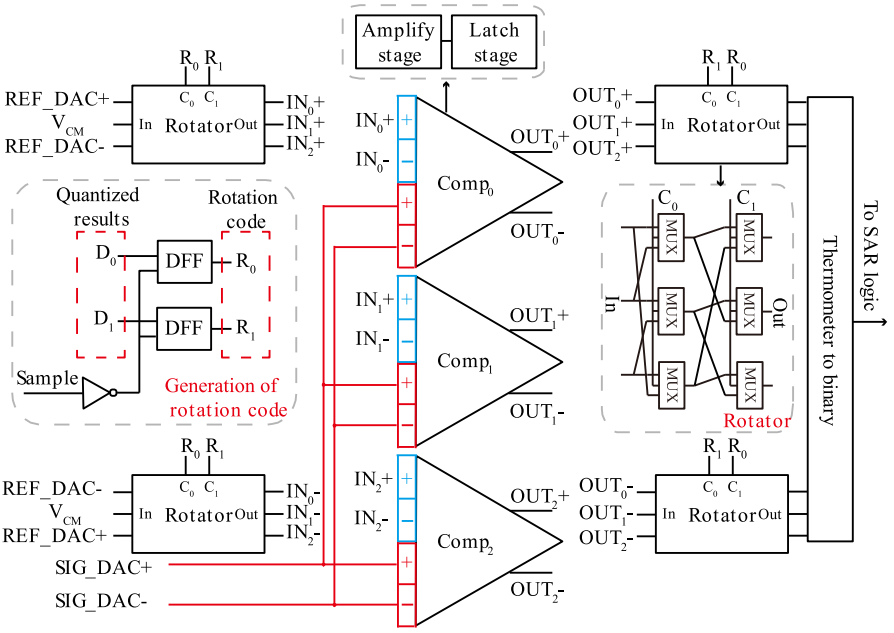


Fig. 6 Block diagram of the proposed background offset mismatch calibration

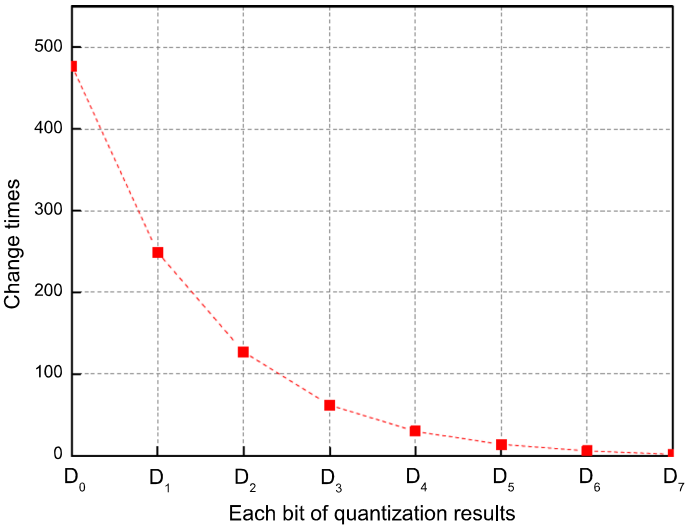


Fig. 7 The number of times each bit quantization result changes

(reference ports) are four inputs for the fully differential SIG_DAC and REF_DAC, respectively. Since the input of the signal ports of all three comparators is the same, no rotation is required. In this scheme, the comparators are rotated by rotating the order of the reference ports.

The rotators mainly consist of several MUXs. C_0 and C_1 are the control ports of the rotator which are connected to the rotation code R_0 and R_1 to control the rotation step. In RRBS, pseudo-random number generator (PRNG) is used to generate pseudo-random number as control code of rotator. However, PRNG will consume a large area with the increase of rotation step. To solve this problem, this paper presents a method using other bitstream to replace PRNG. As is known to all, the quantization result of ADC is composed of a series of 0 and 1, and low significant bit changes more frequently than high bits. Figure 7 gives the number of times each bit quantization result changes with 2048 sampling points, which illustrates that the number of change times decreases as the weight of the bit becomes high. The high significant bits change less frequently even stay constant, which result in fewer change times of rotation step. As a result, the use of high significant bit may reduce the randomness of rotation codes and make the calibration less effective. In order to ensure the randomness of rotation codes, this paper uses low weight quantization results (D_0 and D_1) to replace PRNG as the rotation code.

In order to further verify the randomness of an arbitrary bitstream, we use the power spectral density (PSD) of the bitstream, so as to compare the randomness of the ideal random bitstream, PRNG, and quantization results (D_0 D_1). Simulation results of the PSDs of three different bitstreams are shown in Fig. 8. According to the results, the PSD of the quantization results is similar to the ideal random bitstream, while the PSD of PRNG alternates periodically. Therefore, the quantization results show a better performance in randomness than PRNG in the proposed method. From the

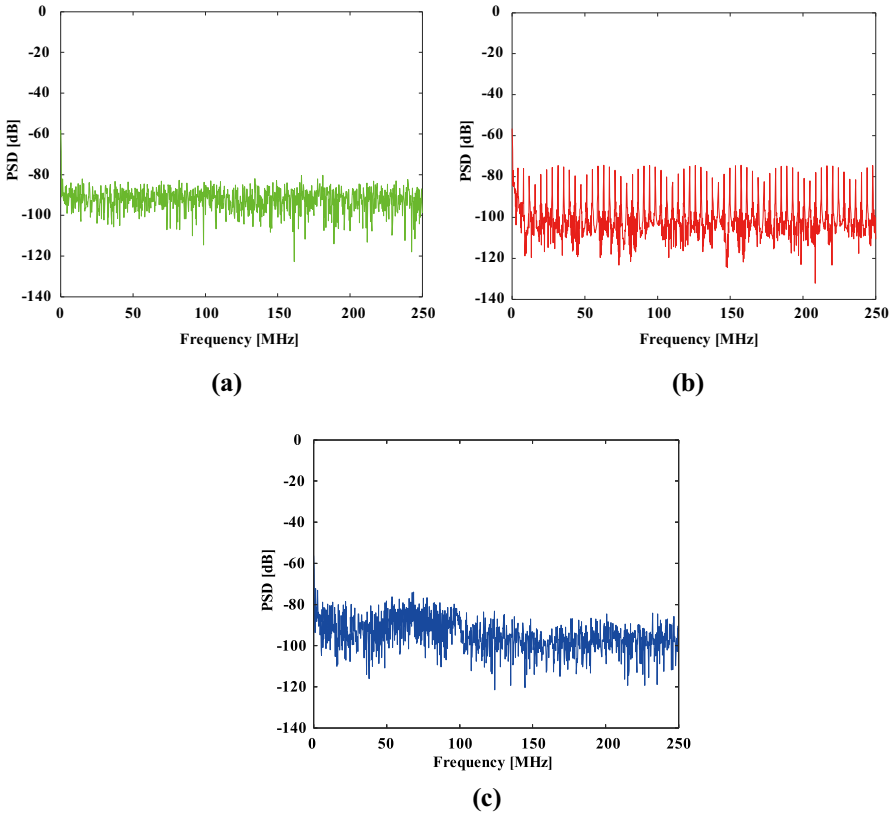


Fig. 8 The PSDs of different bitstreams **a** ideal random bitstream **b** PRNG **c** D_0 and D_1

above discussion, the quantization results (D_0 D_1) can be used to replace PRNG as the rotation code. Thanks to the method, the PRNG is removed which is beneficial to saving power consumption and simplifying logical complexity. The module which generates the rotation code is also shown in Fig. 6. DFF is triggered by the falling edge of the control signal. When the next sampling clock arrives, the quantization results (D_0 D_1) of the last period are locked as the rotation code of the comparators for the next period.

The thermometer code composed of the outputs of the three comparators needs to be converted into binary code by the decoder for the use of subsequent circuits. In the proposed scheme, the weight of the thermometer codes also changes after rotation, so it is necessary to restore the weight of thermometer codes for subsequent processing of decoder. The rotation code for the outputs is obtained by exchanging the 2-bit rotation code (R_1R_0) for the input, the specific implementation method is illustrated by an example in Fig. 9.

Figure 9 gives an example to explain the operation of the comparator array with or without rotation in detail. On the left is the traditional quantization method without rotation, and on the right is the block diagram with the random rotation. If the rotation

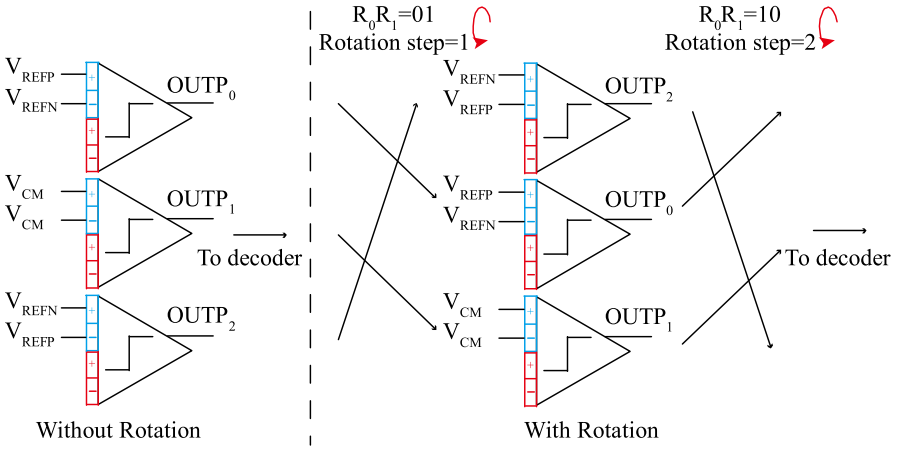


Fig. 9 Comparison of the comparator array with or without rotation

code is 1, it will rotate, and if it is 0, it will not rotate. The rotation code (R_0R_1) for the input of the comparators is 01 corresponding to 1-step rotation, so the comparator array is rotated down 1-step in turn. In order to ensure the weight of the thermometer code, the output should also be rotated before sent to the decoder. The two rotation codes of the input are exchanged and the rotation code for the output is set as 10, corresponding to 2-step rotation, and the comparator array is rotated down 2-step in turn.

2.3 Supply Voltage Calibration

After completing the conversion of all bits, all the capacitors need to be reset to the initial state before the next sampling clock. Figure 10 gives the illustration of the reset phase during the conversion of the ADC. In addition to being the control signal for REF_DAC, EN4 is also used as a reset signal of the proposed ADC. Figure 10 gives the waveforms of reset signal (EN4) under different process corners, the reset phase starts when the reset signal is high. Since the reset signal will generate when

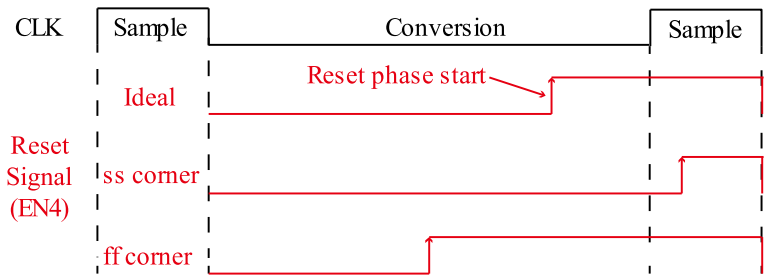


Fig. 10 The timing waveform of SAR ADC

the quantization has been completed, the generation of the reset signal is related to the quantization of LSB, which is related to the working speed of the comparator. As shown in Fig. 10, the reset signal rises after the next sampling clock due to the slower working speed of comparator at ss process corner. As a result, the ADC can't complete the reset phase before the next sampling clock, which indicates that the comparator needs to accelerate the working speed. In another case, the reset signal rises much earlier than the next sampling clock at ff process corner. In this case, the comparator's speed can be appropriately reduced to cut down the power consumption of ADC. In order to solve this problem, a supply voltage calibration of comparators is designed in this paper. By detecting the reset signal and adjusting the voltage of the comparator, the ADC can work normally at various process corners.

Figure 11 shows the block diagram of supply voltage calibration circuit of the comparator. The whole system includes reset signal detection module, switch control logic module, calibration capacitor array and some digital logic units. The reset signal detection module is mainly composed of several XORs and delay units, which compares the reset signal and the next sampling clock to detect the conversion speed of ADC. The working process of the calibration is explained as followed. First, the reset signal detection module compares the sampling signal and the reset signal (EN4). The results of the comparison are sent to the DFFs which are triggered by the falling edge. In this design, the reverse signal of the sampling signal is used to control the DFFs. Once the DFFs are triggered to work, the previous comparison signals are latched and generate calibration code. According to the calibration code, the switch control logic will generate the control signal of the four switches in the calibration capacitor array,

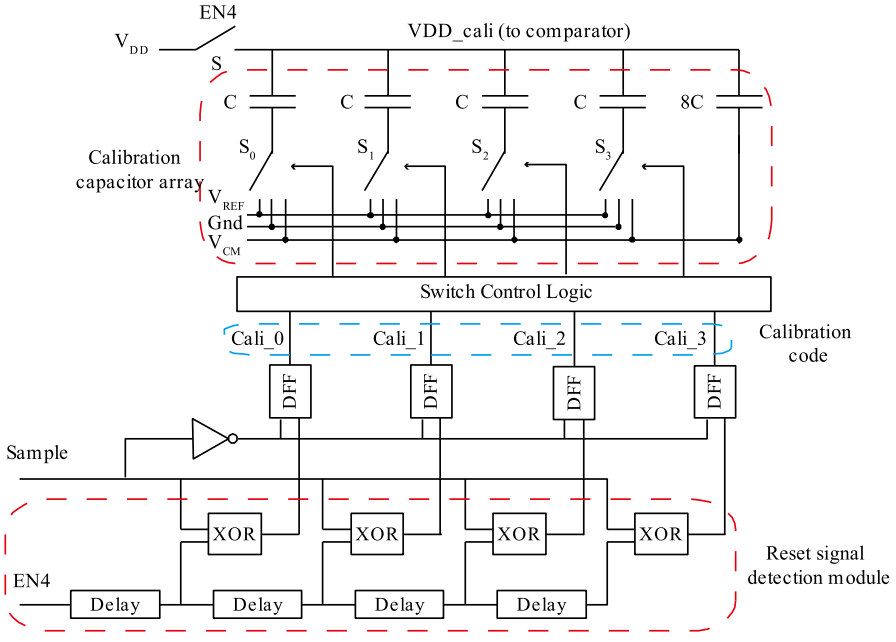


Fig. 11 Block diagram of supply voltage calibration

which are used to decide which reference to connect. This process is similar to the process that logic units control the switches of the capacitor array in SAR ADCs. The calibration capacitor array adjusts and generates the VDD_cali corresponding to the calibration code.

Figure 12 gives the timing waveforms of relevant signals to illustrate the process of the calibration in detail. Figure 12a shows that when the reset signal rises much earlier than the next sampling clock, DFF is triggered by the falling edge and the calibration code is set as 1. In this state, the comparator can be slowed down appropriately, and the calibration code control the switches of capacitor array to reduce the voltage of the comparator. Figure 12b shows that when the reset signal falls behind the sampling signal, the calibration code is set as 0. In this state, the comparator needs to be accelerated, so the calibration code controls the switches to increase the voltage of the comparator.

The proposed 4-bit calibration code is used to control the calibration capacitor array which can generate different voltages from 1.0 V to 1.4 V. During the calibration, when the reset signal EN4 is high, the switch S is on and all the top plates of the capacitors are connected to V_{DD} (1.2 V), all the bottom plates of the capacitors are set to V_{CM} (0.6 V). When the EN4 is low, the switch S is off and all of the top plates of the capacitor array is directly connected to the comparator. The bottom plates of the capacitor array are connected to different references according to the calibration code. Equation (5)-(7) gives some examples to illustrate the generation of supply voltage.

The change of supply voltage controlled by unit capacitor is defined by

$$|\Delta V| = V_{CM} \cdot C/12C = 1/12V_{CM} = 0.05V \tag{5}$$

When the calibration code is 0000, the bottom plates of the four unit capacitors are connected to V_{DD}, the supply voltage V_{S} is defined by

$$V_S = V_{DD} + (V_{\mathrm{REF}} - V_{CM}) \cdot 4C/12C = 1.4V \tag{6}$$

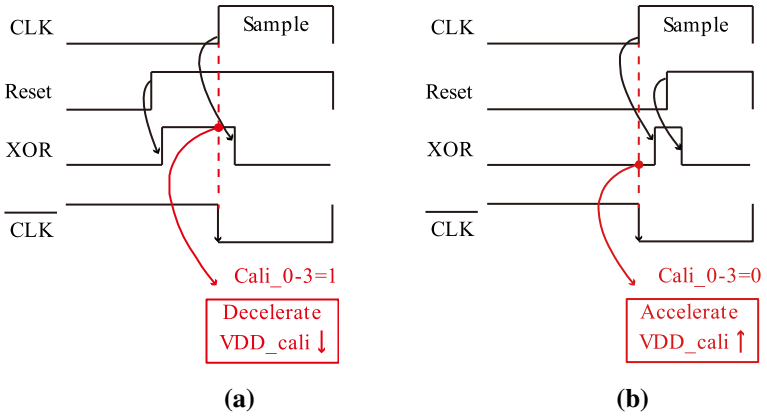


Fig. 12 Timing waveforms of relevant signals during the process of supply voltage calibration

When the calibration code is 1111, the bottom plates of the four unit capacitors are connected to Gnd, the supply voltage V_S is defined by

$$V_S = V_{DD} + (\text{Gnd} - V_{CM}) \cdot 4C/12C = 1.0V \tag{7}$$

3 Simulation Results

Figure 13 shows the layout of the proposed SAR ADC which is implemented in 40 nm CMOS process. The total layout area is 140um*85um. The supply voltage for the SAR ADC is 1.2 V and the power consumption is 2.59 mW. The proposed SAR ADC is designed to work at sampling rate of 500MS/s. Figure 14 gives the 4096 FFT result of the ADC with 245.605 MHz sinusoidal input signal. The proposed SAR ADC achieves 55.5 dB SFDR and 45.8 dB SNDR, which corresponding to ENOB = 7.32bit.

3.1 Background Offset Mismatch Calibration

Figure 15 illustrates the generation of rotation code for the background offset mismatch calibration. Once the falling edge of the control signal comes, the quantization results D_1D_0 of the (N-1)th period is sent to be the rotation code in the (N)th period. The simulated dynamic performance versus the input signal frequency is shown in Fig. 16, which also gives the results with and without background offset mismatch calibration. The size of input transistors for the comparator is 1.2u/40n. To test the

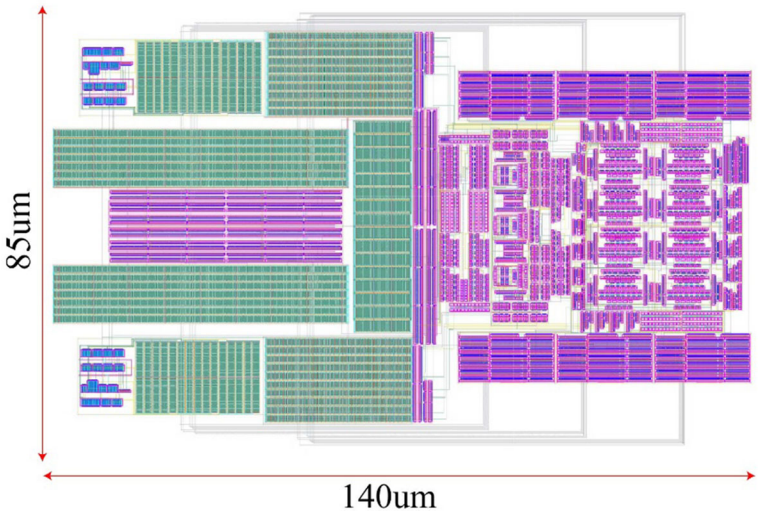


Fig. 13 Layout of the proposed SAR ADC

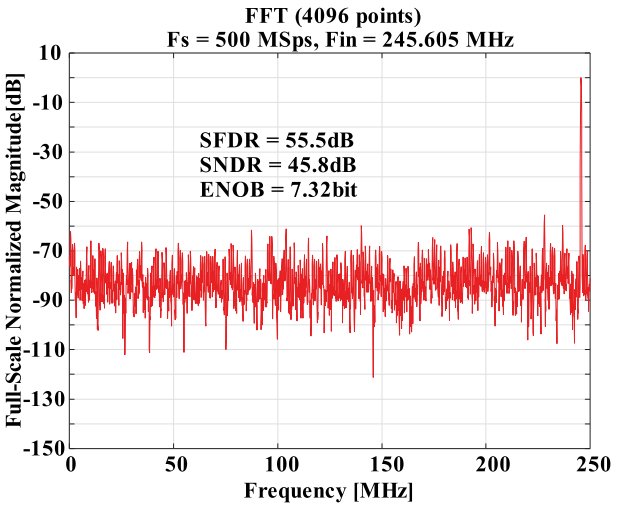


Fig. 14 Output spectrum of the proposed SAR ADC

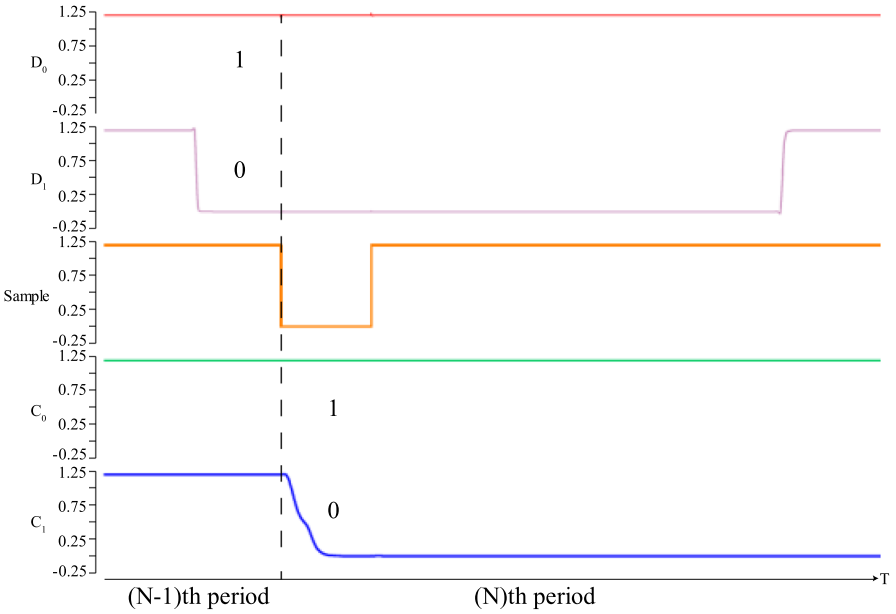


Fig. 15 Simulated waveform of background offset mismatch calibration

offset calibration, ± 20 nm mismatch has been added on the width of input transistors. From the simulation results, the effect of offset mismatch can be eliminated after calibration. Figure 17 gives the simulated output spectrums with/without background offset mismatch calibration.

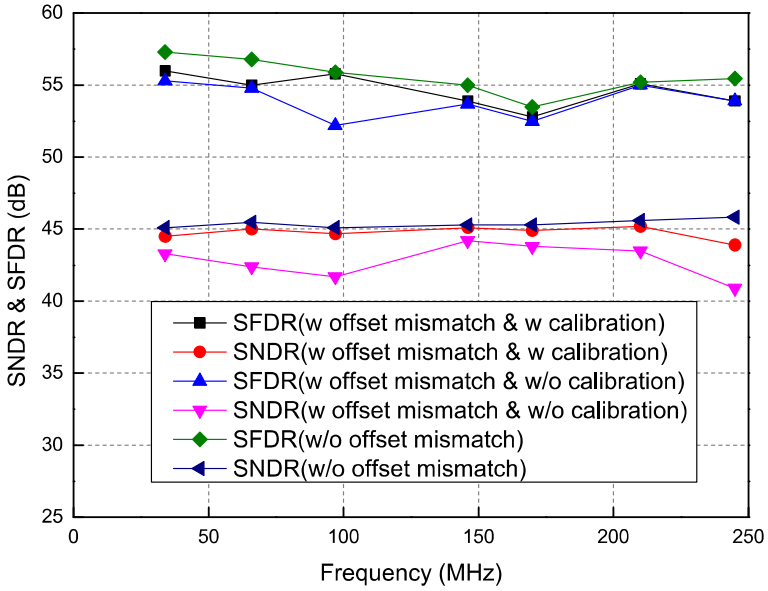
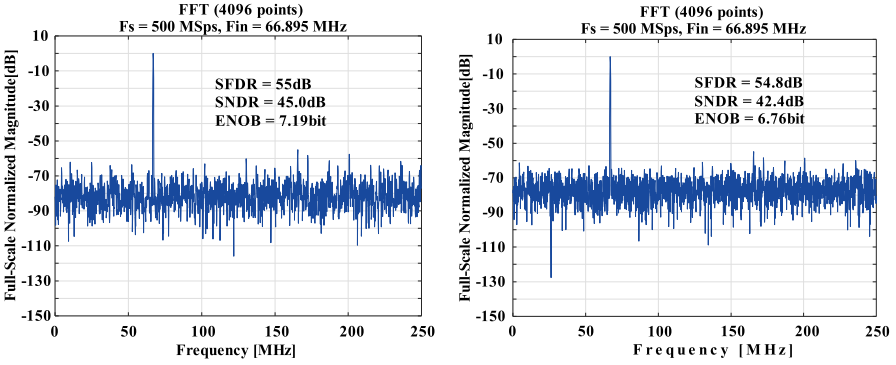


Fig. 16 Simulated results versus the input signal frequency with background offset mismatch calibration



(a) With calibration **(b)** Without calibration

Fig. 17 Simulated output spectrums with/without background offset mismatch calibration

3.2 Supply Voltage Calibration

Figure 18 gives the waveforms of supply voltage calibration at different corners. Figure 18a shows the simulation results at ss corner. The left part of Fig. 18a is the generation of calibration code Cali_0-3, which is set as '0000' according to the reset signal detection module. Then the calibration code controls the switches of calibration capacitor array to generate an increased VDD_cali, which is used to control

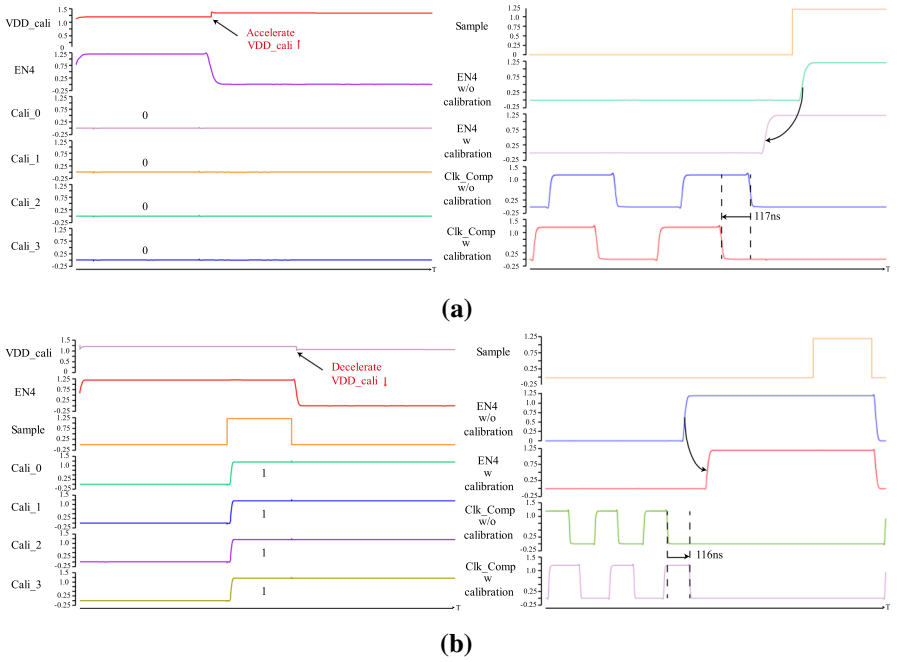


Fig. 18 Simulation waveforms of supply voltage calibration at different corners **a** ss corner **b** ff corner

the comparator and make it accelerate. The right part of Fig. 18a shows the waveforms of comparator with/without calibration. The waveforms of reset signal (EN4) and the clock of comparator (Clk_Comp) after calibration is 117 ns ahead of the signals without calibration. Figure 18b shows the simulation results at ff corner. The left part of Fig. 18b is the generation of calibration code Cali_0-3, which is set as '1111' according to the reset signal detection module. Then the calibration code controls the switches of calibration capacitor array to generate a decreased VDD_cali, which is used to control the comparator and make it decelerate. The right part of Fig. 18b shows the waveforms of comparator with/without calibration. The waveforms of EN4 and Clk_Comp after calibration is 116 ns later than the signals without calibration. According to the simulation results, the system can adjust the clock of the comparator under different process corners based on the supply voltage calibration.

Figure 19 gives results of the proposed ADC at different process corners with solid lines, which indicate that the dynamic performance at ss corner is improved apparently with voltage calibration. The simulation results with supply voltage calibration are given in Fig. 20. Figure 20a shows SNDR and SFDR at ss corner and Fig. 20b shows SFDR at different corners. As shown in Fig. 20a, the SFDR non-linearity reduces with increase in signal frequency at ss corner, especially when ADC without supply voltage calibration. This is because at ss corner the system works at a slow rate, especially the comparator. The poor performance of the comparator delays the generation of quantization results and reset signal, which affects the reset of the capacitors to the initial state before the next sampling clock. The variable performance of comparator results

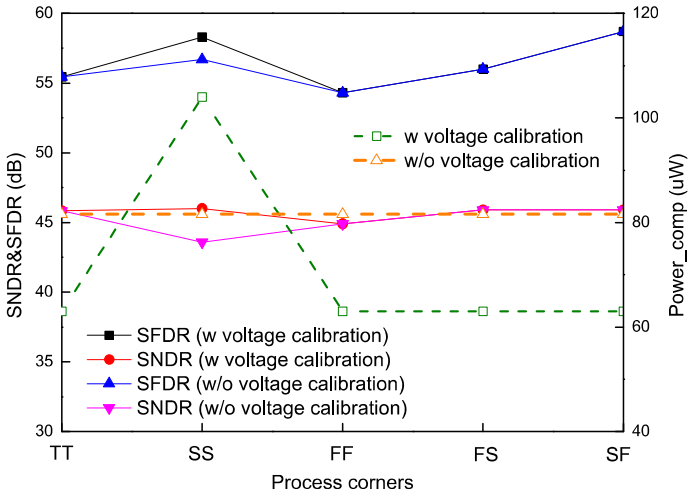


Fig. 19 Comparison of dynamic performance and power consumption with supply voltage calibration

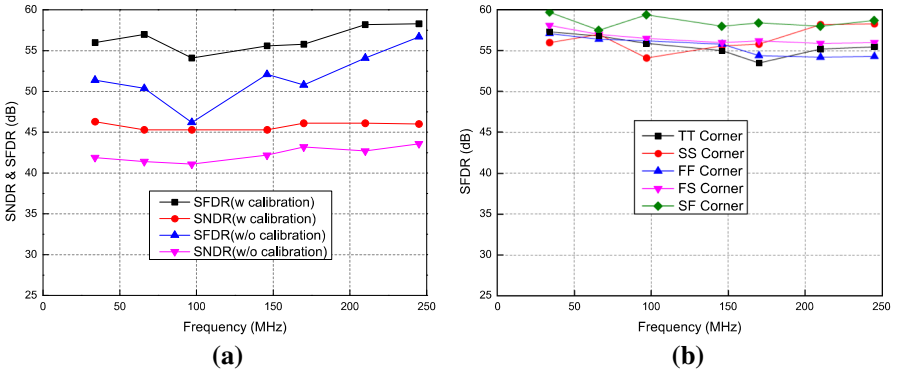


Fig. 20 Simulation results with supply voltage calibration **a** SNDR & SFDR at ss corner **b** SFDR at different corners

in performance degradation at some input frequencies due to incomplete conversion in asynchronous SAR ADC. After adding the calibration module, this phenomenon is somewhat alleviated. The dotted lines in Fig. 19 give the power consumption of comparator array with and without voltage calibration. The power consumption only increases at ss corner and reduces at other process corners.

3.3 Robustness to VT Variations and Linearity

Figure 21 gives the results versus temperature variation and supply voltage variation, which shows that the proposed ADC has good robustness to these variations. The DNL and INL of the proposed ADC are 0.65 LSB and 0.64 LSB, respectively, which are

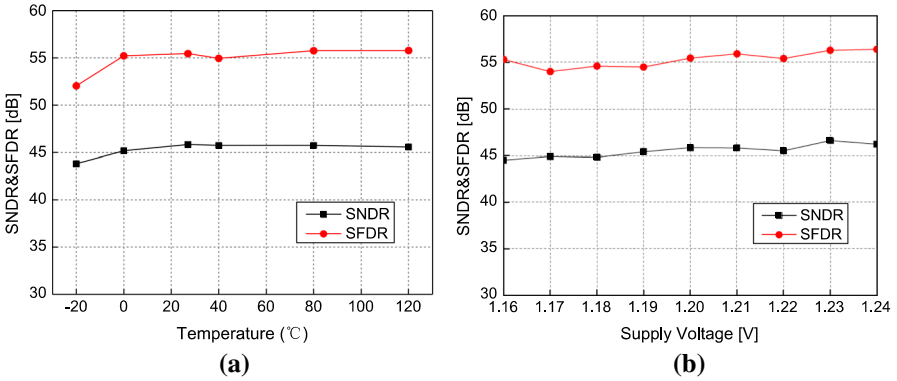


Fig. 21 Results of the proposed SAR ADC versus **a** temperature variation **b** supply voltage variation

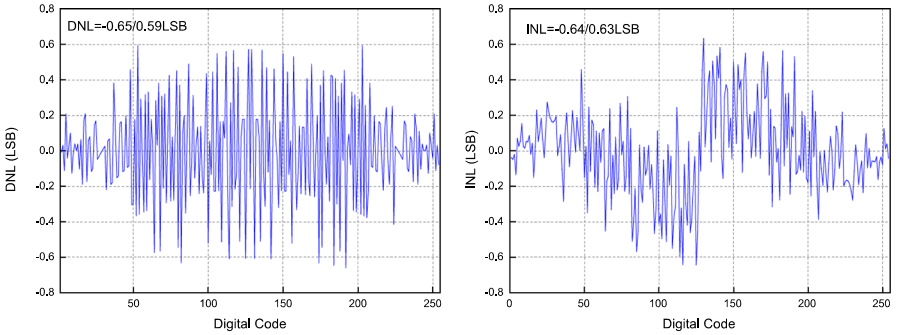


Fig. 22 Results of DNL and INL

shown in Fig. 22. Table 4 gives the comparison of the proposed work with pervious works.

3.4 Discussion of the Simulation Results

It is meaningful to have a discussion about the application conditions of the proposed multiple calibration techniques. The efficient 2b/cycle switching scheme are suitable for SAR ADCs with 2b/cycle structure, which saves switching energy and capacitor area. The background offset mismatch calibration technique can be applied to multi-bit/cycle SAR ADC. The hardware cost of the calibration module is related to the number of the comparators. The designers should pay attention to keeping a balance between the performance and hardware cost.

The application conditions of supply voltage calibration technique can be discussed from supply voltage and resolution two parts. Figure 23 shows a normalized delay of the comparator at different corners depending on the supply voltage. K_1 means that the delay at ss corner (Delay_ss) is divided by the delay that is required at tt corner

Table 4 Summary and performance comparison

	This work	[7]	[8]	[22]	[25]
Architecture	2b/cycle	Two-step	2b/cycle	2b/cycle	TI
Technology	40 nm	65 nm	45 nm	65 nm	65 nm
Resolution	8	8	7	8	7
Fs (MS/s)	500	1200	1000	400	700
Supply (V)	1.2	1.25	1.25	1.2	1.2
SNDR (dB)	45.8	43.7	40.8	44.5	40
Power (mW)	2.59	5	7.2	4	2.72
FoM (fJ/conv)	32	35	80	73	48

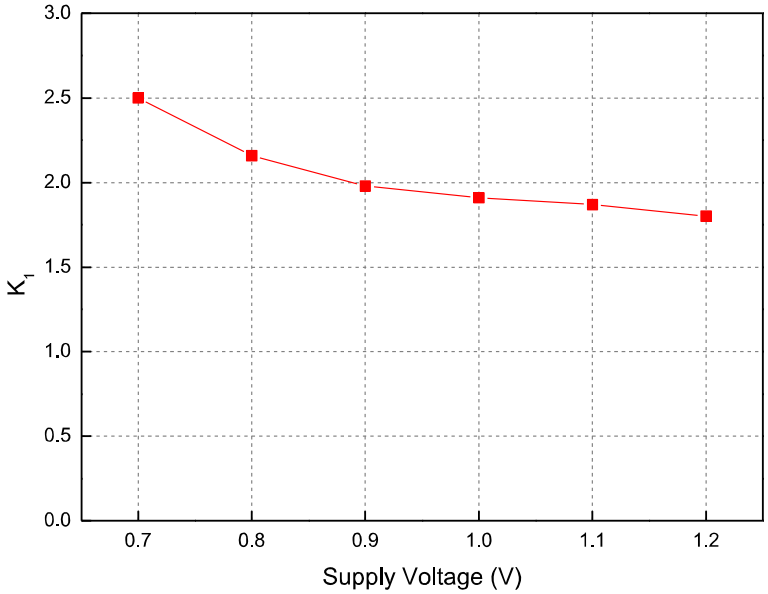


Fig. 23 Normalized delay with various supply voltages

(Delay_tt), which is defined by Eq. (8). K_1 is to show how the comparator works at the worst corner compared to the typical condition.

$$K_1 = \frac{\text{Delay\_ss}}{\text{Delay\_tt}} \tag{8}$$

The simulation is performed at both ss and tt corners with the same input value and same comparator clock, only changing the supply voltage of the comparator. As shown in Fig. 23, the value of K_1 increases as the supply voltage decreases. That is, the delay of ss corner becomes larger in comparison with that of tt corner as the supply

voltage decreases. The results indicate that the delay at worst corner with low supply voltage will be quite large and affect the speed of the comparator. The comparator is only one module of the SAR ADC, the signals need pass other modules and lots of logics during the conversion and will produce large delay at worst corner. Thus, the conversion time of the SAR ADC at ss corner will contain a large delay and become much longer than that at the tt corner with the decrease of supply voltage. The variations of conversion time will result in performance degradation due to incomplete conversion in asynchronous SAR ADC. From the point of supply voltage, the supply voltage calibration will have a more apparently improvement in SAR ADCs with low supply voltage.

Figure 24 gives the delay of the comparator compared to its speed, which is defined by K_2. The value of K_2 is given by Eq. (9), which represents the value of delay divided by one period of the comparator's clock.

$$K_2 = \frac{\text{Delay}}{T\_\text{comp}} \tag{9}$$

The simulation is performed at tt corner with the same input value and supply voltage, only changing the speed of the comparator. As shown in Fig. 24, delay becomes a larger part of a comparison cycle with the increase of comparator speed. The result indicates that the comparator for high-speed applications need to accelerate to reduce delay. In other words, high-speed or high-resolution (For ADCs with the same sampling speed, the comparators need to work faster for ADCs with higher resolutions.) SAR ADCs need supply voltage calibration, which will have a significant performance improvement.

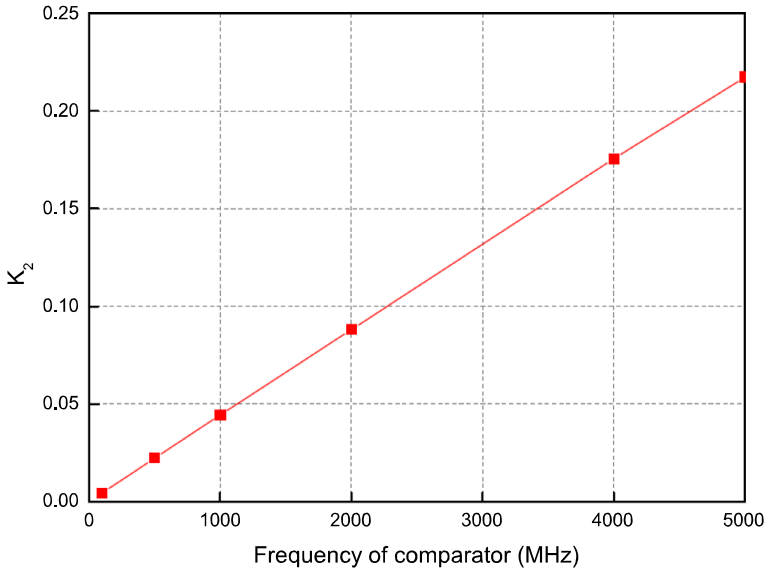


Fig. 24 The delay ratio of the comparator with various speeds

4 Challenges for Silicon Implementation

In the silicon implementation, parasitic capacitance will have an influence on the performance of SAR ADCs. The parasitic capacitance of the capacitor array will increase the charging and discharging time, affect the accuracy of DAC signal establishment, and increase the power consumption required by the switching activity of capacitor array. The parasitic capacitance at the input of the comparator will reduce its speed. The inconsistent parasitic capacitance at the input will also affect the comparison results and reduce the performance of the ADC. The parasitic capacitance of wires in the layout may have an impact on the speed of signal transmission and the matching of timing, and increase the power consumption at the same time.

5 Conclusion

A low power 2b/cycle SAR ADC with high consistency to PVT variations has been presented. The simulation results show that the proposed ADC achieves a SNDR of 45.8 dB and a SFDR of 55.5 dB for a near-Nyquist input with a power consumption of 2.59 mW. Thanks to several improvements introduced in this paper, the proposed SAR ADC shows high energy efficiency and good robustness to PVT variations.

Acknowledgements This work is supported by the Science and Technology on Low-Light-Level Night Vision Laboratory (No.61424120503162412005) and Wuhu and Xidian University special fund for industry-university-research cooperation (Project No.: XWYCXY-012020013-HT).

Data availability The datasets generated during and/or analyzed during the current study are available from the corresponding author on reasonable request.

Declaration

Conflict of interest The authors declare that they have no conflict of interest.

References

1. S. Babayan-Mashhadi, R. Lotfi, Analysis and design of a low-voltage low-power double-tail comparator. IEEE Trans. Very Large Scale Integr. VLSI Syst. **22**, 343–352 (2014)
2. B. Chen, M. Maddox, M.C.W. Coln, Y. Lu, L.D. Fernando, Precision passive-charge-sharing SAR ADC: analysis, design, and measurement results. IEEE J. Solid-State Circuits **53**, 1481–1492 (2018)
3. Y. Chen, J. Wang, H. Hu, F. Ye, J. Ren, A time-interleaved SAR assisted pipeline ADC with a bias-enhanced ring amplifier. IEEE Trans. Circuits Syst. II Exp. Briefs **65**, 1584–1588 (2018)
4. Z. Cao, S. Yan, Y. Li, A 32mW 1.25GS/s 6b 2b/step SAR ADC in 0.13μm CMOS. ISSCC Dig. Tech. Papers, pp. 542–543 (2008)
5. C. Chan, Y. Zhu, W. Zhang, U. Seng-Pan, R.P. Martins, A two-way interleaved 7-b 2.4-GS/s 1-then-2 b/cycle SAR ADC with background offset calibration. IEEE J. Solid-State Circuits **53**, 850–860 (2018)
6. B.P. Ginsburg, A.P. Chandrakasan, An energy-efficient charge recycling approach for a SAR converter With capacitive DAC. In: 2005 IEEE International Symposium on Circuits and Systems. **1**, pp. 184–187 (2005)
7. H. Huang, L. Du, Y. Chiu, A 1.2-GS/s 8-bit two-step SAR ADC in 65-nm CMOS with passive residue transfer. IEEE J. Solid-State Circuits **52**, 1551–1562 (2017)

8. H. Hong, W. Kim, H. Kang, S. Park, M. Choi, H. Park, S. Ryu, A decision-error-tolerant 45 nm CMOS 7b 1 GS/s nonbinary 2b/cycle SAR ADC. IEEE J. Solid-State Circuits **50**, 543–555 (2015)
9. H. Huang, H. Xu, B. Elies, Y. Chiu, A non-interleaved 12-b 330-MS/s pipelined-SAR ADC with PVT-stabilized dynamic amplifier achieving sub-1-dB SNDR variation. IEEE J. Solid-State Circuits **52**, 3235–3247 (2017)
10. H. Jeon, Y.-B. Kim, A CMOS low-power low-offset and high-speed fully dynamic latched comparator. International SoC Conference (SoCC). In: IEEE Proceeding, pp. 285–288 (2010)
11. L. Kull et al., A 3.1mW 8b 1.2GS/s single-channel asynchronous SAR ADC with alternate comparators for enhanced speed in 32 nm digital SOI CMOS. ISSCC Dig. Tech. Papers, pp. 468–470 (2013)
12. J. Kim, T. Yoo, D. Jung, D. Yoon, K. Seong, T. Kim, K. Baek, A 0.5 V 8–12 Bit 300 KSPS SAR ADC with adaptive conversion time detection-and-control for high immunity to PVT variations. IEEE Access **8**, 101359–101368 (2020)
13. C.C. Liu, S.J. Chang, G.Y. Huang, Y.Z. Lin, A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure. IEEE J. Solid-State Circuits **45**, 731–740 (2010)
14. W. Lin, T. Kuo, A compact dynamic-performance-improved current-steering DAC ith random rotation-based binary-weighted selection. IEEE J. Solid-State Circuits **47**, 444–453 (2012)
15. J. Luo, Y. Liu, J. Li, N. Ning, K. Wu, Z. Liu, Q. Yu, A low voltage and low power 10-bit non-binary 2b/cycle time and voltage based SAR ADC. IEEE Trans. Circuits Syst. I Reg. Pap. **67**, 1136–1148 (2020)
16. D. Li, J. Liu, H. Zhuang, Z. Zhu, Y. Yang, N. Sun, A 7b 2.6mW 900MS/s Nonbinary 2-then-3b/cycle SAR ADC with Background Offset Calibration. IEEE CICC, pp. 1–4 (2019)
17. K. Ragab, N. Sun, A 1.4mW 8b 350MS/s loop-unrolled SAR ADC with background offset calibration in 40nm CMOS. IEEE ESSCIRC, pp. 417–420 (2016)
18. V. Savani, N.M. Devashrayee, Design and analysis of low-power high-speed shared charge reset technique based dynamic latch comparator. Microelectron. J. **74**, 116–126 (2018)
19. D. Shinkel, E. Mensink, E. Klumperink, E. van Tuijl, B. Nauta, A double-tail latch-type voltage sense amplifier with 18ps Setup+Hold time. IEEE ISSCC Dig. Tech. Papers, pp. 314–315 (2007)
20. M. van Elzakker, et al., A 1.9 uW 4.4fJ/conversion-step 10b 1MS/s charge-redistribution ADC. IEEE ISSCC Dig. Tech. Papers, pp. 244–245 (2008)
21. S. Wong, U. Chio, C. Chan, H. Choi, S. Sin, Seng-Pan U, R. P. Martins, A 4.8-bit ENOB 5-bit 500MS/s binary-search ADC with minimized number of comparators. IEEE ASSCC, pp. 73–76 (2011)
22. H. Wei, C. Chan, U. Chio, S. Sin, Seng-Pan U, R. P. Martins, F. Maloberti, A 0.024mm^2 8b 400MS/s SAR ADC with 2b/cycle and resistive DAC in 65nm CMOS. ISSCC Dig. Tech. Papers, 188–190 (2011)
23. H. Wang, W.M. Xie, Z.X. Chen, S.J. Cai, A capacitor-splitting switching scheme with low total power consumption for SAR ADCs. J. Circuits Syst. Comput. **28**, 1920002 (2018)
24. H. Xu, H. Huang, Y. Cai, L. Du, Y. Zhou, B. Xu, D. Gong, J. Ye, Y. Chiu, A 78.5-dB SNDR radiation- and metastability-tolerant two-step split SAR ADC operating up to 75 MS/s with 24.9-mW power consumption in 65-nm CMOS. IEEE J. Solid-State Circuits **54**, 441–451 (2019)
25. D. Xing, Y. Zhu, C. Chan, S. Sin, F. Ye, J. Ren, U. Seng-Pan, R.P. Martins, Seven-bit 700-MS/s four-way time-interleaved SAR ADC with partial Vcm-based switching. IEEE Trans. Very Large Scale Integr. VLSI Syst. **25**, 1168–1172 (2017)
26. C. Yuan, Y. Lam, Low-energy and area-efficient tri-level switching scheme for SAR ADC. Electron. Lett. **48**, 482–483 (2012)
27. Y. Zhu, C.H. Chan, U.F. Chio, S.W. Sin, U. Sweng-Pan, R.P. Martins, F. Maloberti, A 10-bit 100-MS/s reference-free SAR ADC in 90 nm CMOS. IEEE J. Solid-State Circuits **45**, 1111–1121 (2010)
28. H.Y. Zhuang, W.J. Guo, J.X. Liu, H. Tang, Z. Zhu, L. Chen, N. Sun, A second-order noise-shaping SAR ADC with passive integrator and tri-level voting. IEEE J. Solid-State Circuits **54**, 1636–1647 (2019)
29. Y. Zhou, B. Xu, Y. Chiu, A 12 bit 160 MS/s two-step SAR ADC with background bit-weight calibration using a time-domain proximity detector. IEEE J. Solid-State Circuits **50**, 920–931 (2015)

30. Y. Zhou, B. Xu, Y. Chiu, A 12-b 1-GS/s 31.5-mW time-interleaved SAR ADC with analog HPF-assisted skew calibration and randomly sampling reference ADC. IEEE J. Solid-State Circuits **54**, 2207–2218 (2019)
31. Z. Zhu, Y. Xiao, X. Song, V_{CM}-based monotonic capacitor switching scheme for SAR ADC. Electron. Lett. **49**, 327–329 (2013)