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Design of Memristor-Based Combinational Logic Circuits

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Abstract

This paper proposes three modified memristor ratioed logic (MRL) gates: NOT, NOR and A AND (NOR B) (i.e., $A \cdot \bar{B}$), each of which only needs 1 memristor and 1 NMOS. Based on the modified MRL gates, we design some combinational logic circuits, including 1-bit comparator, 3-bit binary encoder, 3-bit binary decoder and 4:1 multiplexer. Furthermore, an improved multifunctional logic module is proposed, which contains one NMOS transistor and five memristors, and can implement AND, OR and XOR logic operations. Using this multifunctional logic module, a 4-bit comparator and a 1-bit full adder are designed. Finally, the proposed combinational logic circuits are verified by LTSPICE simulations. Compared with other memristor-based logic circuits and the traditional CMOS technology, the proposed logic circuits have made great progress in reducing delay, power consumption and the number of transistors.

Keywords Memristor · Digital logic circuits · Combinational logic circuits

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1 Introduction

In the past decades, the number of transistors per unit area of chips has been growing rapidly, almost doubling every two years according to Moore's law. However, the Moore's law is being challenged with the limitations of transistors in physical materials, energy consumption and economy [4]. In order to continue Moore's law, many ideas have been put forward, one of which is to find a smaller component instead of the conventional transistor. Professor Chua put forward the concept of memristor in 1971 [3], and then HP Lab realized the first nanoscale memristor in 2008 [16]. The emergence of memristors provides a new way for the continuation of Moore's law.

With the advent of memristors, the research on memristor and its applications has become a hot topic. Among them, the memristor-based logic circuits have received extensive attention. At present, memristor-based logic circuits can be divided into the following aspects:

1. Pure memristors based logic circuits: Memristor-aided Logic (MAGIC) [6] and Material Implication (IMPLY) Memristor Logic [18].
2. Hybrid memristor-/CMOS-based logic circuits: combination of memristor and CMOS components in Boolean logic [7].
3. Memristors based crossbar: logic operations in crossbar arrays relaying on programmable nanowire interconnections [11, 20, 24].

The MAGIC cannot realize cascade connection between multiple logic gates and multiple fan-outs due to its structure. The IMPLY requires multiple operation steps, which prolongs the operation time of the circuit. The memristor ratioed logic (MRL) composed of CMOS transistors is not as good as the former two in reducing occupancy area, but memristors and CMOS transistors can be well compatible, i.e., What's more, memristors can be manufactured on the metal layer of CMOS technology [7]. Therefore, compared with the traditional CMOS logic circuit, the MRL not only reduces the occupancy area of components on the chip, but also greatly improves the operation speed of the logic circuits.

The research of logic circuits based on MRL mainly involves XOR (XNOR) gates: XOR gate composed of 4T–1M (four CMOS transistors and one memristor) [25], XOR (XNOR) gate composed of 3T–4M [21], new type of XOR (XNOR) gate composed of 1T–4M–1R (one transistor, four memristors and one resistor) [23], and XOR (XNOR) gate composed of 2T–4M–1R [19]. Existing full adders include 16T–18M full adder based on MRL [14], 27T–2M full adder based on 4T–1M XOR gate [21], 12T–12M full adder based on new XOR gate 1T–4M–1R [23], 15T–12M–2R full adder based on 2T–4M-1R XOR gate [2] and 15T–15M new full adder based on 3T–3M XNOR gate [13] In addition, a 2-bit binary multiplier [17] based on general logic gates (a 2T–4M circuit with XOR plus AND) was proposed.

At present, memristor-based logic circuits mainly involve the research of full adder [12], multiplier, XOR, XNOR, etc. There is little research on other combinational logic circuits such as encoder, decoder, and multiplexer. Based on the new MRL and the improved multifunctional logic module, this paper designs a series of combinational

logic circuits: 1-bit full adder, 3-bit binary encoder, and line decoder; 1-bit and 4-bit comparator and improving 1T–4M–1R XOR gate to 1T–5M XOR gate based on a 6T–16M 1-bit full adder which is designed.

Based on the memristor ratioed logic (MRL) gates [7], this paper designed three modified MRL gates, i.e., NOT, NOR and A AND (NOR B), each of which only needs 1 memristor and 1 NMOS. Furthermore, using the modified MRL gates, we also designed a new multifunctional logic module, which uses only 5 memristors and 1 NMOS transistor to achieve both XOR and AND functions. Finally, based on the proposed modified logic gate circuits, we designed a 3:8 encoder, 8:3 decoder, and 4 out of 1 data selector, as well as the multifunctional logic module based 1-bit full adder and 4-bit value comparator. LTSPICE simulations and performance comparison analysis show that the proposed combinational logic circuits possess the characteristic of low power consumption, low delay and fewer circuit components.

In this paper, a general memristor model is introduced in Sect. 2. The basic logic gates and a novel XOR and AND multifunctional logic module are introduced in Sect. 3. Section 4 describes the design of combinational logic circuits constructed by basic logic circuits which is presented in Sect. 3. In Sect. 5, LTSPICE simulation results are given, and the performance of the designed combinational logic circuit is analyzed. The conclusion is given at last.

2 Model of Memristor

The memristor model used in this paper can simulate a variety of actual memristors, and different memristor characteristics can be achieved by setting different parameters [10, 22]. Compared with other memristor models, the convergence problem of this model is also greatly improved. Furthermore, this model can realize accurate signal outputs with 256 memristors in a combinational logic circuit. For matching to the relationship of memristor voltage and current, the model based on three different characteristics of the actual memristor is established for the metal-insulated-metal structure memristor:

$$I(t) = \begin{cases} a_1 x(t) \sinh(bV(t)), & V(t) \geq 0 \\ a_2 x(t) \sinh(bV(t)), & V(t) < 0 \end{cases} \tag{1}$$

where $I(t)$ and $V(t)$ are the current and voltage of the memristor; a_1, a_2 and b are constants and $x(t)$ satisfies the state equation:

$$\frac{\mathrm{d}x}{\mathrm{d}t} = \eta g(V(t)) f(x(t)) \tag{2}$$

where η denotes the polarity of the applied voltage. $\eta = 1$ (resp., $\eta = -1$) means that the positive (resp., negative) voltage is applied to the memristor. Threshold functions $g(V(t))$ and $f(x(t))$ are as follows:

$$g(V(t)) = \begin{cases} A_p\left(e^{V(t)} - e^{V_p}\right), & V(t) > V_p \\ -A_n\left(e^{-V(t)} - e^{V_n}\right), & V(t) < -V_n \\ 0 & -V_n \le V(t) \le V_p \end{cases} \tag{3}$$

$$f(x) = \begin{cases} e^{-\partial_p(x-x_p)} w_p\left(x, x_p\right), & x \ge x_p \\ 1, & x < x_p \end{cases} \tag{4}$$

$$f(x) = \begin{cases} e^{\partial_n(x+x_n-1)} w_n\left(x, x_n\right), & x \le 1 - x_n \\ 1, & x > 1 - x_n \end{cases} \tag{5}$$

where A_p and A_n are adjustable amplitudes, V_p and V_n are positive and negative threshold voltages, respectively; $w_p\left(x, x_p\right)$ and $w_n\left(x, x_n\right)$ are window functions, which can be expressed as follows:

$$w_p\left(x, x_p\right) = \frac{x_p - x}{1 - x_p} + 1 \tag{6}$$

$$w_n\left(x, x_n\right) = \frac{x}{1 - x_n} \tag{7}$$

where x_p and x_n are the state values corresponding to the voltages V_p and V_n, respectively. The window function $w_p\ (x,\ x_p)$ is to ensure $f(x) = 0$ when $x(t) = 1$, and the window function $w_n(x,\ x_n)$ is to ensure that the value of $x(t)$ is not less than zero when the current is reversed. The general memristor model used in this paper can simulate the silver-chalcogenide memristor in Ref. [2].

Figure 1 shows the symbol of a memristor. When a positive voltage V_p is applied to the memristor, the resistance of the memristor decreases to R_{ON}; while a negative voltage V_n is applied to the memristor, the memristor resistance increases to R_{OFF}. The memristor model can be used as a binary memory, with R_{ON} representing the binary "1" and R_{OFF} representing the binary "0". Figure 2 shows the *I*–*V* hysteresis loop of the memristor.

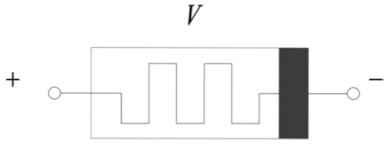


Fig. 1 Symbol of the memristor

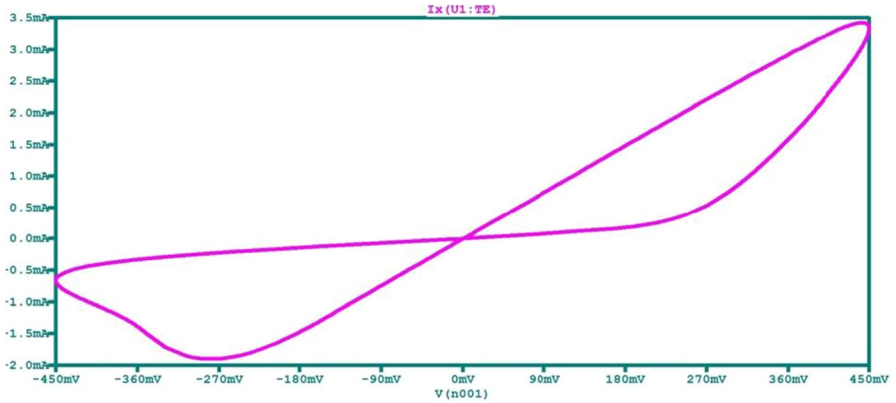


Fig. 2 *I–V* hysteresis loop of the memristor

3 Logic Gate Circuits Based on Memristor Ratioed Logic

Reference [7] first proposed OR gate and AND gate circuits using memristors, as shown in Fig. 3a, b. Here, we quantify the high voltage (V_{high}) to the binary state "1" and the low voltage (V_{low}) to the binary state "0." For the OR gate, when the input voltage signals are $V_{IN\_1} = V_{high} = 1$ and $V_{IN\_2} = V_{low} = 0$, this leads to the memristor at end 1 exhibits low resistance R_{ON}, while the memristor at end 2 exhibits high resistance R_{OFF}, and the output can be expressed as:

$$V_{OUT} = \frac{R_{OFF}}{R_{ON} + R_{OFF}} V_{high} \approx V_{high} = 1 \tag{8}$$

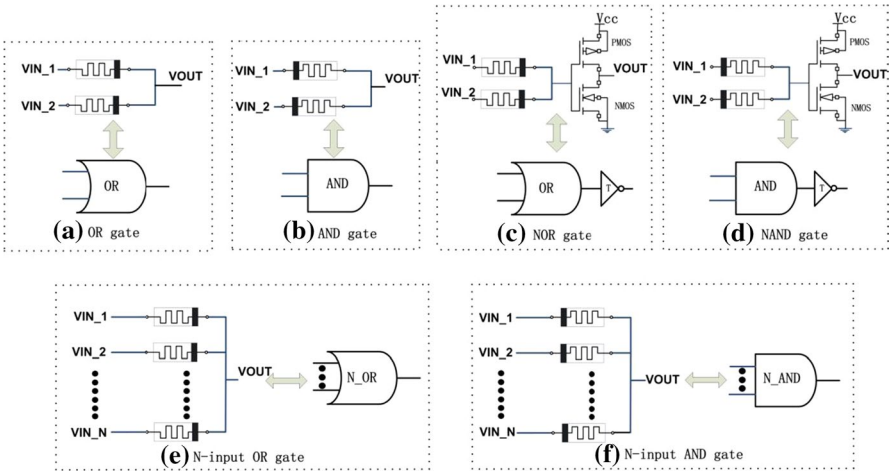


Fig. 3 The OR, AND, NOR, NAND gates constructed by memristors

Similarly, when the input signals at both ends of the OR gate are "1, 1," "0, 0" and "0, 1," the outputs are "1," "0" and "1," respectively.

The AND gate can be verified by the same way. However, because of the output signals in the OR and AND gate circuits are obtained by the voltage dividers, the output signals will fade to some extent. Observe from Eq. (8) that the output voltage is approximately equal to "1" of high voltage, where although the small voltage attenuation does not have a direct impact on single AND gate or OR gate logic circuit, it will have a significant impact in combinational logic circuits, when multiple AND or OR gates are needed. Therefore, a CMOS inverter is usually added behind an OR gate or an AND gate to form a NOR and a NAND to boost the signals, as shown in Fig. 3c, d. Figure 3e, f shows the N inputs OR gate and the N inputs AND gate, respectively. Generally, CMOS inverters need to be added to boosting the signal when they are used in combinational logic circuits.

In Kvatinsky's paper on memristor ratioed logic, he did not propose how to construct Boolean logic's NOT logic. Therefore, when designing combinational logic circuits based on memristors, researchers mostly use CMOS inverters instead of NOT gates, which to some extent increases the area of chips. Ref. [13] presented a NOT gate circuit constructed by one memristor and one NMOS transistor, as shown in Fig. 4a, which is actually an inverting amplifier. The NOT gate circuit is connected to a DC voltage V_{CC} at the front end of the memristor, where V_{IN} is set as the input signal and V_{OUT} is regarded as the output signal. When $V_{IN} = 1$ (the input signal is high voltage), which causes the transistor to turn on, the memristor is biased forward with the memristance value is $R_M = R_{ON}$. At this time, the NMOS is saturated with the on-resistance $R_T \approx 0$, and the output is given as follows:

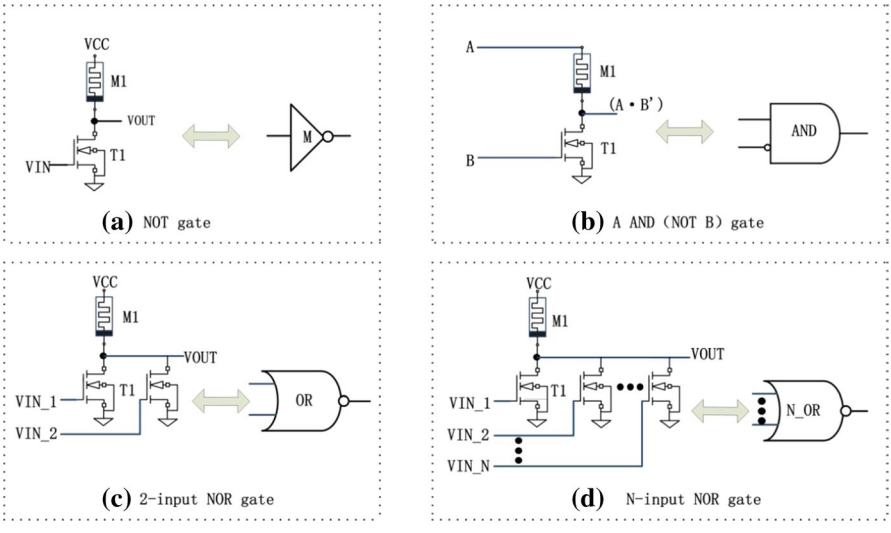


Fig. 4 New basic logic circuits based on memristor ratioed logic

$$V_{\mathrm{OUT}} = \frac{R_T}{R_{\mathrm{ON}} + R_T} V_{\mathrm{CC}} \approx 0 \tag{9}$$

When $V_{\mathrm{IN}} = 0$, which causes the transistor to cut off, the $R_T \approx \infty$ and the output is given as follows:

$$V_{\mathrm{OUT}} = \frac{R_T}{R_{\mathrm{ON}} + R_T} V_{\mathrm{CC}} \approx 1 \tag{10}$$

Furthermore, if the DC bias voltage V_{CC} is used as the input signal A, we can obtain the logic $A \cdot \bar{B}$, as shown in Fig. 4b. When $A = 1$ and $B = 1$, memristor M1 and the transistor T1 exhibit low memristance R_{ON} and low resistance $R_T \approx 0$, respectively, which lead to $V_{\mathrm{OUT}} = 0$, implementing the logic $A \cdot \bar{B} = 0$.When $A = 0$, i.e., the transistor T1 is unbiased, the transistor cuts off regardless of the input signal B = 1 or B = 0, which also lead to $V_{\mathrm{OUT}} = 0$, i.e., the logic $A \cdot \bar{B} = 0$.

Figure 4c, d shows the NOR with two-input and N inputs. In Fig. 4c, when $V_{\mathrm{IN1}} = V_{\mathrm{IN2}} = 1$, the two transistors turn on, leading to the output voltage $V_{\mathrm{OUT}} = 0$ and implementing the logic NOR: $\overline{V_{\mathrm{IN1}} + V_{\mathrm{IN2}}} = 0$., while when $V_{\mathrm{IN1}} = V_{\mathrm{IN2}} = 0$, the two transistors cut off, leading to the output voltage $V_{\mathrm{OUT}} = V_{\mathrm{CC}}$ and implementing the logic NOR: $\overline{V_{\mathrm{IN1}} + V_{\mathrm{IN2}}} = 1$. Similarly, we can get the other two logical relations of NOR for $V_{\mathrm{IN1}} = 1$ and $V_{\mathrm{IN2}} = 0$, and $V_{\mathrm{IN1}} = 0$ and $V_{\mathrm{IN2}} = 1$.

In the process of building combinational logic circuits based on this new memristor ratioed logic, a lot of components can be saved.

In digital logic circuits, besides basic logic gates (AND, OR and NOT), NAND, NOR, XOR and XNOR are often used as basic logic circuit modules. Reference [25] proposes a new logic circuit module (1T–4M–1R) consisting of 1 CMOS transistor, 4 memristors and 1 resistor, which can realize both XOR and AND outputs simultaneously. This circuit structure can not only reduce the use of transistors, but also improve the operation speed and reduce power consumption. However, there is a disadvantage of this structure, that is, it must use a large resistance, which usually occupies a large amount of precious area of the chip for micron-level chips. Aim to this problem, this paper proposes an improved logic module (1T–5M) composed of 1 NMOS transistor and 5 memristors, as shown in Fig. 5. The right sub-circuit (composed of M5 and T1) realizes the logic of $V_B \cdot \overline{V_A}$; M1 and M2 realize the logic $V_A = X_1 \cdot X_2$ (Fig. 3); and M3 and M4 realize the logic $V_B = X_1 + X_2$ (Fig. 3). The principle of this circuit can be expressed by the following equations:

$$V_A = X_1 \cdot X_2, \quad V_B = X_1 + X_2. \tag{11}$$

$$V_{\mathrm{XOR}} = \overline{V_A} \cdot V_B = \overline{\left(X_1 \cdot X_2\right)} \cdot \left(X_1 + X_2\right) = X_1 \oplus X_2. \tag{12}$$

The above is basic logic circuits based on which we can design some combinational logic circuits.

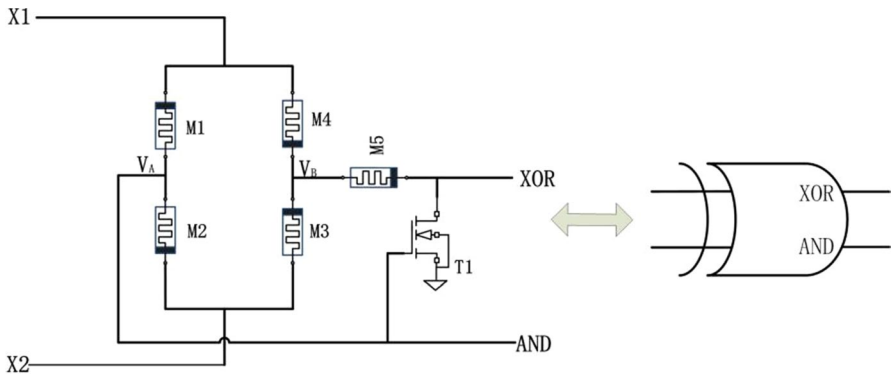


Fig. 5 The XOR and AND multifunctional logic module

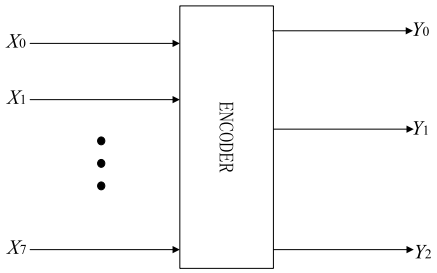
4 Memristor-Based Combinational Logic Circuits

Conventional memristor ratioed logic is usually composed of two memristors and two CMOS transistors. Reference [9] proposes the new memristor ratioed logic based on one memristor and one NMOS to design combinational logic circuits. Compared with conventional memristor ratioed logic, the output signal of the new memristor ratioed logic is obtained not by dividing the input voltage, but by the saturation voltage and cut-off voltage of the NMOS transistor that is controlled by the high and low input voltages of the NMOS grid terminal, as shown in Fig. 4b. Therefore, the new memristor ratioed logic can achieve the accurate output of the signal without adding the inverter at the output to boost the signal. Compared with the traditional CMOS technology, the new memristor ratioed logic can not only reduce the number of components used, but also greatly reduce the power consumption and improve the operation speed of whole circuit due to the reduction of the CMOS transistors.

In this section, we use two ways to design combinational logic circuits. Using the new MRL, we design a 3-bit binary encoder, a 3-bit binary decoder, a 4:1 multiplexer and a 1-bit comparator. Based on the new MRL and the multifunctional logic module (1T–5M) proposed in this paper, a 1-bit full adder (6T–16M) and a 4-bit comparator are designed.

4.1 Memristor-Based Encoder

In digital logic circuit systems, information (numbers or symbols) with specific meanings are usually coded into corresponding bits of binary code. The circuit that realizes the encoding function is called the encoder. Its characteristic is that when one of the input terminals is an effective level, the output terminal of the encoder outputs the corresponding multi-bit binary code in parallel. The circuit encoding $M = 2^n$ signals with N-bit binary code is called binary encoder. Figure 6a, b shows block diagrams of 3-bit binary coders and corresponding



(a)

X_0	X_1	X_2	X_3	X_4	X_5	X_6	X_7	Y_2	Y_1	$Y0$
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

(b)

Fig. 6 Block diagram and truth table of the 3-bit binary encoder

input–output truth tables, respectively. The relationship between input and output can be obtained from the truth table.

$$\begin{aligned} Y_2 &= X_4 + X_5 + X_6 + X_7 \\ Y_1 &= X_2 + X_3 + X_6 + X_7 \\ Y_0 &= X_1 + X_3 + X_5 + X_7 \end{aligned} . \tag{13}$$

According to the relationship between input and output, a 3-bit binary encoder combinational logic circuit can be constructed by using the new MRL, as shown in Fig. 7, in which X_1–X_7 are input signals, and Y_0, Y_1 and Y_2 are output signals. M1, T1, T4, T5 and T6 constitute a four-input NOR gate. The input signals X_1, X_3, X_5 and X_7 pass through the NOR gate, and the signal at the gate of the transistor T13 is $\overline{X_1 + X_3 + X_5}$. Then, the output signal of the NOT gate (M4, T13) is $Y_0 = X_1 + X_3 + X_5 + X_7$. Similarly, the output signals Y_1 and Y_2 that are shown in Eq. 13 are obtained by using the same way.

In Fig. 7, the 3-bit binary encoder contains only 15 NMOS transistors and 6 memristors by using the new MRL, while the traditional CMOS technology requires at least 40 transistors for implementing the same encoder [1].

4.2 Memristor-Based Decoder

The process of translating binary codes with specific meanings into numbers or characters is called decoding, and the circuit that implements the decoding operation is called decoder. Decoder is a multi-input, multi-output combinational logic circuit, which can be divided into different decoders according to its functions. The binary decoder has n input terminals and 2^n output terminals. The function of binary decoder is just the opposite of that of binary encoder. It identifies different binary codes with specific meanings and converts them into corresponding level signals. Figure 8 shows a block diagram of a 3-bit binary decoder and a truth table. The input–output relationship can be obtained:

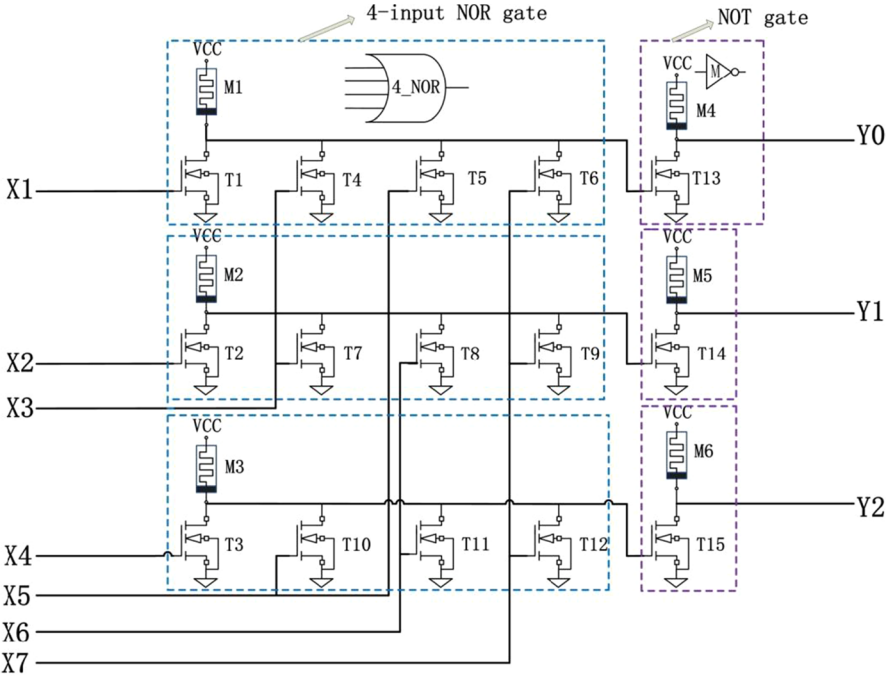
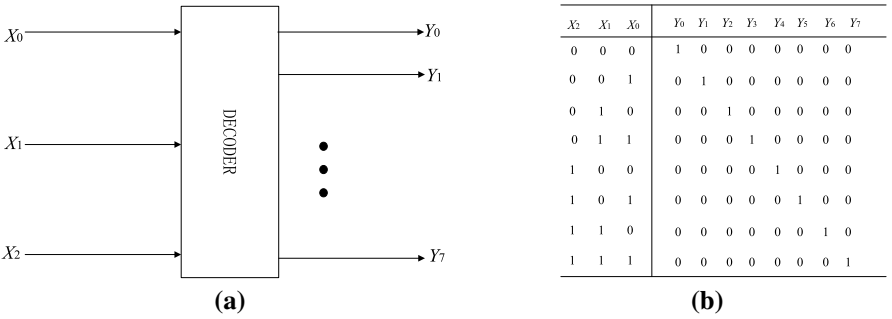


Fig. 7 3-bit binary encoder



X_2	X_1	X_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Fig. 8 Block diagram and truth table of the 3-bit binary decoder

$$
\begin{aligned}
Y_0 &= \overline{X_2 X_1 X_0}, \quad Y_1 = \overline{X_2 X_1} X_0, \quad Y_2 = \overline{X_2} X_1 \overline{X_0} \\
Y_3 &= \overline{X_2} X_1 X_0, \quad Y_4 = X_2 \overline{X_1 X_0}, \quad Y_5 = X_2 \overline{X_1} X_0 \\
Y_6 &= X_2 X_1 \overline{X_0}, \quad Y_7 = X_2 X_1 X_0
\end{aligned} \tag{14}
$$

The 3-bit binary decoder constructed by the new MRL is shown in Fig. 9, where the module circuit corresponding to each output is a 2-input NOR gate circuit. The

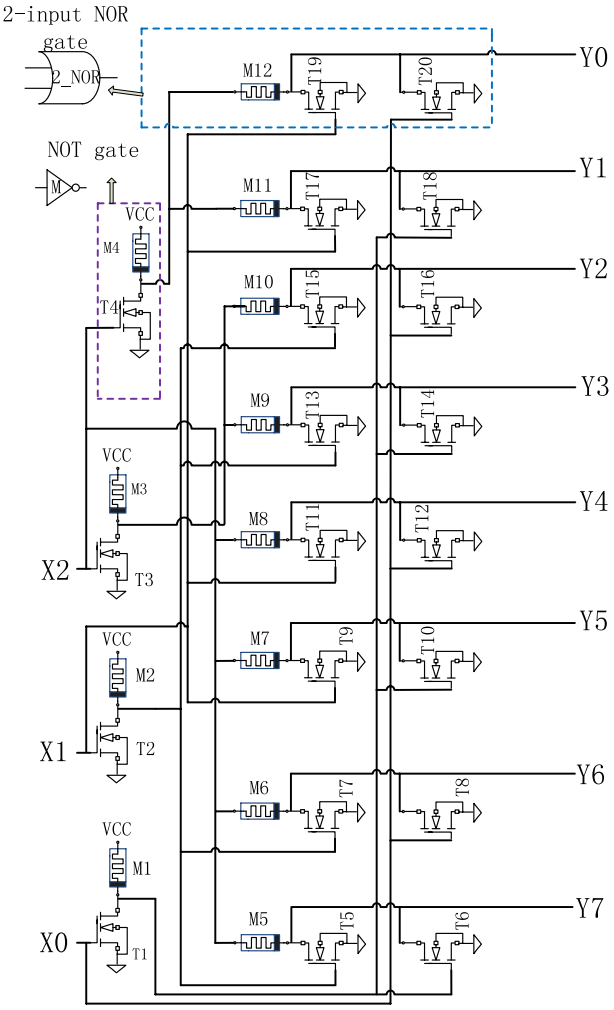


Fig. 9 3-bit binary decoder

input signals are X_2, X_1, X_0 and the output signals are $Y_0 \sim Y_7$. In the circuit, M_4–T_4, M_3–T_3, M_2–T_2 and M_1–T_1 constitute four inverters, which are used to reverse the input signals X_2, X_1 and X_0.

In Fig. 9, M12, T19 and T20 form a 3-input NOR gate, which is obtained by taking the DC voltage V_{CC} in Fig. 4c as an input (i.e., $\bar{X}_2$) from the drain of transistor T4 (the other two inputs are X_1 and X_0). Therefore, only when the input signal is logic 1, i.e., $\bar{X}_2 = 1$, the 3-input NOR logic, $\overline{X_1 + X_0}$, can be realized, while when the input signal is 0, the output is always 0. Hence, we obtain the logic $Y_0 = \overline{X_2} \cdot \overline{X_1 + X_0} = \overline{X_2 X_1 X_0}$, as shown in Eq. 14. For the output Y_1, where M11-T17- T18 also form a 3-input NOR gate, whose inputs are $\bar{X}_2$ X_1 and $\bar{X}_0$, and the output Y_1 is $Y_1 = \overline{X_2} \cdot X_1 + \bar{X}_0 = \overline{X_2 X_1 X_0}$.

Similarly, the logical expressions of output signals Y_2-Y_7 described by Eq. 14 can be obtained in the same way, such as $Y_7 = X_2 \cdot \bar{X}_1 + \bar{X}_0 = X_2X_1X_0$. Compared with the traditional CMOS technology, which requires at least 70 transistors to construct a 3-bit binary decoder [1], only 20 NMOS transistors and 12 memristors are needed in this decoder circuit by using the new MRL modules.

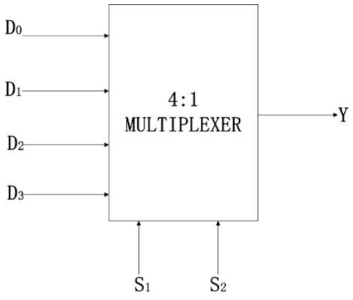
4.3 Memristor-Based Multiplexer

Multiplexer is also called data selector, or multi-way switch. Its basic function is to select one of the data from multiple input signals and send it to the output port under the control of address signal (channel selection signal), which is equivalent to a single-pole multi-throw switch with multiple inputs. The multiplexer with 2^n data input terminals must have N-bit address input terminals, which is called 2^n:1 multiplexer. Figure 10a, b shows the block diagram and truth table of the 4:1 multiplexer.

Output logic expression of 4:1 multiplexer can be obtained:

$$Y = D_0\overline{S_2S_1} + D_1\overline{S_2}S_1 + D_2S_2\overline{S_1} + D_3S_2S_1 \tag{15}$$

According to the output logic expression, the circuit constructed by the new memristor ratioed logic is shown in Fig. 11, in which D_0–D_3 are data input terminals, and S_2, S_1 are address input terminals. The values of address variables S_2 and S_1 determine the selection of one of the four input signals. In the circuit, M_3–T_3 and M_6–T_9 are two NOT gates, which are used to reverse the address input signals S_1 and S_2. M_5–T_5–T_{10} constitute a three-input NOR gate (where the DC voltage VCC connected with M_5 is treated as a input signal D_3), which is used to perform the logic operation: $D_3 \cdot \overline{\bar{S}_2 + \bar{S}_1} = D_3S_2S_1$. Similarly, the output of the three-input NOR gate, M_1–T_1–T_6, is $D_2 \cdot \overline{\bar{S}_2 + S_1} = D_2S_2\bar{S}_1$; and the outputs of the three-input NOR gates, M_4–T_4–T_7 and M_2–T_2–T_8, are $D_1\bar{S}_2S_1$ and $D_0\bar{S}_2\bar{S}_1$, respectively. These four outputs are then applied to the inputs of the four inputs NOR gate (consisting of M_7, T_{11}–T_{14}), and its output can be described as



(a)

INPUT		OUTPUT
S_2	S_1	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

(b)

Fig. 10 The 4:1 multiplexer block diagram and truth table

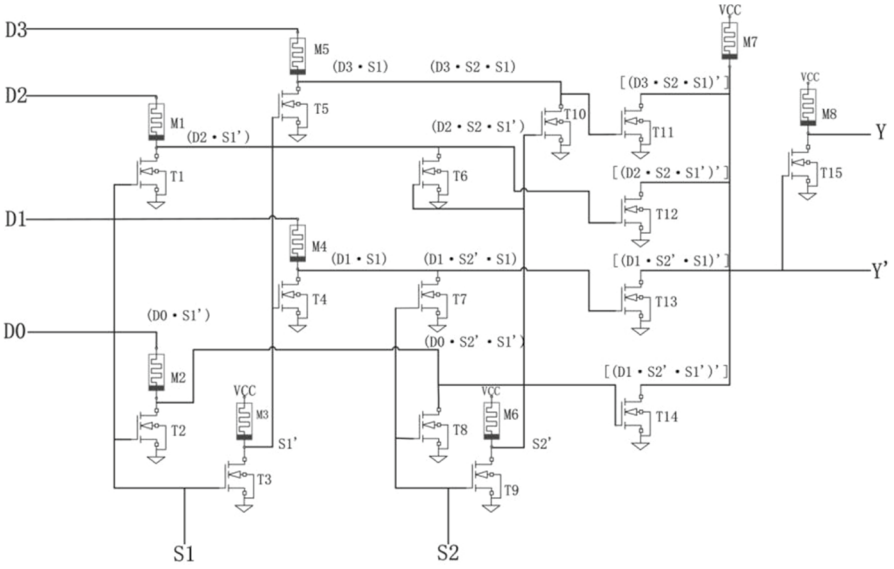


Fig. 11 The 4:1 multiplexer

$$Y' = \overline{D_0\overline{S_2S_1} + D_1\overline{S_2}S_1 + D_2S_2\overline{S_1} + D_3S_2S_1}.$$

Then, the signal is sent to the inverter (consisting of M_8 and T_{15}), and the output signal $Y = \overline{Y'}$ is obtained as described in Eq. (15).

Observe from Fig. 11 that the logic circuit uses only 15 NMOS transistors and 8 memristors, while the traditional CMOS process requires at least 39 transistors [8]. Therefore, the operation rate of the multiplexer is improved and its power consumption is further reduced.

4.4 Memristor-Based Full Adder

At present, there are many papers related to the design of memristor-based full adder. Here, an improved 1-bit full adder is presented in the paper, as shown in Fig. 12, where the multifunctional 1T–5M logic circuit module shown in Fig. 5 is used to design the full adder. The full adder uses only 6 NMOS transistors and 16 memristors. Compared with the previous memristor-based full adders proposed in Refs. [5, 7, 19, 21], the proposed full adder has a great improvement in reducing the number of transistors, as shown in Table 1.

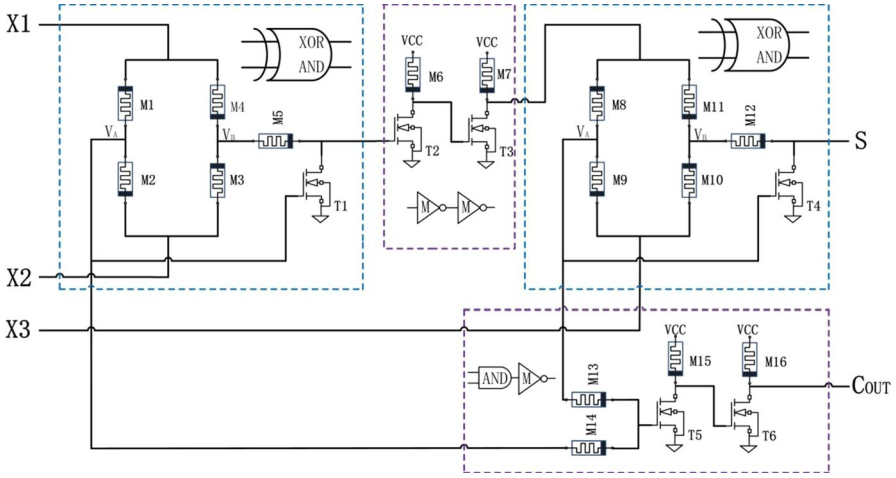


Fig. 12 The 1-bit full adder

Table 1 Quantity comparison of transistors and memristors of 5 different full adders

Parameters	Full adder in Ref. [5]	Full adder in Ref. [7]	Full adder in Ref. [19]	Full adder in Ref. [21]	Full adder in this paper
CMOS	15 T	15 T	15 T	15 T	6 T
MEMRISTOR	12 M	18 M	15 M	12 M	16 M

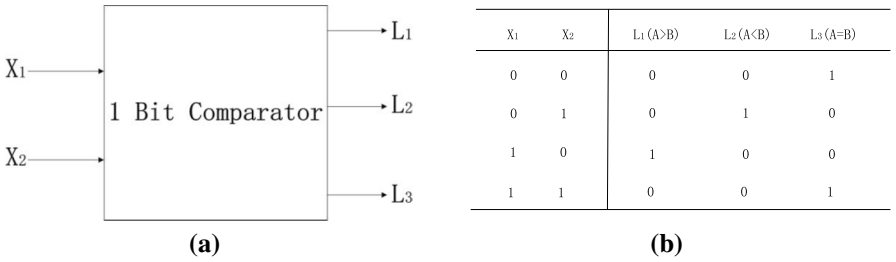


Fig. 13 Block diagram and truth table of the 1-bit numeric comparator

4.5 Memristor-Based Numerical Comparator

A logic circuit used to compare the numeric values of two numbers is called a numerical comparator. 1-bit numerical comparator is the basis of all numerical comparators. Its logical block diagram and truth table are shown in Fig. 13a, b.

The 1-bit numerical comparator circuit can be implemented by the new memristor ratioed logic gates, as shown in Fig. 14, which contains one NOR gate

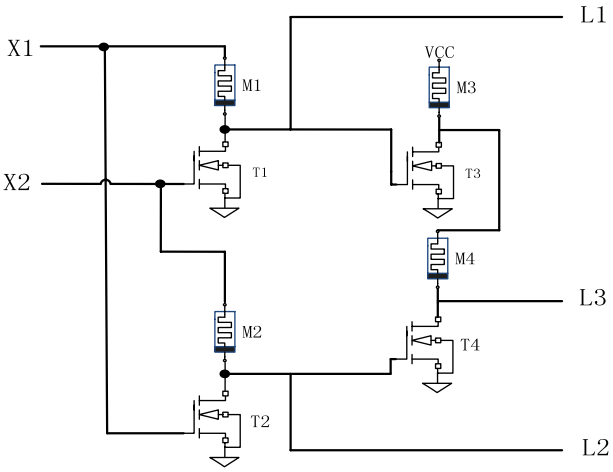


Fig. 14 The 1-bit numeric comparator

M3-T3 and three A AND (NOR B) gates in Fig. 4b: M1–T1, M2–T2 and M4–T4. Observe from Fig. 14 that, the logic relationships are as follows:

$$\begin{aligned} L_1 &= X_1\overline{X_2} \\ L_2 &= \overline{X_1}X_2 \\ L_3 &= \overline{\overline{X_1}X_2 + X_1\overline{X_2}} \end{aligned} \tag{16}$$

Similar to 1-bit numerical comparator, 4-bit numerical comparator has more complex functions, and its output logic expression is as follows:

$$\begin{aligned} L_1(A>B) &= A_3\overline{B_3} + \overline{A_3 \oplus B_3}\cdot A_2\overline{B_2} + \overline{A_3 \oplus B_3}\cdot\overline{A_2 \oplus B_2}\cdot A_1\overline{B_1} \\ &\quad + \overline{A_3 \oplus B_3}\cdot\overline{A_2 \oplus B_2}\cdot\overline{A_1 \oplus B_1}\cdot A_0\overline{B_0} \\ &\quad + \overline{A_3 \oplus B_3}\cdot\overline{A_2 \oplus B_2}\cdot\overline{A_1 \oplus B_1}\cdot\overline{A_0 \oplus B_0}\cdot(a>b) \\ L_2(A<B) &= A_3\overline{B_3} + \overline{A_3 \oplus B_3}\cdot\overline{A_2}B_2 + \overline{A_3 \oplus B_3}\cdot\overline{A_2 \oplus B_2}\cdot\overline{A_1}B_1 \\ &\quad + \overline{A_3 \oplus B_3}\cdot\overline{A_2 \oplus B_2}\cdot\overline{A_1 \oplus B_1}\cdot\overline{A_0}B_0 \\ &\quad + \overline{A_3 \oplus B_3}\cdot\overline{A_2 \oplus B_2}\cdot\overline{A_1 \oplus B_1}\cdot\overline{A_0 \oplus B_0}\cdot(a<b) \\ L_3(A=B) &= \overline{A_3 \oplus B_3}\cdot\overline{A_2 \oplus B_2}\cdot\overline{A_1 \oplus B_1}\cdot\overline{A_0 \oplus B_0}\cdot(a=b) \end{aligned} \tag{17}$$

Because of the complexity of this combinational logic circuit, some basic logic circuit blocks are encapsulated in this paper, as shown in Fig. 15. The 4-bit digital comparator circuit consists only of 32 NMOS transistors and 91 memristors. Therefore, compared with the traditional CMOS 4-bit comparator [10], the logic circuit uses not only less transistors, but also less power consumption.

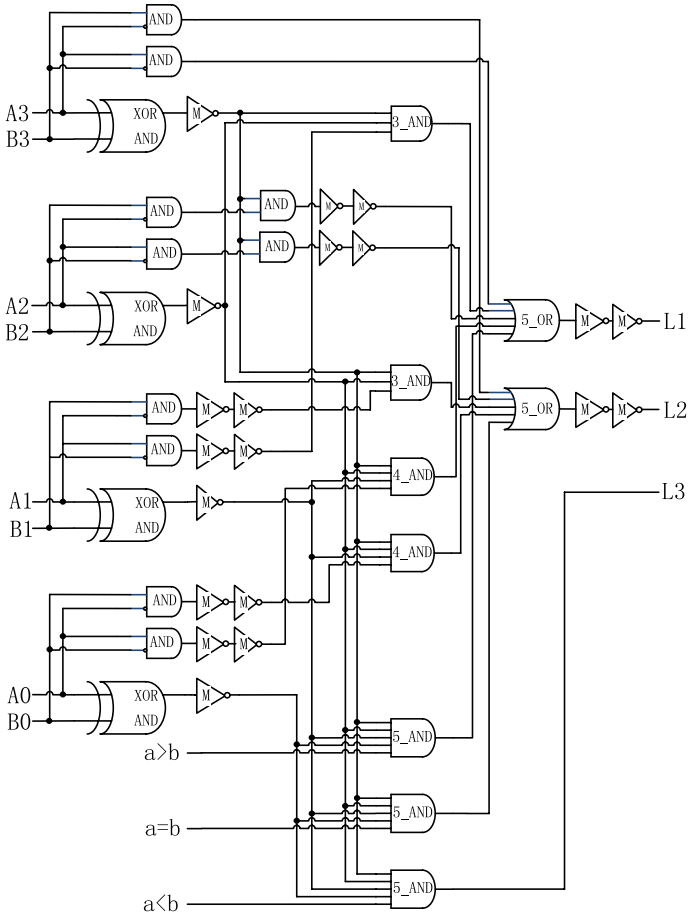


Fig. 15 The 4-bit numeric comparator

5 Ltspice Simulation Results and Performance Analysis

In this paper, we use the general memristor model to design the combinational logic circuits, in which encoder, decoder, 1-bit numerical comparator and 4:1 multiplexer are based on the new memristor ratioed logic, and the 1-bit full adder and 4-bit numerical comparator are based on the new MRL and the multifunctional logic module. In the LTspice simulations, the parameters of NMOS transistor are: $L = 0.01$ µm, $W = 40$ µm; the parameters of the memristor are identical with those in Fig. 2. And some performances of the designed combinational logic circuits, including power consumption, delay and the number of components, are calculated and compared with the traditional CMOS technology.

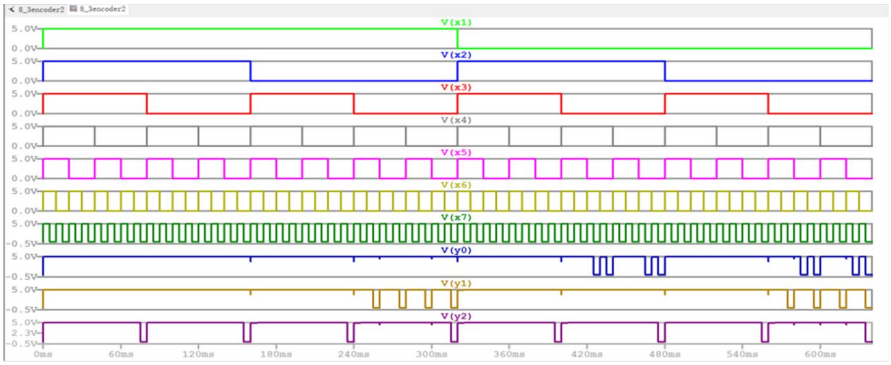


Fig. 16 The 3-bit binary encoder simulation waveform

Table 2 Quantity comparisons of CMOS-based encoder and memristor-based encoder

Parameters	The CMOS-based 3-bit encoder in Ref. [15]	The memristor-based 3-bit encoder
Num of components	40 (transistor)	22 (15 transistors + 6 memristors)
Power consumption	14.3mW	7.96uW
Delay	50.02 ns	0.412 ns

5.1 The 3-Bit Binary Encoder

As shown in Fig. 16, the simulation results of the memristor-based 3-bit binary encoder are consistent with the corresponding truth table, which can realize the function of the encoder. Compared with CMOS-based 3-bit binary encoder [1], the designed memristor encoder consumes less power and uses less components and the results are shown in Table 2. At the same time, due to the use of less components, it can also be improved in reducing the area of chips.

5.2 The 3-Bit Binary Decoder

As shown in Fig. 17, the simulation results of the memristor-based 3-bit binary decoder are consistent with its truth table. Compared with CMOS-based 3-bit binary decoder [15], the memristor decoder designed in this paper uses fewer transistors, consumes less power and uses less components and the results are shown in Table 3. Because of the fewer components used, it can also have a greater improvement in reducing the chip area.

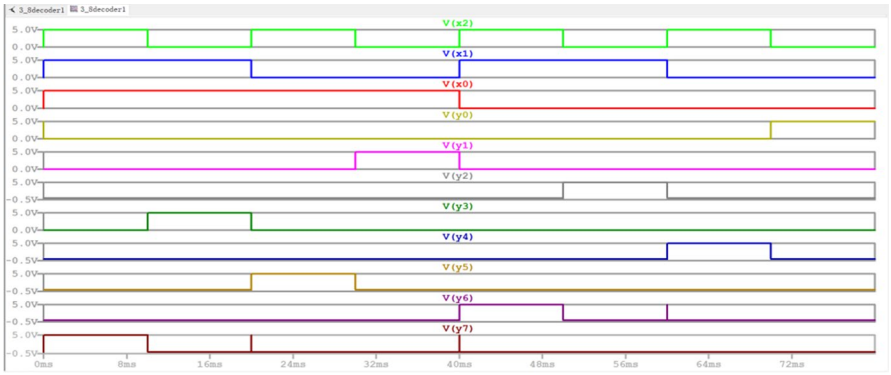


Fig. 17 The 3-bit binary decoder simulation waveform

Table 3 Quantity comparisons of CMOS-based decoder and memristor-based decoder

Parameters	The CMOS-based 3-bit decoder in Ref. [15]	The memristor-based 3-bit decoder
Num of components	70 (transistor)	32 (20 transistors + 12 memristors)
Power consumption	33.06 mW	6.34uW
Delay	5 ps	0.31 ps

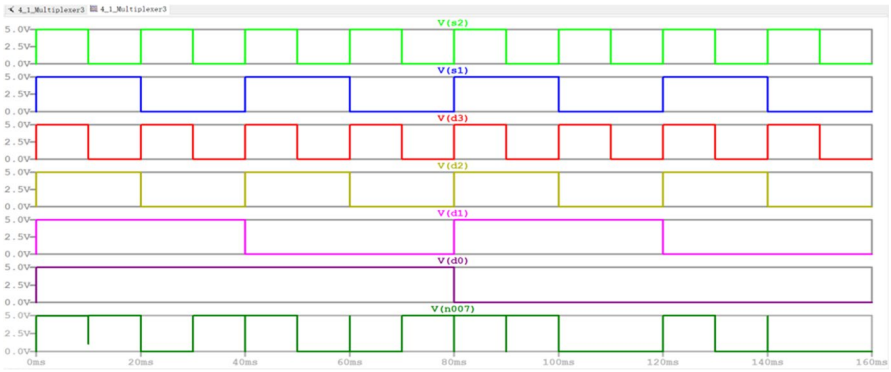


Fig. 18 The 4:1 multiplexer simulation waveform

5.3 The 4:1 Multiplexer

The simulation waveforms of 4:1 multiplexer are shown in Fig. 18. By selecting the address signal, the corresponding input signal can be selected for output. The

Table 4 Comparisons of CMOS-based multiplexer and memristor-based multiplexer

Parameters	The CMOS-based 4:1 multiplexer in Ref. [1]	The memristor-based 4:1 multiplexer
Num of components	At least 26 (transistor)	23 (15 transistors + 8 memristors)
Power consumption	1.45 W	13.92 mW
Delay	7 ps	0.273 ps

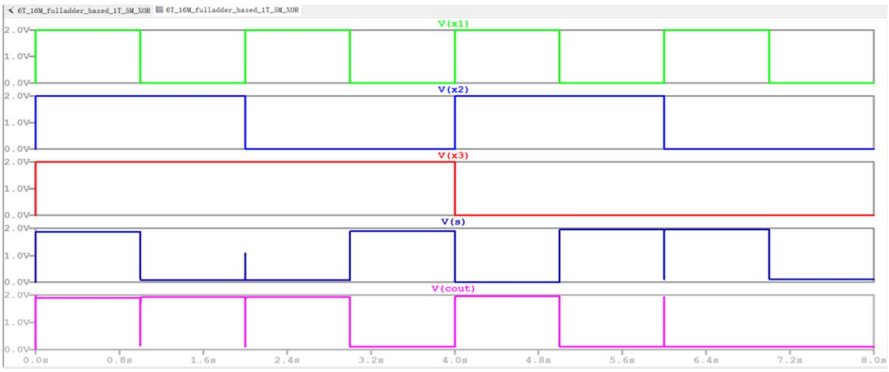


Fig. 19 The 1-bit full adder simulation waveform

simulation waveforms are consistent with the truth table and play the role of data selection. From Table 4, we can see that compared with the traditional CMOS-based 4:1 multiplexer [8], the 4:1 multiplexer based on the memristor ratioed logic is superior to the traditional logic circuit in terms of low power consumption and low delay. Due to the use of fewer transistors, the multiplexer can help to reduce chip area.

5.4 1-Bit Full Adder

In this paper, a 1-bit full adder has been designed based on 1T–5M multifunctional module, and its simulation waveforms are shown in Fig. 19. In the simulation process, all the input–output relations are consistent with the truth table, and the function of 1-bit full adder is realized. Table 5 shows that compared with the traditional CMOS-based 1-bit full adder [10] the full adder designed in this paper has improved in low power consumption, low delay, and reducing chip area.

5.5 4-Bit Numerical Comparator

Figure 20 shows the simulation waveforms of the 4-bit numerical comparator based on the multifunctional module and new memristor ratioed logic. In the simulation

Table 5 Comparisons of CMOS-based full adder and memristor-based 1-bit full adder

Parameters	The CMOS-based 1-bit full adder in Ref. [8]	The memristor-based 1-bit full adder
Num of components	28 (transistor)	22 (15 transistors + 8 memristors)
Power consumption	37.618 mW	6.2 mW
Delay	0.224 ns	0.09 ns

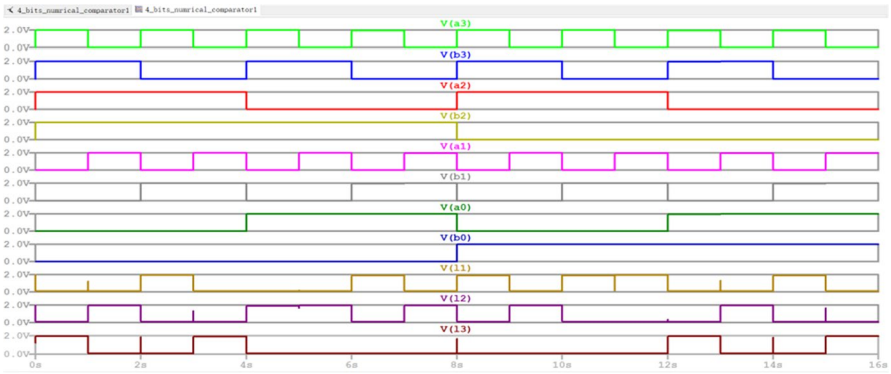


Fig. 20 4-bit numerical comparator simulation waveform

Table 6 Comparison of CMOS-based comparator and memristor-based comparator

Parameters	The CMOS-based 4-bit priority-encoding comparator in Ref. [10]	The memristor-based 4-bit priority-encoding comparator
Num of components	118 (transistor)	123 (32 transistors + 91 memristors)
Power consumption	114 mW	102.69 mW
Delay	20 ns	0.96 ns

test of the circuit, the relationship between input and output of all signals is consistent with its truth table. The circuit can realize the function of 4-bit numerical comparator. It can be observed from Table 6 that compared with the numerical comparator based on CMOS technology [5] the logic circuit proposed in this paper can reduce the number of transistors.

In summary, as a nanometer device, memristor is much smaller in size than CMOS transistor, and it is well compatible with CMOS transistors, that is, the manufacturing process of memristors can be completed on the metal layer of CMOS. Therefore, in the case of using the same components, the larger the proportion of the number of memristors in the same combinational logic circuit, the smaller chip area of the logic circuit. In addition, in physical principle, the delay of CMOS-based

logic circuits depends on the rate of hole and electron migration of CMOS, while the memristor-based logic circuits depend on the moving speed of the boundary between doped and non-doped regions, which is usually 10^4 times faster than the former [15]. Therefore, the delay of the memristor-based logic circuit is much lower than that of the traditional CMOS-based combinational logic circuit.

6 Conclusion

In this paper, based on the new MRL, we have designed the combinational logic circuits: a 3-bit binary encoder, a 3-bit binary decoder, a 4:1 multiplexer and a 1-bit comparator. Based on the new MRL and the proposed multifunctional logic module (1T–5M), we have designed a 1-bit full adder (6T–16M) and a 4-bit comparator. The LTSPICE simulation software is used to verify the logic functions of these logic circuits. It follows from the emulational and analytical results that compared with other memristor-based logic circuits and the traditional CMOS technology. The logic circuits designed in the paper use fewer circuit elements, have higher precision, and reduce the time delay, chip area and power consumption.

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Data Availability The authors first thank the anonymous reviewers, and the datasets generated during the current study are available from the corresponding author on reasonable request.

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