



A 16 ns, 28 fJ Wide-Range Subthreshold Level Converter Using Low-Voltage Current Mirror

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Abstract

This paper proposes a high-speed and energy-efficient low-voltage current mirror-based level converter (LCM LC) which can perform a wide-range conversion of a subthreshold input signal (180 mV) to an above-threshold output signal (1.2 V). The proposed level converter utilizes low-voltage current mirror (LCM) circuit with high-threshold-voltage (*hvt*) PMOS devices in the pull-up network, which drives a switching current from high supply rail to output node during the high-to-low transition of an input signal to ensure wide-range conversion. The driving capability of the pull-down network in LCM LC is increased by employing inverse-narrow-width-effect (INWE)-aware low-threshold-voltage (*lvt*) NMOS devices in order to perform a high-speed operation. This level converter employs multi-threshold CMOS devices and is implemented in 45 nm technology using Cadence Virtuoso. The LCM LC exhibits a delay of 16.4 ns, energy per transition of 28.1 fJ and static power of 412 pW which are observed using Spectre circuit simulator for the target conversion from 0.2 to 1.2 V at a signal frequency of 1 MHz.

Keywords Low-voltage current mirror · Inverse narrow width effect · Subthreshold level converter · High speed · Energy efficient · Voltage level shifter

1 Introduction

The prominent demands of battery-operated/battery-less portable high-performance systems command the need for optimal power consumption in very high-density VLSI chips. The reduction of power consumption (dynamic) is a very crucial design con-

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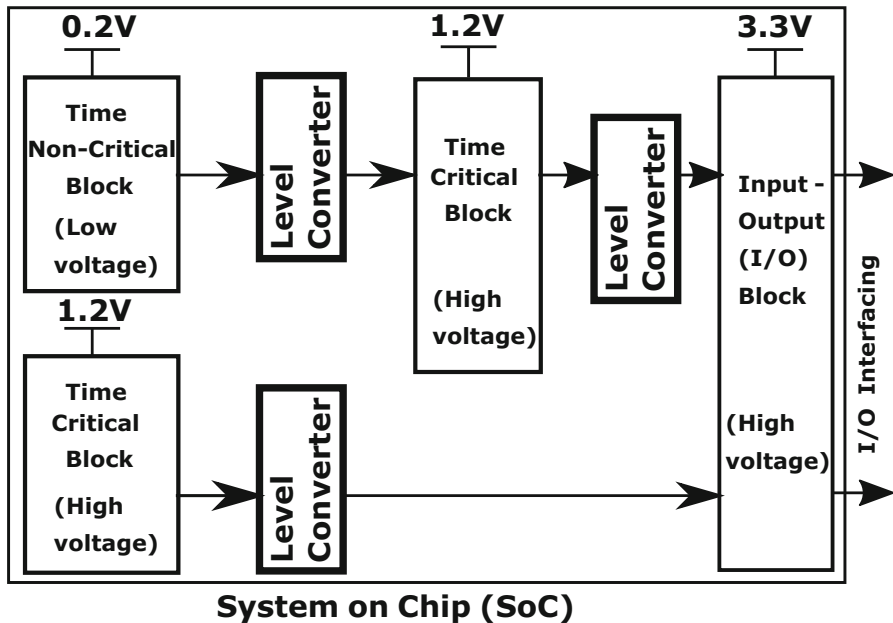


Fig. 1 Conceptual example of level converters in multi- V_{DD} design

cerning due to its correlation with the reliability of VLSI systems. This requirement has led to rapid and innovative developments in low power design during the recent years [4].

One of the widely preferred methodologies to reduce power consumption is voltage scaling. Reducing the supply voltage to near/subthreshold level is an efficient technique; however, it is limited by the time requirements of the system. Since scaling down the supply voltage degrades the performance of the system, time-critical parts of a system are operated above the threshold voltage (high voltage, i.e. V_{DDH}), while time non-critical parts of a system are operated with subthreshold voltage (low voltage, i.e. V_{DDL}) to improve its overall performance. This motivates to use multiple supply voltages in a system known as ‘Multi- V_{DD} technique’ or ‘Multi-Supply Voltage Design (MSVD)’ [5–8,13,16,17], which allows the designer to sufficient trade-off the power consumption and delay performance of the system.

Depending on the time requirements, different parts of the system are supplied with power using the multi- V_{DD} technique as shown in Fig. 1. In this conceptual example, high voltage domains that are supplied with voltage greater than the threshold voltage (i.e. 1.2 V, 3.3 V) are not able to identify the signals coming from low voltage domains that are fed with near/subthreshold voltage (i.e. 0.2 V). In order to alleviate this performance degradation, the system requires a vital level conversion circuit to convert near/subthreshold voltage to above threshold voltage by interfacing two different voltage domains. Moreover, the level converter (LC) should be designed with the ability to perform the desired level conversion with improved speed and power consumption performance with smaller silicon area. To address this issue, a state-of-the-art LC is

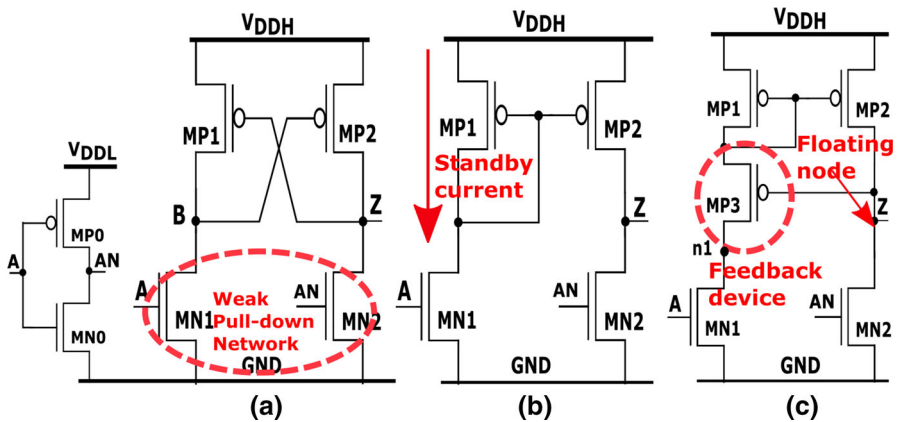


Fig. 2 Conventional level converters: **a** DCVS-based LC [5,13]; **b** CM-based LC; **c** WCM-based LC [8,17]

realized with differential cascaded voltage switch (DCVS) and current mirror (CM) structures.

In this paper, a high-speed and energy-efficient LCM LC with a wide range of voltage conversion using low-voltage current mirror (LCM) is proposed to alleviate the above limitations. The rest of this paper is organized as follows: The literature survey performed on existing LCs is presented in Sect. 2. The detailed explanation of the structure, design optimization and operational principles of proposed LC is listed in Sect. 3. Section 4 presents the simulation results and Sect. 5 is the conclusion of this paper.

2 Background Works

This section presents a brief overview of the three conventional level converters namely (1) differential cascaded voltage switch-based LC (DCVS LC), (2) current mirror-based LC (CMLC) and (3) Wilson current mirror-based LC (WCMLC).

DCVS LC The operation of the DCVS LC shown in Fig. 2a is explained as follows: For the low-to-high transition of input signal A, devices MN1 and MN2 are turned ON and OFF, respectively. The device MN1 pulls node B to the ground which makes MP2 ON and hence the output node Z charges to V_{DDH} . For the high-to-low transition of input signal A, devices MN1 and MN2 are turned OFF and ON, respectively. The device MN2 discharges the node Z to ground. Hence, the DCVS LC exhibits full-swing output voltage with no static current due to the absence of direct path between supply rails during the transitions.

However, the major limitation of DCVS LC [5–7,13,17] is that if the input signal approaches extremely low voltage (i.e. near/subthreshold level), then pull-down network (PDN) (MN1 & MN2) operates in weak inversion region, while pull-up network (PUN) (MP1 & MP2) operates in strong inversion region. That is, when PDN tries to discharge the node Z to ground, PUN charges the node Z towards V_{DDH} simul-

taneously. It causes a high current contention issue between PUN and PDN which makes the fall transition slow. One way to dominate the pull-up (PMOS) network is to strengthen the pull-down (NMOS) network by increasing the NMOS-to-PMOS size ratio [17]. But it takes a larger size and makes the circuit unrealizable. Additionally, the LC in [17] adopts inverse-narrow-width-effect (INWE)-aware PDN to improve driving capability. Alternatively, NMOS-diode current limiter can be inserted in the PUN to reduce the contention problem [5]. Eventually, the solution suggested is that the PMOS current should be lesser than NMOS current (i.e. $I_{PMOS} \ll I_{NMOS}$) [6]. Similarly, the two-stage structure with diode-connected NMOS [13] and the stacked pull-up network [7] based DCVS LCs are also suggested for robust voltage conversion. Though they limit contention issues, they exhibit larger delay, static power and circuit complexity. Hence, an alternative LC structure is essential for efficient voltage level conversion.

CMLC Fortunately, the current mirror-based LC (CMLC) structure helps to mitigate the contention issue in DCVS LC as shown in Fig. 2b. For high-to-low transitions, MN1 turns OFF and does not allow current flow through MP1 and MP2. At the same time, MN2 turns ON and discharges the output node Z to ground. However, the main drawback of CMLC is the presence of static current that flows through the devices MN1 and MP1 when the input signal goes to logic ‘high’ and results in larger standby power.

WCMLC To address the static current issue in CMLC, several improved CM-based LCs are suggested recently. In [8], Wilson current mirror-based LC (WCMLC) is shown in Fig. 2c and it effectively reduces the static current with feedback device MP3 which is connected at node Z. When signal A is V_{DDL} , there is current flow through devices MN1, MP3 and MP1. This current is mirrored through MP2 and it charges the node Z to V_{DDH} . At the same time, the feedback device MP3 being turned OFF reduces the static current through MN1, MP3 and MP1.

Limitations of WCMLC (1) Due to the feedback device MP3 turning OFF for low-to-high transition, WCMLC reduces the current through MP2 by making the node Z floating and reduces the voltage swing. This floating node voltage (FNV) at Z causes the short circuit current in the output inverter connected at this node Z.

(2) When the input signal A is at logic ‘0’ (0V), MN2 turns ON and discharges the output node Z. Simultaneously, MP3 also turns ON and charges the node *n1* by driving the current from V_{DDH} . This current is mirrored through MP2 (since MP1 and MP2 form a current mirror) to charge the output node Z and results in further contention problem (CP) between MP2 and MN2. The aforementioned issues were reduced by modifying the WCMLC.

The FNV is reduced by utilizing dual CM structure [16] and multi-stage structure [1] to produce a full-swing voltage at the output of WCMLC. However, due to multiple stages, they suffer from larger delay and energy consumption. Alternatively, usage of a reduced swing inverter [9] to restore the output voltage and modified Wilson current mirror [12] (using diode-connected PMOS) helps to avoid the FNV. But the performance degrades with the circuit complexity, increased power consumption and higher delay.

The CP is suppressed by the use of the current limiter for weakening the PUN when PDN is pulling the output node down. This can be accomplished by using controlled

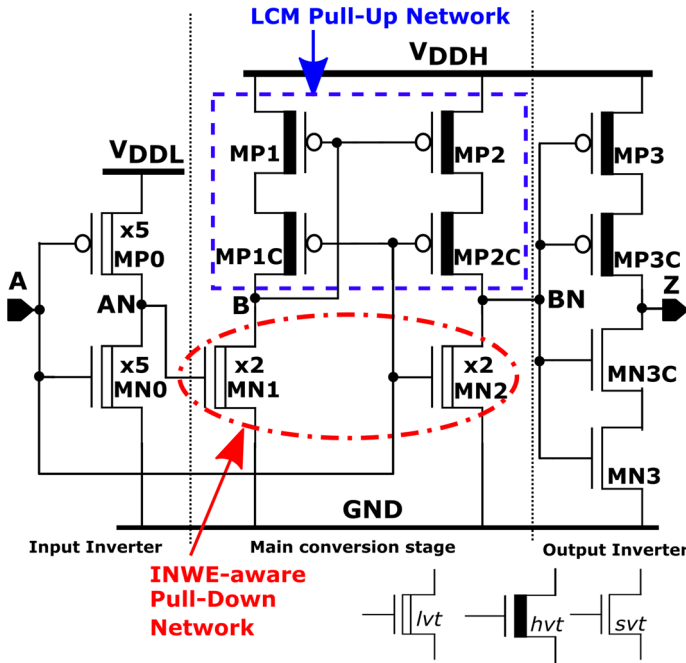


Fig. 3 Schematic of the proposed low-voltage current mirror level converter (LCM LC) circuit

CM structure [2] with self-control mechanism by detecting output error [3,14] or controllable current source with diode-connected level shifter [10]. Even though this method produces better static power performance, it consumes larger switching energy and larger delay due to additional devices.

The FNV and CP in LC are overcome by the proposed LCM LC which ensures energy-efficient operation with full-swing output voltage. It also helps to minimize the contention problem due to the presence of its internal control mechanism in the pull-up network. In addition, INWE-aware [18] pull-down network improves the speed of high-to-low transition, while MTCMOS devices assist to reduce the static power consumption. The detailed description of the proposed LCM LC is furnished in Sect. 3.

3 Proposed Low-Voltage Current Mirror Level Converter (LCM LC)

This section describes the structure, performance optimization and operational principles of proposed LCM LC. The schematic of the proposed level converter is shown in Fig. 3.

3.1 Structure of LCM LC

The proposed LCM LC consists of three stages namely (1) input inverter, (2) main conversion stage and (3) output inverter.

Input Inverter It consists of low-threshold-voltage (*lvt*) transistors (MN0 & MP0) to provide fast low-voltage inverted input signal (AN) to the main conversion stage. The speed of the input inverter is increased using minimum width sizing with five numbers of fingers based on the INWE-aware sizing method [18] (transistors with a width of 120nm).

Main conversion stage This stage consists of two blocks which are inverse-narrow-width-effect (INWE)-aware [18] PDN and low-voltage current mirror (or low-voltage cascode mirror) (LCM) [11] based PUN. The INWE-aware PDN is composed of MN1 and MN2, while LCM-based PUN is composed of MP1-MP1C and MP2-MP2C.

The gates of pull-down NMOS devices MN1 and MN2 are connected to low-voltage inverted input signal (AN) and the input signal (A), respectively. To increase the driving capability of the NMOS devices and to provide a fast switching response for the low-to-high transition of the input signal, both are chosen as low-threshold (*lvt*) devices.

The LCM structure is composed of four high-threshold-voltage (*hvt*) transistors. The gates of MP1 and MP2 are tied together and connected to the drain of MN1 (at node B) and this node voltage decides the functioning of MP1 and MP2. Likewise, the gates of cascode devices MP1C and MP2C are tied together and connected to a low-voltage input signal (A) to control the functionality of cascode transistors. The LCM structure requires only one V_{GS} voltage for its proper operation (i.e. say 1 V) and provides pull-up control to the level converter. The output signal is taken from the intersection node of pull-up and pull-down networks (at node BN) to provide a complementary full-swing output signal to the next stage.

Output inverter This stage is constructed using two stacked *hvt* PMOS and two standard-threshold-voltage (*svt*) NMOS devices. This output stage is used to provide the required output signal from the node BN. The ultimate purpose of this structure is to function as an output driver and also to reduce the static current issue in the LCM LC. The *hvt* PMOS MP3 maintains the source voltage of MP3C below V_{DDH} which is lesser than bulk voltage since bulks of all PMOS are connected to V_{DDH} . This increases the threshold voltage (V_{TH}) but reduces the static current.

3.2 Performance Optimization of LCM LC

The proposed LCM LC's performance is optimized by (1) utilizing multi-threshold CMOS (MTCMOS) technique together with proper subthreshold device sizing and (2) inverse-narrow-width-effect (INWE)-aware PDN. These methodologies help further to reduce static current and to increase the speed performance of LCM LC.

3.2.1 Usage of MTCMOS

In the main conversion stage, the pull-up network employs LCM with *hvt* devices which helps to reduce the contention problem and static power consumption. Additionally, these devices improve the immunity of parameter variation and also provide strong pull-up strength to the node BN. The *hvt* LCM-based pull-up network is purposely chosen because this can operate under low supply voltage (i.e. requires only

$V_{TH,PMOS}$) and helps to convert the near/subthreshold to the above threshold voltage. In addition, the internal control formed by MP1C and MP2C of LCM structure mitigates the contention issue.

In addition, the input inverter utilizes *lvt* devices, while the output inverter adopts stacked *hvt* pull-up and *svt* pull-down devices to improve the robustness and minimize static current issue to guarantee a powerful pull-down at the output node Z.

3.2.2 INWE-Aware Sizing

The inverse narrow width effect (INWE) is explored in the pull-down network of the main conversion stage with low-threshold-voltage (*lvt*) devices. When the channel width of transistor reduces, the threshold voltage (V_{TH}) decreases and the drain current ($I_{D,SAT}$) increases due to the contribution of sharp corner parasitic transistor in the Shallow-Trench Isolation (STI) process. This is known as the inverse narrow width effect (INWE) [15]. Since the drain current is exponentially related to threshold voltage in the near/subthreshold region, it is heavily influenced by the INWE-aware device sizing method [18] to reduce the threshold voltage without compromising the drain current. It is investigated on 45 nm CMOS technology with V_{DDH} of 1.2 V. It is observed that when the NMOS channel width decreases towards the minimum width ($W = 120$ nm), the threshold voltage and the drain current roll-off sharply as shown in Fig. 4. However, the drain current still maintains sufficiently higher values to improve the driving capability of a pull-down network. The threshold voltage resides nearly constant for transistor widths above $1.5 \mu\text{m}$. It is also noted that a smaller variation in threshold voltage of 22 mV results in higher drain current variation around 140 nA.

As a result, the pull-down devices (MN1 & MN2) in the main conversion stage are chosen as INWE-aware devices to improve the drivability and enhance the speed. This INWE-aware sizing of the pull-down network is implemented by having a minimum channel width of 120 nm with two fingers to provide sufficient current for fast switching without aggressive device sizing. So the sizing of the pull-down NMOS is drastically reduced to half of the size used in [17]. Further, the selection of low-threshold-voltage (*lvt*) devices in a pull-down network helps to handle low-voltage input signals with fast switching.

The speed performance of the input inverter is also enhanced by utilizing a similar INWE-aware device sizing method for both MP0 and MN0 (here, five transistors with a width of 120 nm are connected in parallel).

3.3 Operation of Proposed LCM LC

This section introduces the essential operational principles of the proposed LCM LC. The input signal (A) with an amplitude of 0.2 V and signal frequency of 1 MHz with rising and fall times of 1 ns is applied to the proposed LCM LC and the transient response is observed in Fig. 5 with (a) internal node voltages (AN, B, BN), (b) switching current (I_{DDH}) at V_{DDH} ($=1.2$ V) and (c) switching current (I_{DDL}) at V_{DDL} ($=0.2$ V) using Spectre circuit simulator.

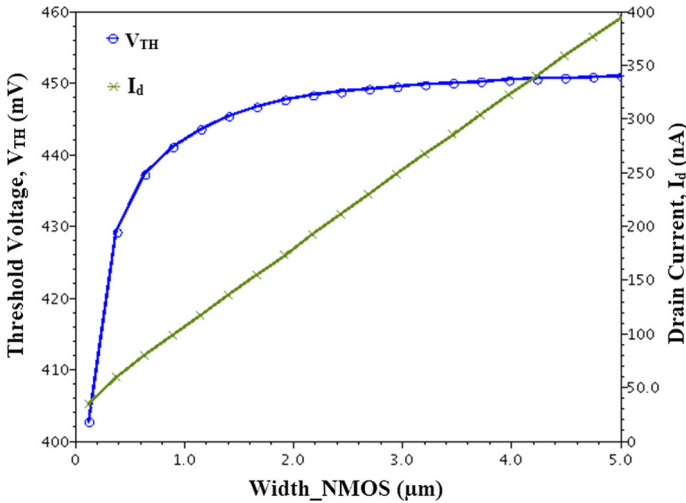


Fig. 4 Inverse narrow width effect: Effect of channel width on threshold voltage (V_{TH}) and drain current (I_d) at $V_{DDH} = 1.2$ V with 45 nm CMOS technology

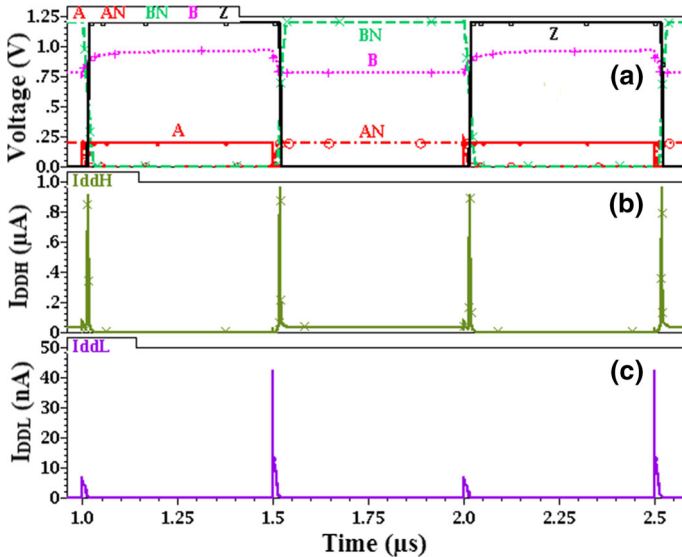


Fig. 5 Simulated transient response of LCM LC, **a** internal node voltages (AN,B,BN) with input (A) and output (Z) signal, **b** switching current (I_{DDH}) produced by $V_{DDH} (=1.2$ V), **c** switching current (I_{DDL}) produced by $V_{DDL} (=0.2$ V)

At the standby mode, both the signals A and Z stand at zero voltage (0 V), while AN is switched to V_{DDL} . So the devices MN1 and MN2 are turned ON and OFF, respectively. Since the gates of MP1C and MP2C are connected to the input signal A, both the devices are turned ON. Now the voltage at node B is pulled down quickly due to INWE-aware lvt device and leads to MP1 & MP2 being switched ON. Hence,

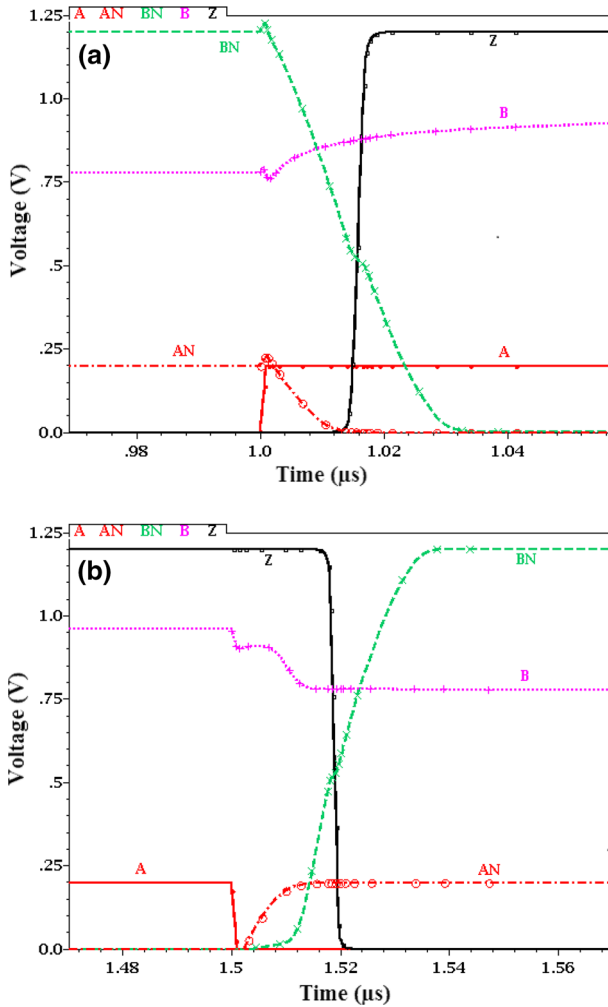


Fig. 6 Transient response of output signal (Z) and other internal signals (AN, B, BN) for the given input signal (A): **a** low-to-high transition, **b** high-to-low transition

there is current conduction through MP1, MP1C and MN1 which leads to the voltage drop at node B as $V_{DDH} - V_{TH,MP1(MP2)}$. Since the transistors MP1, MP2, MP1C and MP2C form a low-voltage current mirror (LCM), the current is mirrored through MP2 and MP2C and charges the node BN towards V_{DDH} . After that, the node voltage BN turns ON MN3 and MN3C in the output inverter to discharge the node Z. Finally, the output node Z becomes low (0 V).

As shown in Fig. 6a, for the low-to-high transition of the input signal A, MN2 turns ON and discharges the node BN to ground. Simultaneously, the *hvt* PMOS devices MP1C & MP2C turn OFF when the input signal A goes to V_{DDL} . Also when AN is low, the transistor MN1 is turned OFF to make the LCM PUN inactive and

cut-off the transition current to the node BN. So the node BN is isolated from the supply voltage (V_{DDH}) and eliminates the contention problem between pull-up and pull-down networks. It is noted that contention-free operation is achieved by internal control, formed by MP1C and MP2C.

In addition, INWE-aware device sizing of MN2 supports to quickly discharge the node BN. This drives the stacked PMOS devices (MP3 & MP3C) in the output inverter to charge the node Z towards V_{DDH} . Finally, the full-swing output voltage is obtained at the output node Z, which highlights the advantage of LCM LC over WCMLC. Finally, the problem of contention during the low-to-high transition is naturally mitigated in the LCM LC. A noteworthy mention is that the output inverter drives the current from higher supply voltage V_{DDH} during the low-to-high transition, while the current through the main conversion stage is cut-off, because of LCM PUN turn off. Also, note that the output inverter limits the current from V_{DDH} (less than $1 \mu\text{A}$) as shown in Fig. 5b due to the stacked PMOS structure. However, due to the stacking of devices, delay of LC increases as the capacitance load increases at the output node.

Similarly, the high-to-low transition at the input signal A (the node AN is charged to V_{DDL}) turns MN1 ON, while turning MN2 OFF. Since the gates of MP1C and MP2C are connected to the input signal A, both will be turned ON and allow the transition current through MP1, MP1C and MN1. This will be mirrored through MP2, MP2C to charge the node BN towards V_{DDH} as depicted in Fig. 6b. Finally, the stacked pull-down devices in the output inverter are turned ON to discharge the node 'Z' to the ground (0 V). Unlike WCMLC, the LCM LC exhibits full-swing voltage at the node BN and eliminates the static current issue in the output inverter. Hence, the proposed LC provides full-swing output voltage with reduced static current and mitigates the problem of contention during both the transitions.

4 Simulation Results and Discussion

In this section, the performance of the LCM LC is verified using the Spectre circuit simulator and implemented in 45 nm technology using Cadence Virtuoso. The layout of the LCM LC circuit is shown in Fig. 7 and it covers a silicon area of $0.173 \mu\text{m}^2$. The various transistor sizes used for performance analysis are summarized in Table 1. The channel length of the pull-down devices (MN1 & MN2) and pull-up devices (MP1 & MP2) are assumed as 90 nm (double of minimum allowable channel length) to reduce leakage of current through the main conversion stage. The width of pull-down devices in the main conversion stage is based on INWE-aware device sizing and kept at a minimum width of 120 nm with two numbers of fingers ($W = 120 \text{ nm} \times 2$). Similarly in the input inverter, the width of the devices (MP0 & MN0) are kept at a minimum with five number of fingers ($W = 120 \text{ nm} \times 5$) such that this enables the inverter to operate with extremely low input voltage and fast switching time. In the output inverter, minimum device size is chosen ($W/L = 120 \text{ nm}/45 \text{ nm}$) to avoid additional capacitance effect at the node BN. Though it uses minimum device size, the leakage current is mitigated by the stacking of devices. The circuit targets minimum delay and energy consumption and has been designed to be functional for three different

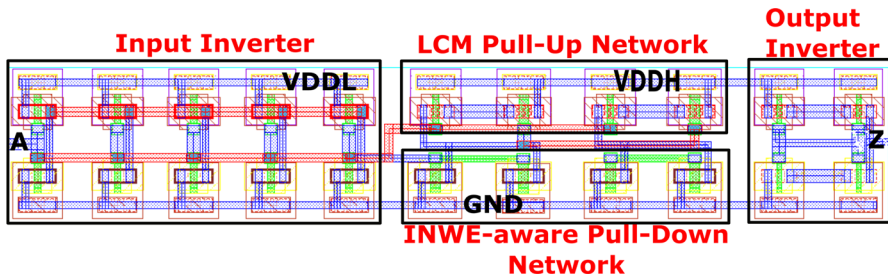


Fig. 7 Layout of the proposed LCM LC circuit

Table 1 Summary of transistor sizing in the proposed LCM LC circuit

Transistor	W/L (nm)	Transistor	W/L (nm)	Transistor	W/L (nm)
MP0	(120/60)*5	MN1	(120/90)*2	MN2	(120/90)*2
MN0	(120/60)*5	MP1	120/90	MP1C	120/60
MN3	120/45	MP2	120/90	MP2C	120/60
MN3C	120/45	MP3	120/45	MP3C	120/45

processes, voltage and temperature (PVT) corners with $V_{DDL} = 0.2$ V, $V_{DDH} = 1.2$ V and input signal frequency of 1 MHz with fall and rise times of 1 ns.

4.1 Energy per Transition and Delay Analysis

Three corners including the nominal corner, best corner and worst corner are considered to investigate the delay and energy consumption of the proposed LCM LC. The nominal corner includes typical nMOS and pMOS, $V_{DDH} = 1.2$ V and temperature of 27 °C. The worst corner includes slow nMOS and fast pMOS, $V_{DDH} = 1.32$ V and temperature of 0 °C. It emphasizes the significance of pull-down devices for proper level shifting by outperforming the pull-up devices. In contrast, the best corner includes fast nMOS, slow pMOS, $V_{DDH} = 1.08$ V and temperature of 125 °C for suitable level conversion.

The delay of the LCM LC circuit as a function of V_{DDL} across three PVT corners is demonstrated in Fig. 8a. It is observed that delay increases as V_{DDL} scales down towards the deep subthreshold region due to drastic reduction in drive current pull-down network. On the contrary, delay for three PVT corners shows flat response as V_{DDL} increases, especially after 300 mV. At $V_{DDL} = 200$ mV, the proposed LC shows a worst-case delay of 49.0 ns and best-case delay of 6.6 ns. From this observation, the worst corner delay is $7.43\times$ higher than the best corner delay. But, for $V_{DDL} \geq 300$ mV, the proposed LC shows the worst-case delay of 50 ns, nominal corner delay of 10.5 ns and best corner delay of 4.9 ns. Now the worst corner delay is $10.2\times$ higher than the best corner delay.

The energy consumption of LCM LC against V_{DDL} is depicted in Fig. 8b, in which the energy per transition decreases as V_{DDL} reduces, i.e. <400 mV, and increases

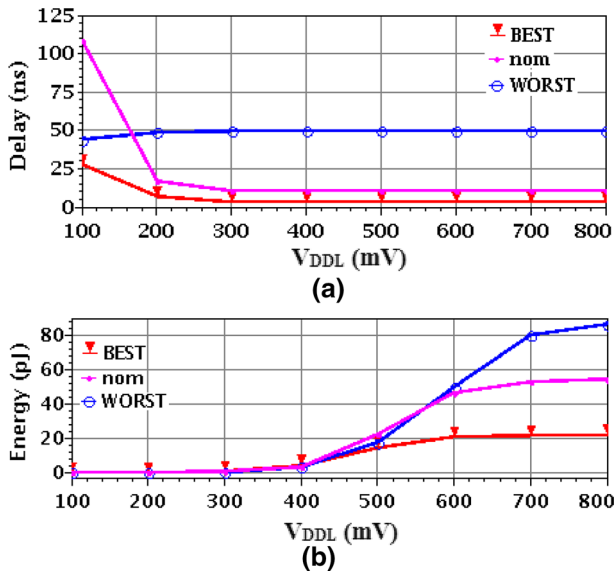


Fig. 8 Simulated results of **a** delay and **b** energy consumption of the proposed level converter for different values of V_{DDL} under three PVT corners with $V_{DDH} = 1.2$ V and $f_{in} = 1$ MHz

above that value for three PVT corners. At $V_{DDL} = 200$ mV, the energy consumption of the worst corner (74.43 fJ) is $3.4\times$ higher than the best corner (21.9 fJ), while it consumes 28.1 fJ at the nominal corner. From Fig. 8, noteworthy observation is that the LCM LC exhibits better delay and energy consumption performance between 300 and 400 mV of V_{DDL} .

Furthermore, in order to verify the performance of LCM LC against the capacitance load (CL), it is varied from no-load condition to 100 fF with $V_{ddL} = 0.2$ V, $V_{ddH} = 1.2$ V and input signal frequency of 1 MHz. Figure 9 shows the delay and energy consumption per transition of proposed LCM LC versus capacitance load. As expected, due to the stacking of devices in output inverter, delay and energy consumption are increased almost linearly as the capacitance load increases.

4.2 Performance Comparison of LCM LC with Existing LCs

The robustness of LCM LC is exhibited by comparing its performance with other LCs. Figure 10 shows the simulated value of delay, energy and static power consumption of proposed circuit and other state-of-the-art circuits for different values of V_{DDL} . All the circuits are implemented in 45 nm technology with optimization techniques such as MTCMOS & INWE-aware device sizing. It is simulated at nominal corner with $V_{DDH} = 1.2$ V, $V_{DDL} = 0.2$ V and $f_{in} = 1$ MHz. The output delay of the proposed LC is less than other existing circuits and it remains constant when V_{DDL} exceeds 300 mV. But the speed reduces as V_{DDL} approaches below 300 mV. However, the LCM LC takes 16.4 ns @ $V_{DDL} = 0.2$ V which is $1.8\times$ and $8.5\times$ less than WCMLC and DCVS LC, respectively, as shown in Fig. 10a.

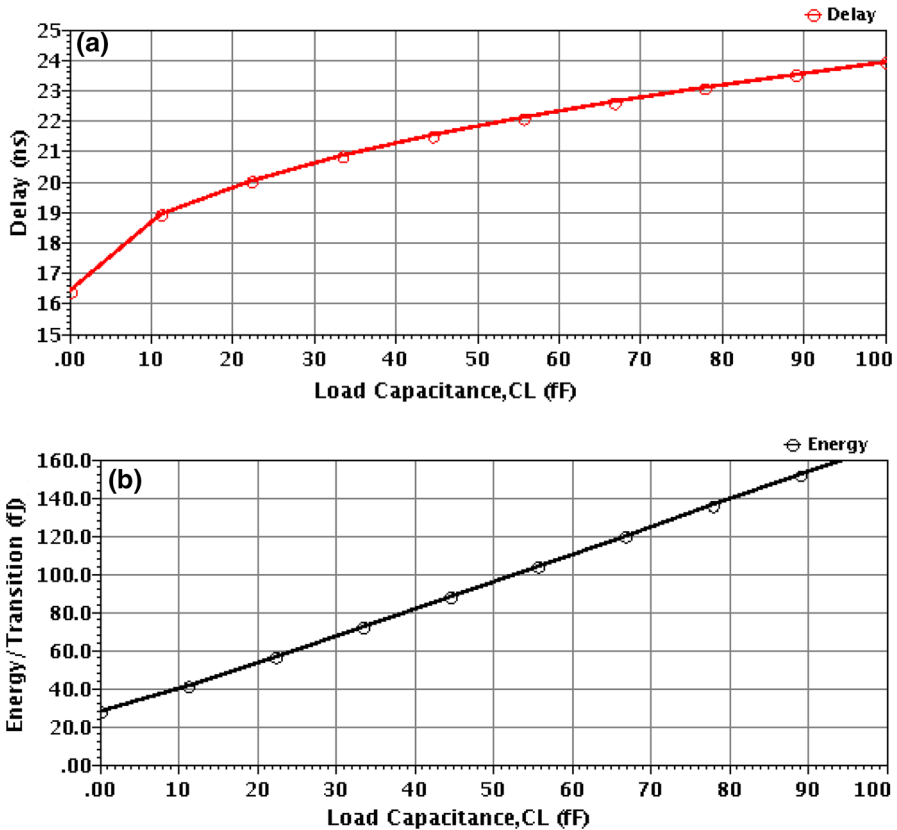


Fig. 9 Simulated results of **a** delay and **b** energy consumption of proposed LCM LC for different values of load capacitance with $V_{DDH} = 1.2$ V, $V_{DDL} = 0.2$ V and $f_{in} = 1$ MHz

In contrast to the delay performance, LCs are exhibiting higher energy consumption as V_{DDL} (above 300 mV) increases and they consume lower energy as V_{DDL} approaches Sub- V_{TH} (below 200 mV). Like delay performance, the LCM LC consumes energy of 28.1 fJ @ $V_{DDL} = 0.2$ V which is $3.1 \times$ less than WCMLC but it is closer to DCVS LC and CMLC as shown in Fig. 10b. But, it is observed that the WCMLC produces flat response better than other LCs when V_{DDL} is above 200 mV.

In order to study the static power performance, the input signal is kept at logic 'High'. Since the gates of MP1C & MP2C are connected to the logic 'high', both are turned OFF, MN2 is turned ON and discharges the node BN. Therefore, the static current flows through MP3 & MP3C; however, it is suppressed due to the stacking of devices. Figure 10c compares the static power consumption of existing LCs taken for analysis. All the LCs exhibit almost constant behaviour as V_{DDL} increases above 300 mV. But when V_{DDL} decreases, except WCMLC, all other LCs show optimal static power consumption. Although the static power consumption of DCVS LC is good compared to CM-based LCs, DCVS topology is not suitable for subthreshold voltage conversion. From Fig. 10c, it is observed that the LCM LC takes only static

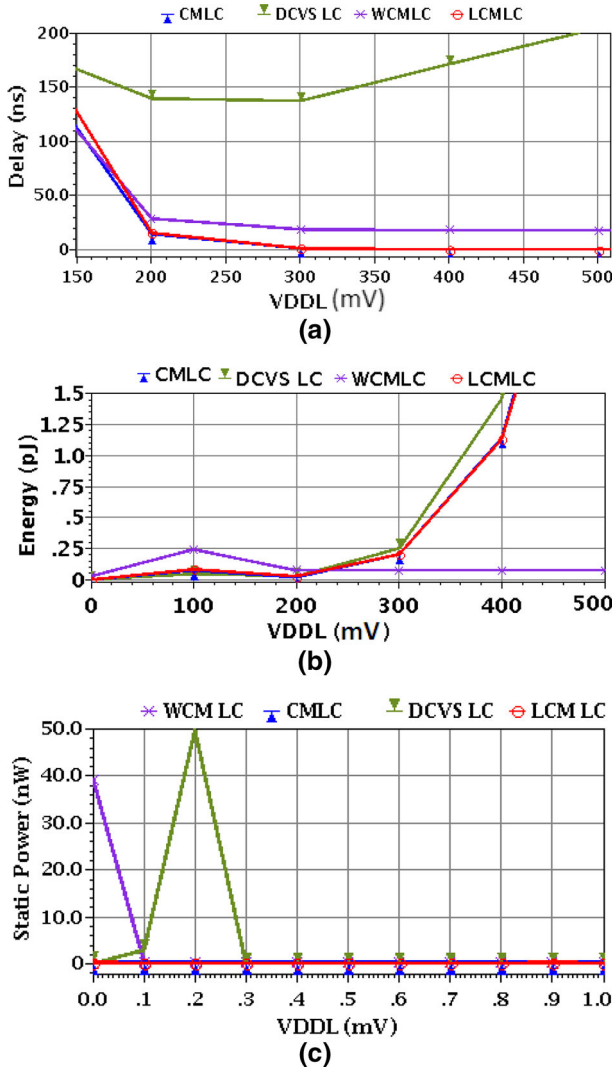


Fig. 10 Simulated results of **a** delay **b** energy consumption and **c** Static power of proposed LCM LC for V_{DDL} variation with $V_{DDH} = 1.2$ V and $f_{in} = 1$ MHz

power of 0.412 nW which is $95.1 \times$ less than the WCMLC. It can be seen that both LCM LC and CMLC show almost exact delay, energy and static power performance due to diode-connected device (MP1) utilized in the pull-up network.

The proposed LCM LC is compared with conventional LCs and the same is summarized in Table 2. It is observed that the state-of-the-art LC with DCVS topology consumes low static power (0.326 nW) with the expense of delay (237.3 ns) and energy (11.57 pJ). In the CM topology, specifically, WCMLC exhibits worst performance with a delay of 29.7 ns, energy per transition of 85.6 fJ and static power of 39.2 nW. For-

Table 2 Performance comparison of LCM LC with other state-of-the-art level converters in 45 nm technology ($V_{DDL} = 0.2$ V, $V_{DDH} = 1.2$ V and $f_{in} = 1$ MHz)

Work	Tech (nm)	Topology	$V_{DDL, min}$ (mV)	V_{DDH} (V)	Delay (ns) @ V_{DDL}	Energy (fJ) @ V_{DDL}	Static Power (nW)	Area (μm^2)
Proposed LCM LC	45	CM	180	1.2	16.4@0.2 V	28.1@0.2 V	0.412	0.173
WCMLC [17]	45	CM	100	1.2	29.7@0.2 V	85.6@0.2 V	39.2	0.166
CMLC [6]	45	CM	100	1.2	14.7@0.2 V	28.8@0.2 V	0.394	0.158
DCVSLC [5,13]	45	DCVS	600	1.2	237.3@0.6 V	11570@0.6 V	0.326	0.158
WCMLC [17]	65	CM	100	1.0	18.4@0.2 V	93.9@0.2 V	6.6	1.38
SCL ² S [7] ^a	65	CM	100	1.2	13.7@0.2 V	90.9@0.2 V	1.24	31.3
CL ² C [1] ^b	65	DCVS	140	1.2	25@0.3 V	30.7@0.3 V	2.5	17.6

^aSelf-controlled current limiter level shifter (SCL²S)^bCurrent limiter level converter (CL²C)

tunately, the LCM LC exhibits better performance with a delay of 16.4 ns, energy per transition of 28.1 fJ and static power of 0.412 nW.

5 Conclusion

A fast and energy-efficient voltage level converter based on the low-voltage current mirror capable of subthreshold (180 mV) to above threshold voltage (1.2 V) conversion is proposed in this paper. The low-power and high-speed operation was ensured by the MTCMOS and INWE-aware devices in pull-up and pull-down networks, respectively. The simulation result shows that LCM LC in 45 nm CMOS technology achieves $1.8\times$, $3.1\times$ and $95.1\times$ lesser delay, energy per transition and static power, respectively, compared to WCMLC. Hence, the proposed LCM LC can be utilized for the applications that require a high-speed and energy-efficient operation.

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Data Availability Statement The authors declare that the data supporting the findings and obtained during this research work are available within the paper, as listed in Tables 1 and 2.

Compliance with ethical standards

Conflict of interest The authors declare that they have no conflict of interest.

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