



# Novel Optimum Parity-Preserving Reversible Multiplier Circuits

Ehsan PourAliAkbar<sup>1</sup> · Keivan Navi<sup>2</sup> · Majid Haghparast<sup>3</sup> · Midia Reshadi<sup>1</sup>

Received: 11 March 2019 / Revised: 22 March 2020 / Accepted: 23 March 2020 / Published online: 8 April 2020  
© Springer Science+Business Media, LLC, part of Springer Nature 2020

## Abstract

Reversible logic is considered as a basic requirement for designing quantum computers. Reversible circuits do not waste energy. The use of this logic in low-power complementary metal–oxide–semiconductor circuits, quantum computing, and DNA computing has rendered reversible logic integral in today’s technology. Multiplication is regarded as a major operation in the arithmetic. Herein, four optimized parity-preserving reversible signed and unsigned multiplier circuits are presented to reduce the QUANTUM COST of the circuits. The designs can be expanded to an  $N \times N$  dimension. We prove that these multiplier circuits have lower QUANTUM COST, CONSTANT INPUTS, and GARBAGE OUTPUTS compared with previous studies.

**Keywords** Reversible logic circuit · Reversible multiplier · Unsigned multiplier · Signed multiplier · Quantum computing · Parity preserving

---

✉ Keivan Navi  
navi@sbu.ac.ir

Ehsan PourAliAkbar  
pour.ali@srbiau.ac.ir

Majid Haghparast  
haghparast@srbiau.ac.ir

Midia Reshadi  
reshadi@srbiau.ac.ir

- <sup>1</sup> Department of Computer Engineering, Science and Research Branch, Islamic Azad University, Tehran, Iran
- <sup>2</sup> Faculty of Computer Science and Engineering, Shahid Beheshti University G. C., Tehran, Iran
- <sup>3</sup> Department of Computer Engineering, Yadegar -e- Imam Khomeini (RAH) Shahre Rey Branch, Islamic Azad University, Tehran, Iran

## 1 Introduction

Reversible logic has attracted significant attention in circuit design. Reversible logic circuits are used because they do not waste energy. Irreversible logic circuits waste energy because of data loss. In 1961, Landauer proved that the loss of one bit of information results in  $KTLn2$  joules of energy wastage in irreversible logical circuits, where  $K$  is Boltzmann's constant [15]. In reversible circuits, this energy is not wasted, as proven by Bennet [2], and the number of inputs and outputs is equal. In addition, a one-to-one correspondence exists between the inputs and output. The input vector ( $I_v$ ) represents the inputs of a reversible logic circuit, and the output vector ( $O_v$ ) denotes the output of that circuit [27]. Equation (1) shows the  $I_v$  and  $O_v$  vectors.

$$\begin{aligned} I_v &= (I_1, I_2, I_3, \dots, I_n) \\ O_v &= (O_1, O_2, O_3, \dots, O_n) \end{aligned} \quad (1)$$

Using parity-preserving reversible blocks and gates is essential for a parity-preserving reversible circuit. A gate or block is considered as parity preserving when a balance is available between its inputs and outputs [7, 10, 19, 23, 27, 30, 31, 35].

Multiplication is considered as a popular arithmetic operation. In reversible logic, the design of unsigned and signed multipliers has been reviewed, some of which were parity preserving [3, 4, 8–10, 12–14, 18, 20, 28, 29, 31, 32, 35, 36].

We present a  $4 \times 4$  parity-preserving reversible unsigned multiplier circuit. It has been proved that the best result can be obtained in terms of the number of CONSTANT INPUTs, number of GARBAGE OUTPUTs, and QUANTUM COST. Furthermore, we present a  $5 \times 5$  parity-preserving reversible signed multiplier, unsigned multiplier circuits, as well as signed  $N \times N$  ones.

The remainder of this paper is organized as follows. Section 2 presents some basic concepts of reversible logic. Section 3 describes previous studies. The proposed circuits are presented in Sect. 4. The evaluation and comparison results are demonstrated in Sect. 5. The conclusion is presented in Sect. 6.

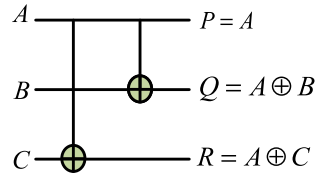
## 2 Basic Concepts

In this section, the basic concepts of reversible logic are defined. Subsequently, a few reversible logic parity-preserving gates are analyzed. Finally, multiplier circuits are explained.

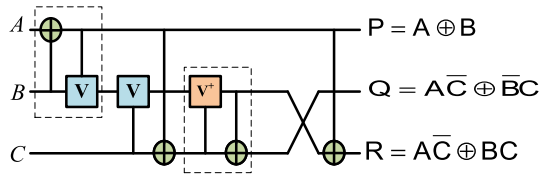
### 2.1 Reversible Logic

A gate is reversible if a one-to-one correspondence exists between the inputs and outputs values. To evaluate the efficiency of a reversible circuit, a few parameters can be used as benchmarks, including the CONSTANT INPUT, which involves a fixed value (of 0 or 1) [17], GARBAGE OUTPUT (useless output) [33], and QUANTUM COST (the sum of  $2 \times 2$  reversible gates). Circuits larger than  $2 \times 2$  should be converted

**Fig. 1** Parity-preserving reversible F2G gate



**Fig. 2** Parity-preserving reversible NFT gate



to several  $2 \times 2$  or  $1 \times 1$  smaller circuits. The total QUANTUM COST of  $2 \times 2$  circuits yields the QUANTUM COST of the larger circuits. In reversible logic, two quantum gates exist, i.e.,  $V$  and  $V^+$ . Another name for  $V$  is square root. Equation (2) is related to  $V$  and  $V^+$  gates [22].

$$\begin{aligned} V \times V &= V^+ \times V^+ = \text{NOT} \\ V \times V^+ &= I \end{aligned} \tag{2}$$

**2.2 Reversible Gates**

The Feynman [5], Toffoli [34], and Peres gates [25] are examples of nonparity-preserving gates. Many reversible parity-preserving gates exist, including the Feynman double gate (F2G) [33], new fault tolerant (NFT) gate [5], and FRG [6].

The F2G is regarded as a reversible parity-preserving gate with three inputs and three outputs, as shown in Eq. (3)

$$\begin{aligned} I_v &= (A, B, C) \\ O_v &= (P = A, Q = A \oplus B, R = A \oplus C) \end{aligned} \tag{3}$$

In Eq. (3),  $I_v$  and  $O_v$  are the F2G inputs and outputs, respectively. Figure 1 shows the F2G gate in the quantum structure. The F2G gate is used to produce a Fan-OUT in reversible parity-preserving circuits. The QUANTUM COST of the F2G gate is 2.

The NFT gate is another reversible gate that includes three inputs and three outputs, which is a parity-preserving gate. The inputs and outputs of this gate are shown in Eq. (4)

$$\begin{aligned} I_v &= (A, B, C) \\ O_v &= (P = A \oplus B, Q = B'C \oplus AC', R = BC \oplus AC') \end{aligned} \tag{4}$$

Figure 2 displays the NFT gate with a QUANTUM COST of 5.

			x	$X_3$ $Y_3$	$X_2$ $Y_2$	$X_1$ $Y_1$	$X_0$ $Y_0$
			$P_{31}$	$P_{30}$ $P_{21}$	$P_{20}$ $P_{11}$	$P_{10}$ $P_{01}$	$P_{00}$
	$P_{33}$	$P_{32}$ $P_{23}$	$P_{22}$ $P_{13}$	$P_{12}$ $P_{03}$			
$P_7$	$P_6$	$P_5$	$P_4$	$P_3$	$P_2$	$P_1$	$P_0$

**Fig. 3** Unsigned multiply operation of two 4-bit numbers

### 3 Related Studies

In this section, explanations are provided for the multiplication operation and analysis of reversible unsigned and signed multiplier circuits.

#### 3.1 Irreversible Multiplier

Multipliers can be categorized into unsigned and signed groups from one viewpoint. Furthermore, multiplication circuits can be categorized into serial and array structures. Hitherto, many serial and array multiplier circuits have been presented. The serial multiplication operation can be performed using a shift to the left or right. Several methods can be used in array multiplier operations including the Dadda and Wallace tree. Multiplying operations in the array method are performed in two sections, including partial product generation and partial product addition [24]. Figure 3 illustrates the operation of an unsigned multiplication.

#### 3.2 Parity-Preserving Reversible Multiplier

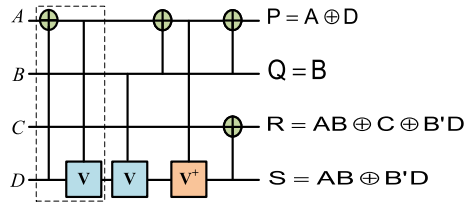
Thapliyal et al. [32] developed a nonparity-preserving reversible unsigned multiplier circuit using the TSG gate. In [8], Haghparast et al. presented a reversible unsigned multiplier circuit based on Peres gate (PG), Toffoli gate (TG), and HNG gates. In addition, Moghadam et al. formed a reversible multiplier circuit using PG and TG gates [18]. Furthermore, Jigalur et al. presented a reversible  $4 \times 4$  unsigned multiplier circuit using PG and HNG gates [12].

In another study, a parity-preserving unsigned reversible multiplier circuit was designed [11]. Valinataj presented two parity-preserving reversible unsigned multiplier circuits [35].

Additionally, Qi et al. [31] presented a parity-preserving reversible signed multiplier circuit and Valinataj a parity-preserving reversible signed multiplier circuit [35].

Having a minimum GARBAGE OUTPUT is considered as one of the targets [1, 16, 21, 26]. These circuits reuse fixed inputs to reduce the number of circuit lines and redundant outputs. The study by [21] is regarded as the best study performed in terms of T-count, qubits, and CONSTANT INPUTs. Meanwhile, regarding the circuit design method presented in [1, 16, 21, 26], the QUANTUM COST of the circuit increased

**Fig. 4** The first proposed parity-preserving reversible block (E1)



owing to the redundancy of the gates required to convert CONSTANT INPUTs to their original values. These circuits require a low number of CONSTANT INPUTs and yield a small number of GARBAGE OUTPUTs; however, they incur a high QUANTUM COST. Therefore, the QUANTUM COST and the number of CONSTANT INPUTs are inversely correlated. In fact, the QUANTUM COST increases when the number of circuit lines is decreased.

The abovementioned methods can be used when the importance of the QUANTUM COST is low [21]. Otherwise, the proposed designs can be used as the best designs to date.

## 4 The Proposed Parity-Preserving Reversible Multipliers

In the present study, four parity-preserving reversible multiplier circuits are presented. The first and second designs are parity-preserving reversible unsigned circuits. In the third and fourth plans, two parity-preserving reversible signed circuits are proposed.

### 4.1 First Block

The first proposed block is a parity-preserving circuit with four inputs and four outputs. Figure 4 illustrates the first block in the quantum structure, denoted E1. If C and D are 0, then AB appears in the R and S outputs. Furthermore, it is used as a Fan-OUT. The QUANTUM COST of the proposed block E1 is 6.

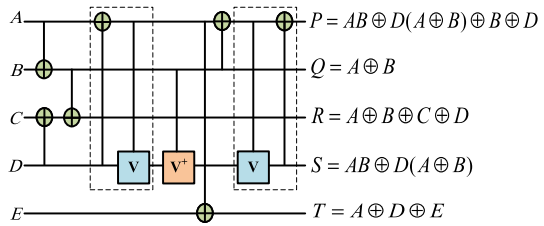
### 4.2 Second Block

The second block comprises a parity-preserving circuit with five inputs and five outputs. Figure 5 shows the second block, denoted E2. If the D and E inputs are 0, then sum and carry values exist in the S and R outputs, respectively. The QUANTUM COST of the E2 block is 8.

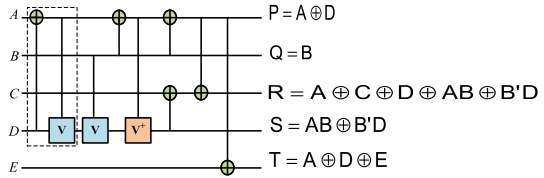
### 4.3 Third Block

The third block is a parity-preserving reversible circuit with five inputs and five outputs. The third block design provides a parity-preserving block for the synchronous part of the output functions of a  $2 \times 2$  multiplication circuit. In designing the third block, we

**Fig. 5** The second proposed parity-preserving reversible block (E2)



**Fig. 6** The third proposed parity-preserving reversible block (E3)



attempted to reduce the QUANTUM COST as much as possible. Figure 6 shows the third block in the quantum structure, denoted E3. The QUANTUM COST of E3 is 8.

**4.4 Parity-Preserving Reversible 4 × 4 Unsigned Multiplier**

The reversible unsigned multiplier operation was categorized into two parts. First, the partial product generation (PPG) operation was performed, which generated AND results for multiplier operations. In the second section of the circuit, a partial product addition (PPA) circuit was used.

In the PPG section, 16 AND functions are required. These functions were developed using NFT gates and E1 blocks. Figure 7 illustrates the PPG circuit.

The PPG design of the reversible unsigned multiplier circuit requires seven NFT gates and nine E1 blocks.

A significant improvement was achieved by separating the multiplier circuit into two sections. The first section of this design includes 2 × 2 multiplier circuits, and the second section encompasses the remaining multiplication parts.

In this circuit, an optimal parity-preserving circuit is presented using QUANTUM COST optimization blocks. Figure 8 shows the proposed PPA circuit in the reversible unsigned circuit.

Four HAs and eight FAs are necessary for designing a PPA circuit in a reversible 4 × 4 unsigned multiplier circuit. In the suggested PPA circuit (Fig. 8), E2 blocks were used to generate a full adder. The results obtained in the PPG section should be considered in PPA computations. Hence, the E1(A), E1(B), E3(A), and E3(B) blocks and two other E1 blocks contribute to the final results of the 2 × 2 multiplier.

**4.5 Parity-Preserving Reversible N × N Unsigned Multiplier**

Designing a circuit in variable sizes is necessary for designing a 4 × 4 reversible unsigned multiplier circuit. Similar to the previous design, it contains two PPG and

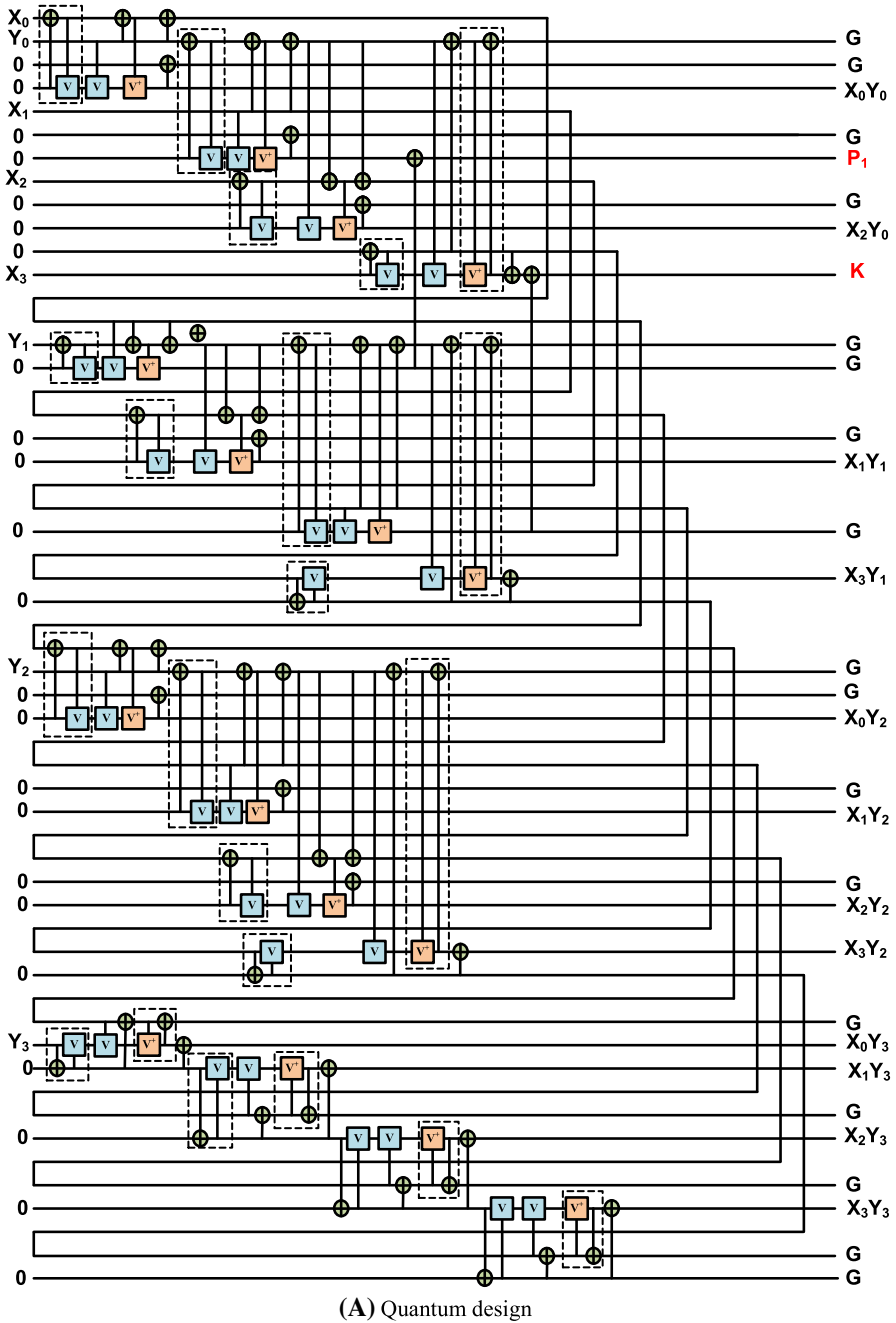


Fig. 7 Partial product generation circuit in parity-preserving reversible unsigned  $4 \times 4$  multiplier circuit

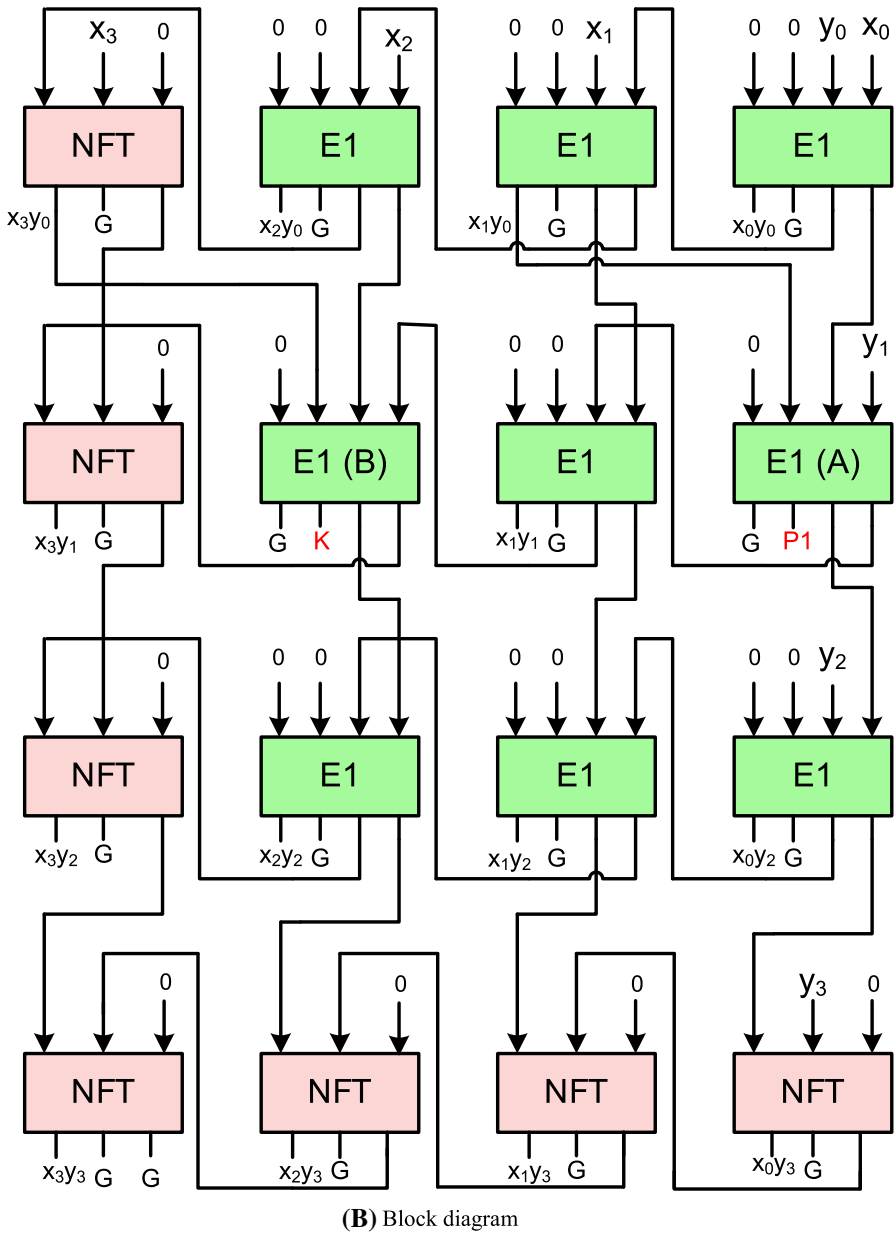
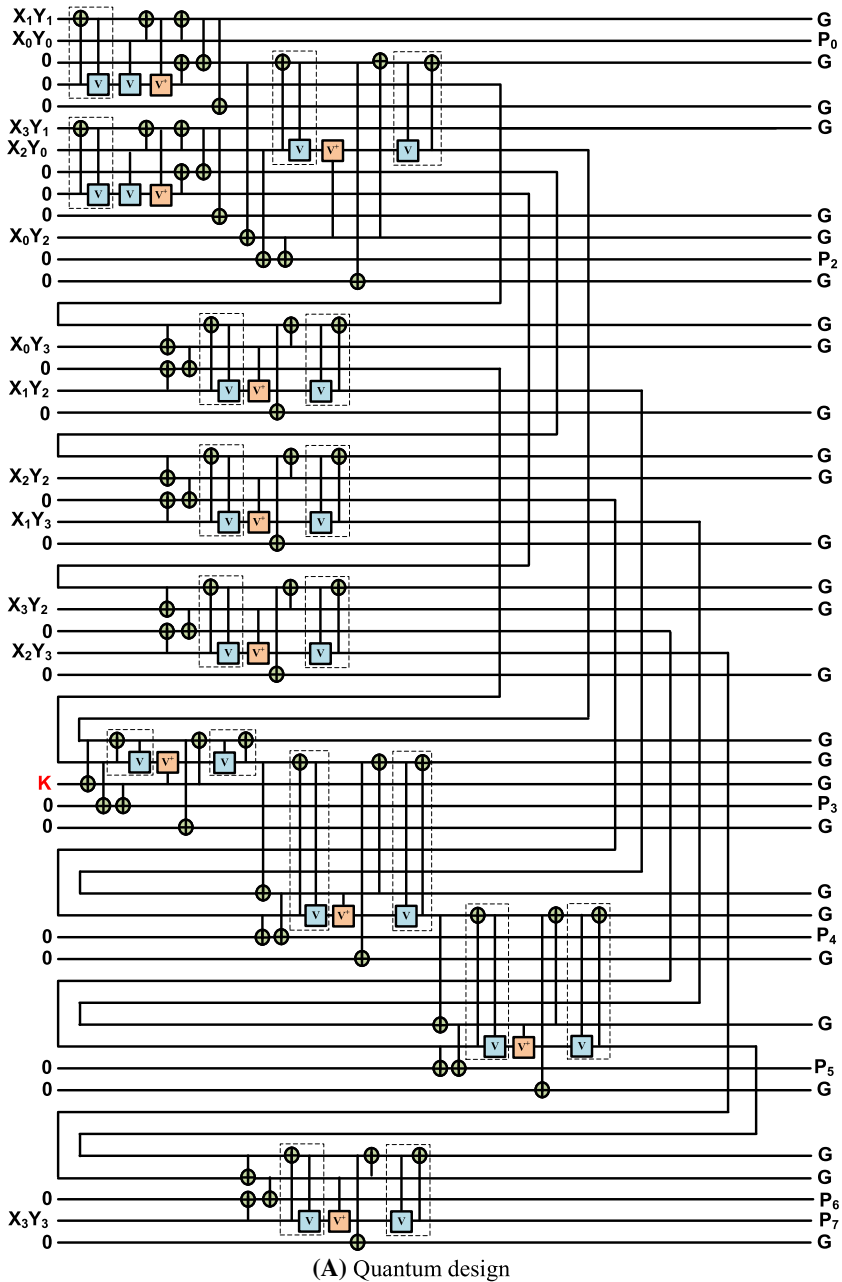


Fig. 7 continued

PPA sections. In this design, NFT gates and E1 blocks were used to for PPG. Figure 9 illustrates the PPG in an  $N \times N$  unsigned parity-preserving reversible multiplier circuit.





**Fig. 8** Partial product addition circuit in the proposed parity-preserving reversible unsigned  $4 \times 4$  multiplier circuit

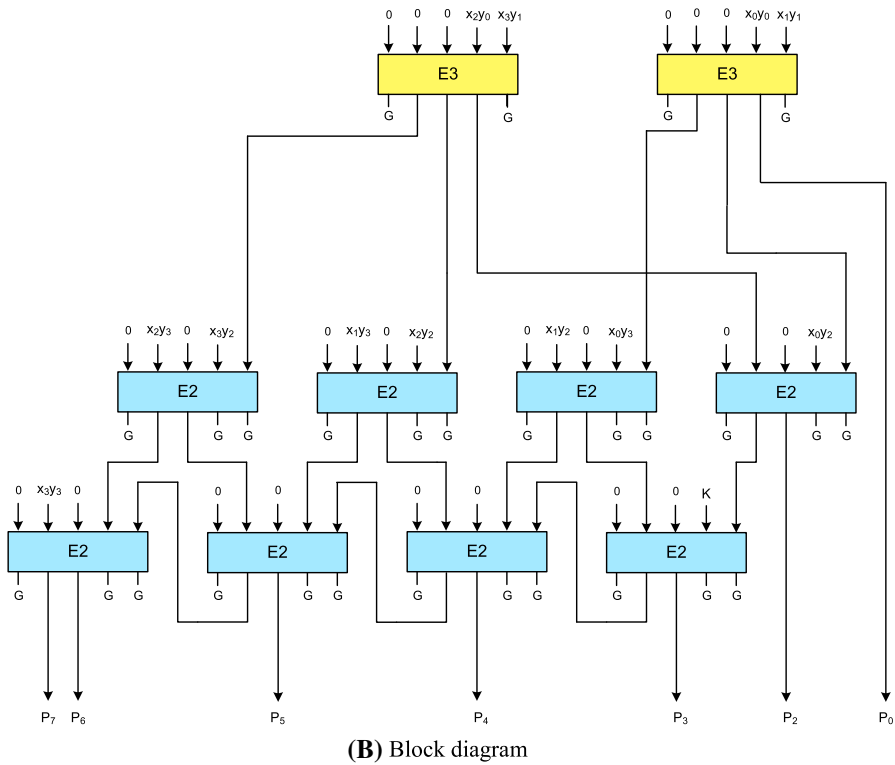


Fig. 8 continued

No additional gate or block is necessary for implementing half adders.

In this circuit,  $N$  blocks of HA and  $N \times (N - 2)$  FA blocks are required. We used the E3 block in PPA to complete the results of PPG. The E2 block was used to create the FA function in an  $N \times N$  design. Figure 10 displays the PPA generator circuit in  $N \times N$  dimensions for producing a parity-preserving unsigned reversible multiplier circuit.

As shown in Fig. 10, the E2 and E3 blocks were used to generate the PPA circuit.

The sum of QUANTUM COST of the PPA and PPG is illustrated in Eq. (5)

$$QC = 14(N^2 - N) + 1. \tag{5}$$

Equation (6) indicates the QUANTUM COST of the circuit with respect to  $N$

$$\text{No. CI} = 4N^2 - 5N + 1. \tag{6}$$

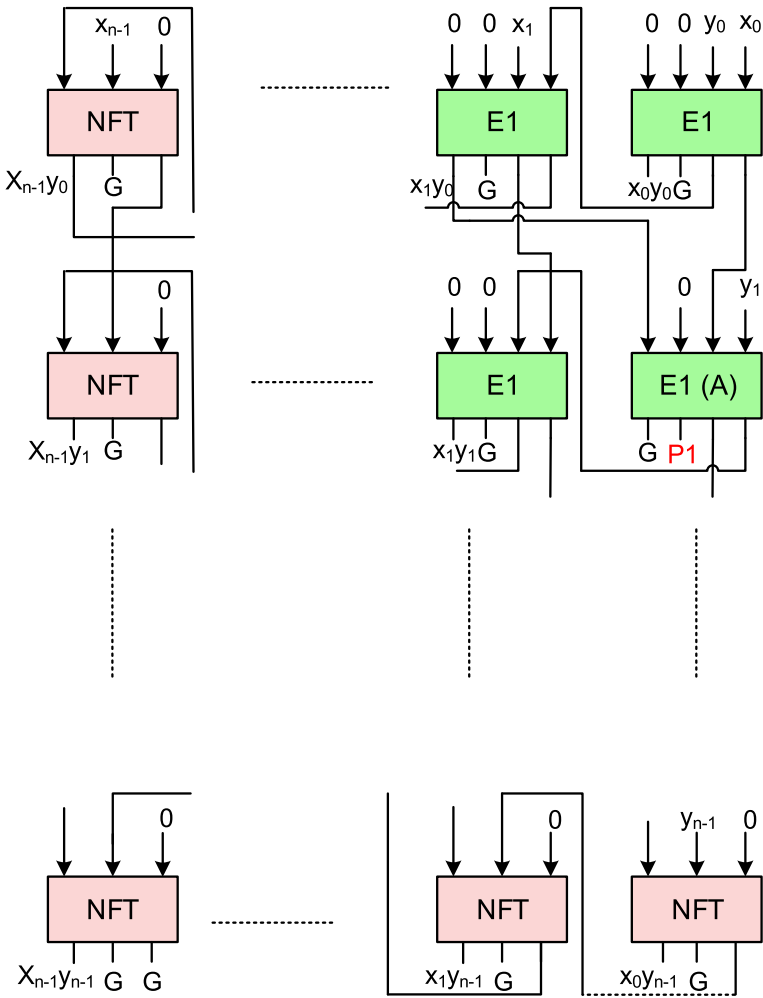


Fig. 9 Parity-preserving reversible unsigned  $N \times N$  partial product generation circuit

Equation (7) represents the number of GARBAGE OUTPUTS.

$$\text{No. GO} = 4N^2 - 5N + 1 \tag{7}$$

### 4.6 Parity-Preserving Reversible 5 x 5 Signed Multiplier

In this section, a  $5 \times 5$  parity-preserving signed reversible multiplier circuit is proposed; 17 ANDs and eight NANDs are required. We used E1 blocks and NFT gates to obtain PPG outputs. Because the NFT gate incurs less QUANTUM COST than block E1, NFT gates are preferable for the production of required ANDs and NANDs. Figure 11 illustrates the parity-preserving signed reversible multiplier PPG circuit.

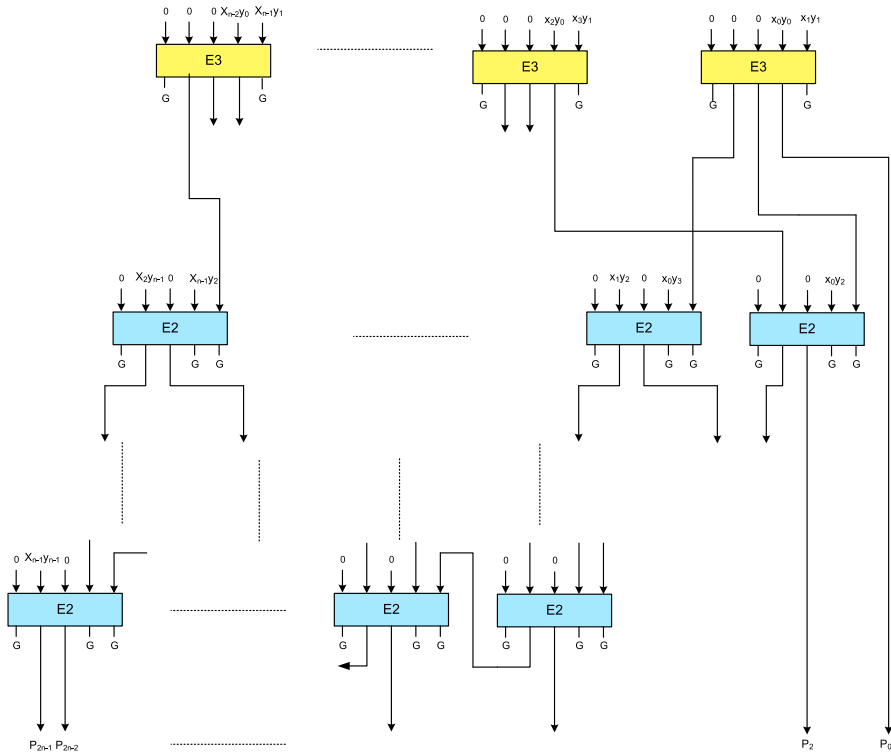


Fig. 10 Parity-preserving reversible unsigned  $N \times N$  partial product addition circuit

As shown in Fig. 11, seven NFT gates and 18 E1 blocks are required. One of the inputs must be set to logical 1 to obtain a NAND gate.

As illustrated in Fig. 12, two E3 blocks and 16 E2 blocks are required; the E3 blocks were used to complete the function of a  $2 \times 2$  multiplier.

#### 4.7 Parity-Preserving Reversible $N \times N$ Signed Multiplier

An  $N \times N$  parity-preserving reversible signed multiplier circuit is presented. Figure 13 illustrates the PPG circuit in the parity-preserving reversible signed  $N \times N$  multiplier circuit.

In the  $N \times N$  PPG circuit, the number of E1 blocks is  $(N - 1)^2 + 2$  and the number of NFT gates is  $2N - 3$ .

Figure 14 shows the  $N \times N$  parity-preserving reversible signed multiplier circuit.

As shown in Fig. 14, the number of E2 blocks for an  $N \times N$  multiplication is  $(N - 1)^2$ . Combining the circuits in Figs. 13 and 14 produces the multiplication of the parity-preserving reversible signed  $N \times N$  numbers.

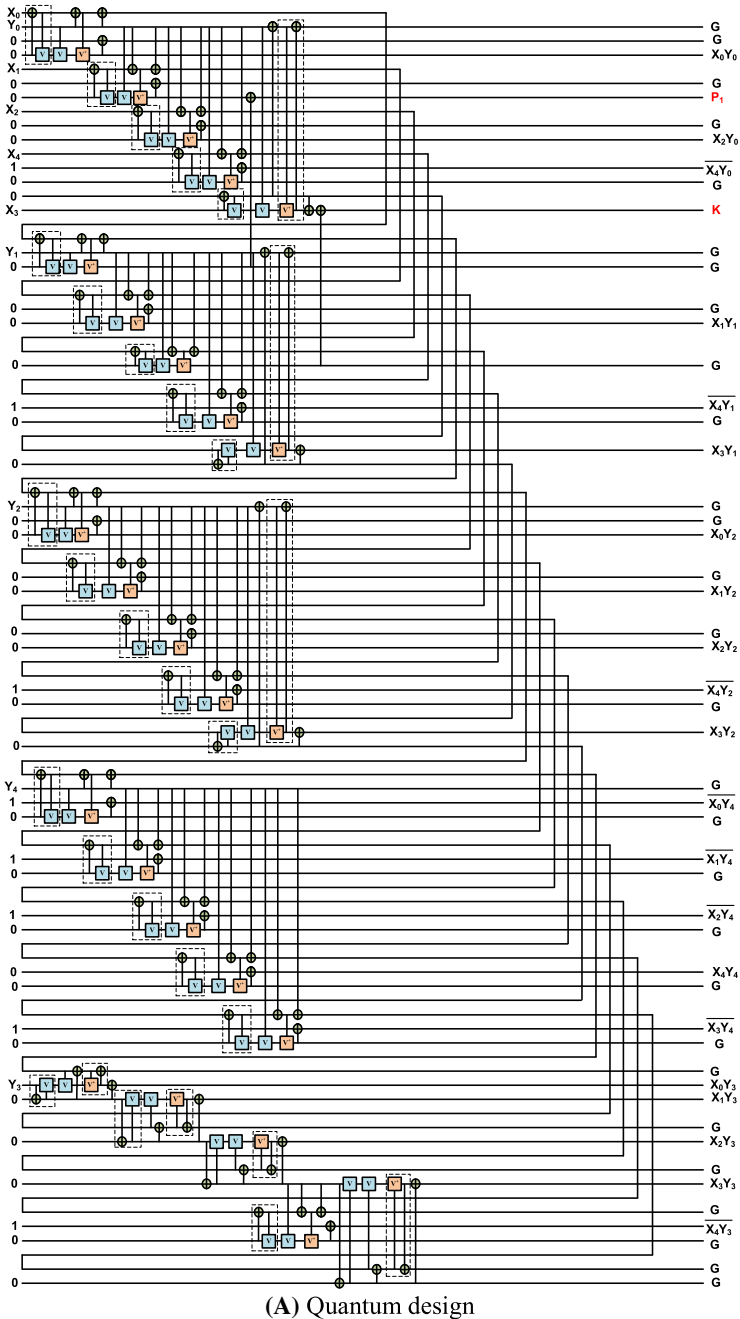
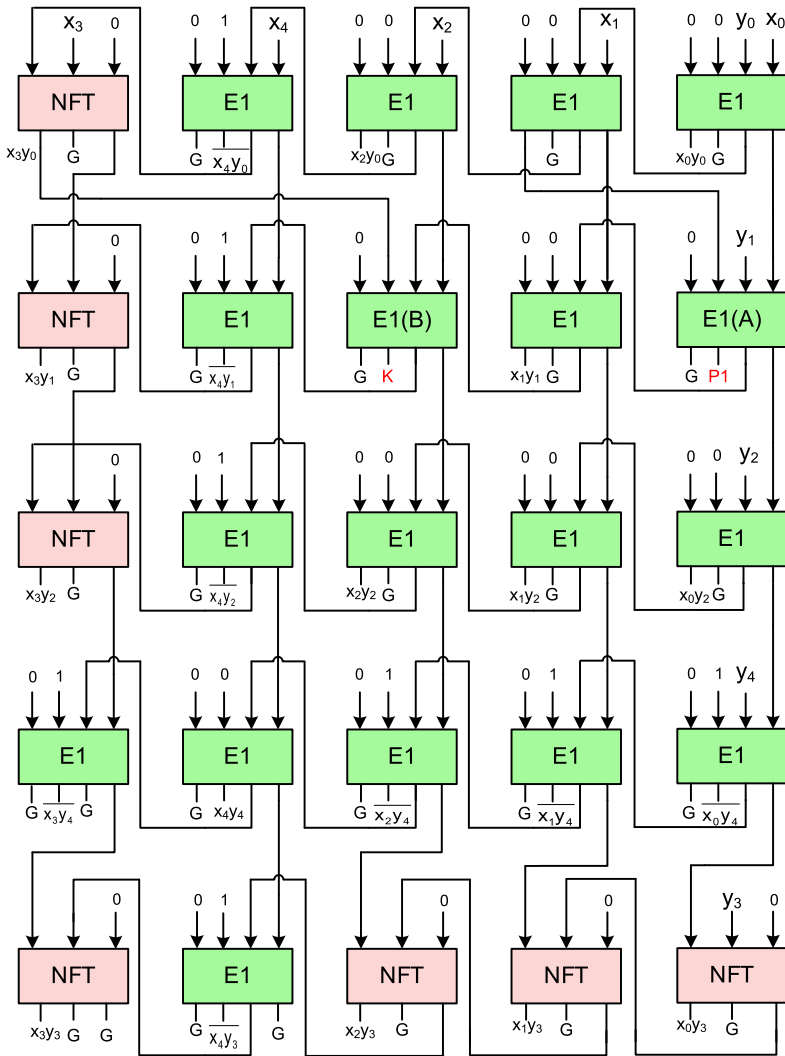


Fig. 11 Parity-preserving reversible signed  $5 \times 5$  partial product generation circuit



(B) Block diagram

Fig. 11 continued

The QUANTUM COST of the signed multiplier circuit is shown in Eq. (8)

$$Q_c = 14N^2 - 18N + 13 + 8 * \frac{N}{2}. \tag{8}$$

Equation (9) displays the number of CONSTANT INPUTS

$$\text{NO. CI} = 4N^2 - 6N + 8 + 2 * \frac{N}{2}. \tag{9}$$

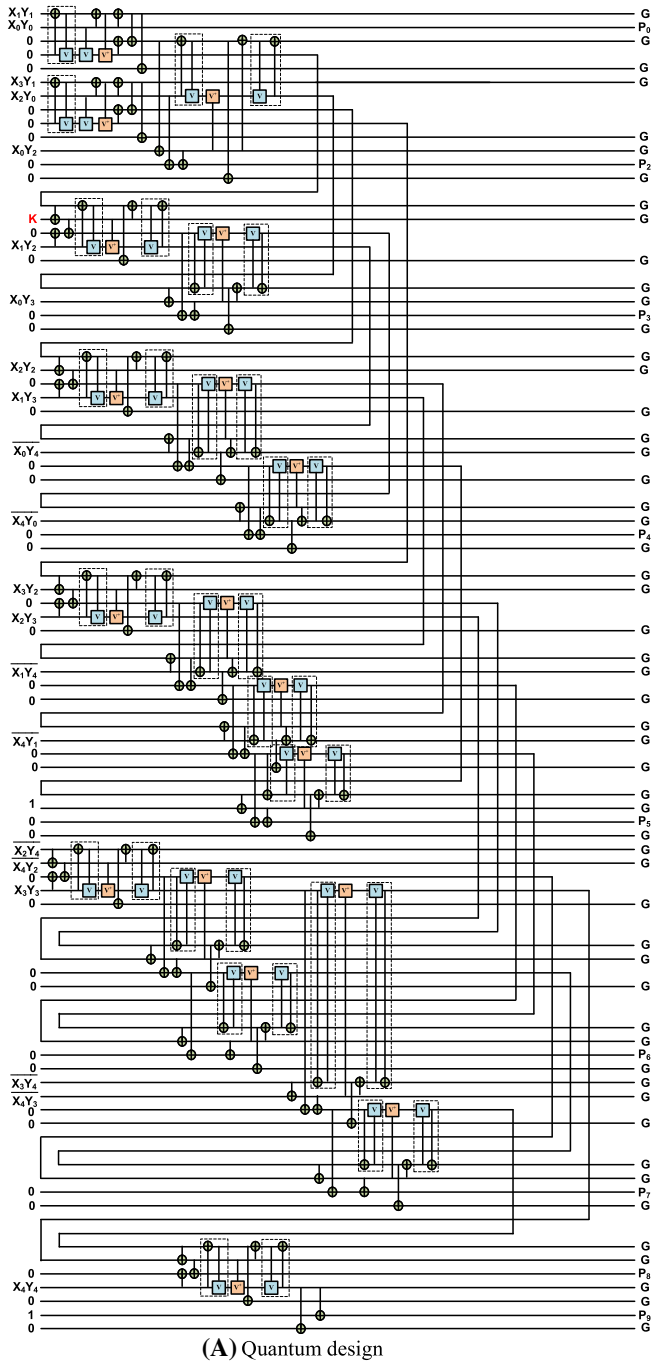
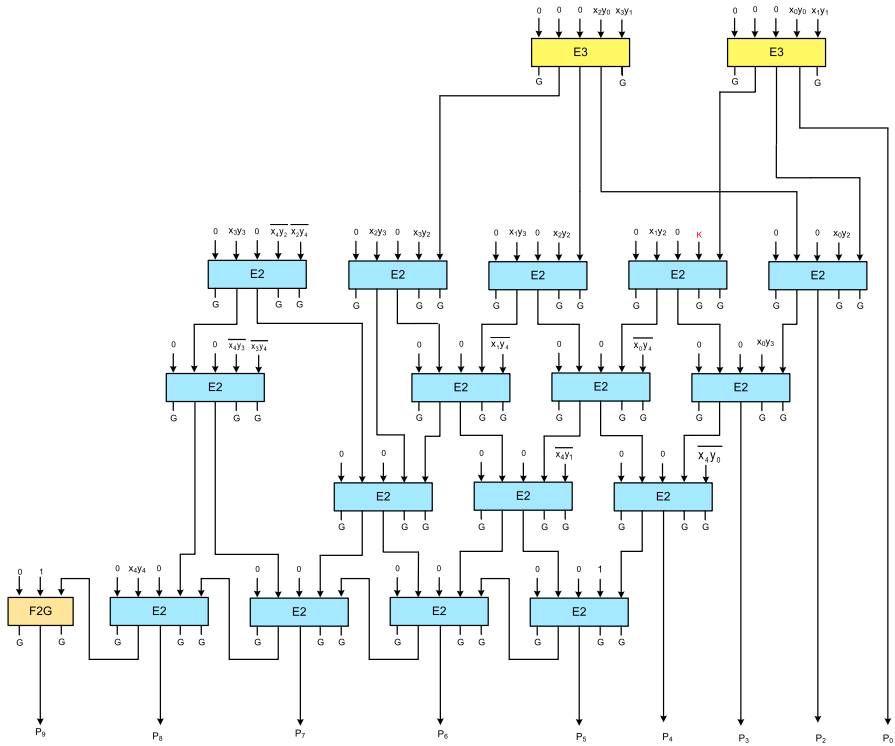


Fig. 12 Parity-preserving reversible signed  $5 \times 5$  partial product addition circuit



(B) Block diagram

Fig. 12 continued

Equation (10) represents the number of GARBAGE OUTPUTS.

$$\text{NO. GO} = 4N^2 - 6N + 8 + 2 * \frac{N}{2} \tag{10}$$

### 5 Evaluation of the Proposed Reversible Multiplier Circuit

In this section, the proposed parity-preserving  $4 \times 4$  and  $N \times N$  reversible unsigned multiplier circuits are analyzed. Subsequently, the parity-preserving  $5 \times 5$  and  $N \times N$  reversible signed multiplier circuits are evaluated.

Table 1 shows a comparison between this parity-preserving reversible unsigned multiplier circuit and those of previous studies.

As shown in Table 1, this parity-preserving  $4 \times 4$  reversible unsigned multiplier circuit contains 45 CONSTANT INPUTs and 45 GARBAGE OUTPUTs; its QUANTUM COST is 169. This circuit is considerably better than those of previous studies in terms of the number of CONSTANT INPUTs, number of GARBAGE OUTPUTs, and QUANTUM COST.



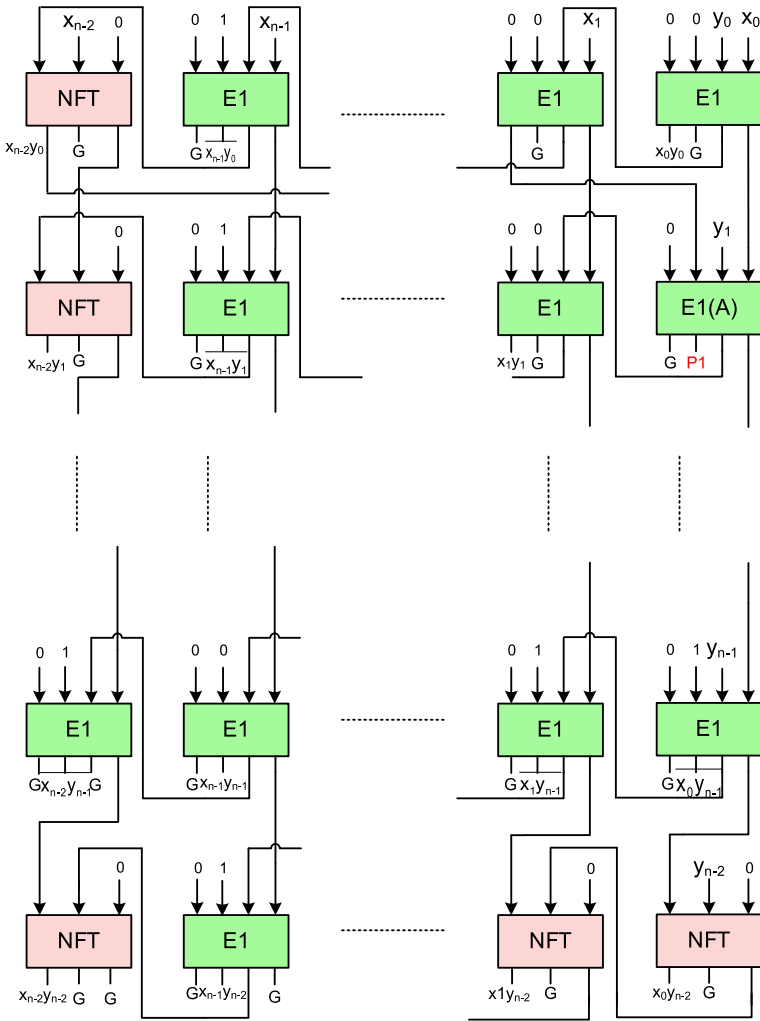


Fig. 13 Parity-preserving reversible signed  $N \times N$  partial product generation circuit

Considering all the evaluation criteria, the  $4 \times 4$  parity-preserving reversible unsigned multiplier circuit exhibited the best result compared with those of previous studies.

Table 2 shows a comparison between our  $N \times N$  reversible unsigned multiplier circuit and those of previous studies.

As shown in Table 2, the efficiency increased in three criteria related to the number of CONSTANT INPUTS, number of GARBAGE OUTPUTS, and QUANTUM COST.

Table 3 shows a comparison between the performances of the  $5 \times 5$  signed multiplier circuit and state-of-the-art signed multiplier circuits.

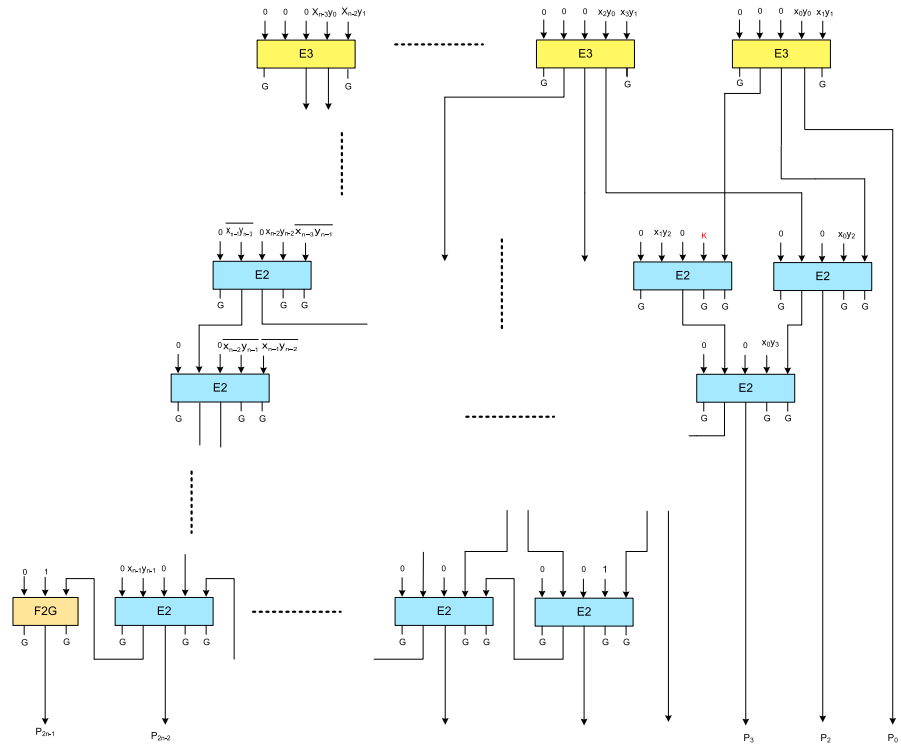


Fig. 14 Parity-preserving reversible signed  $N \times N$  partial product addition circuit

Table 1 Comparison of different parity-preserving reversible  $4 \times 4$  unsigned multipliers

	No. of CONSTANT INPUTs	No. of GARBAGE OUTPUTs	QUANTUM COST
The proposed method	45	45	169
Jamal [11]	49	49	205
Valinataj [35] (first approach)	56	56	184
Valinataj [35] (second approach)	49	49	177

As shown, the  $5 \times 5$  reversible signed multiplier circuit demonstrated the best result compared with those in previous studies.

Table 4 shows the results compared with those in [8].

The results indicated improvements in terms of the QUANTUM COST and numbers of CONSTANT INPUTs and GARBAGE OUTPUTs compared with those in [35].

**Table 2** Comparison of different parity-preserving reversible  $N \times N$  unsigned multipliers

	No. of CONSTANT INPUTs	No. of GARBAGE OUTPUTs	QUANTUM COST
The proposed method	$4N^2 - 5N + 1$	$4N^2 - 5N + 1$	$14(N^2 - N) + 1$
Valinataj [35] (first approach)	$3N^2 + 2N * (\frac{N}{2} - 1)$	$4N^2 - 3N$	$13N^2 + 2N * \frac{N}{2} + 10N$
Valinataj [35] (second approach)	$4N^2 - 4N + 1$	$4N^2 - 4N + 1$	$14N^2 - 12N + 1$

**Table 3** Comparison of different parity-preserving reversible  $5 \times 5$  signed multipliers

	No. of CONSTANT INPUTs	No. of GARBAGE OUTPUTs	QUANTUM COST
The proposed method	82	82	289
Qi [31]	90	90	401
Valinataj [35]	86	86	297

**Table 4** Comparison of different parity-preserving reversible  $N \times N$  signed multipliers

	No. of CONSTANT INPUT	No. of GARBAGE OUTPUT	QUANTUM COST
The proposed method	$4N^2 - 6N + 8 + 2 * \frac{N}{2}$	$4N^2 - 6N + 8 + 2 * \frac{N}{2}$	$14N^2 - 18N + 13 + 8 * \frac{N}{2}$
Valinataj [35]	$4N^2 - 4N + 6$	$4N^2 - 4N + 6$	$14N^2 - 12N + 7$

## 6 Conclusion

We herein presented parity-preserving reversible multiplier circuits. First, three parity-preserving reversible blocks were presented and a parity-preserving reversible  $4 \times 4$  unsigned multiplier circuit was designed using these blocks. Based on the results, the proposed circuit demonstrated the best performance compared with those of previous studies. In addition, an  $N \times N$  reversible unsigned multiplier circuit was proposed, along with relevant equations for computing the circuit costs. Regarding the number of CONSTANT INPUTs and GARBAGE OUTPUTs, the unsigned multiplier circuit demonstrated better results compared with those of previous studies. Furthermore, a parity-preserving reversible  $5 \times 5$  signed multiplier was presented, along with an  $N \times N$  parity-preserving one. The results proved that our circuit demonstrated the best efficiency. The performance evaluation of these designs indicated a significant improvement in terms of the QUANTUM COST and the numbers of CONSTANT INPUTs and GARBAGE OUTPUTs compared with previous studies.

**Acknowledgements** The authors would like to thank Prof. Nader Bagherzadeh, Eng. Elika Navi, and Eng. Pegah Foroutan for their contribution.

## References

1. H.M.H. Babu, Cost-efficient design of a quantum multiplier–accumulator unit. *Quantum Inf. Process.* **16**(1), 30 (2016). <https://doi.org/10.1007/s11128-016-1455-0>
2. C.H. Bennett, Logical reversibility of computation. *IBM J. Res. Dev.* **17**, 525–532 (1973)
3. K. Bhardwaj, M. Deshpande, K-Algorithm: an improved Booth's recoding for optimal fault tolerant reversible multiplier, in *26th International Conference on VLSI Design* (2013), pp. 362–367
4. X.-D. Cai, D. Wu, Z.-E. Su, M.-C. Chen, X.-L. Wang, L. Li, N.-L. Liu, C.-Y. Lu, J.-W. Pan, Entanglement-based machine learning on a quantum computer. *Phys. Rev. Lett.* **114**(11), 110504 (2015)
5. R. Feynman, Quantum mechanical computers. *Opt. News* **11**, 11–20 (1985)
6. E. Fredkin, T. Toffoli, Conservative logic. *Int. J. Theor. Phys.* **21**, 219–253 (1982)
7. M. Haghparast, Design and implementation of nanometric fault tolerant reversible BCD adder. *Aust. J. Basic Appl. Sci.* **5**(10), 896–901 (2011)
8. M. Haghparast, M. Mohammadi, K. Navi, M. Eshghi, Optimized reversible multiplier circuit. *J. Circuits Syst. Comput.* **18**(2), 311–323 (2009)
9. A.P. Hatkar, A.A. Hatkar, N.P. Narkhede, ASIC design of reversible multiplier circuit, in *Proceedings of International Conference on Electronic Systems, Signal Processing and Computing Technologies* (2014), pp. 47–52
10. M.S. Islam, M.M. Rahman, Z. Begum, M.Z. Hafiz, Fault tolerant reversible logic synthesis: carry look-ahead and carry skip adders, in *International Conference on Advances in Computational Tools for Engineering Applications (ACTEA)* (2009), pp. 396–401
11. L. Jamal, M.M. Rahman, H.M.H. Babu, An optimal design of a fault tolerant reversible multiplier, in *IEEE 26th International SOC Conference (SOCC)* (2013), pp. 37–42
12. M.V. Jigalur, M.S. Meharunnis, Efficient reversible multiplier using column bypass technique for DSP applications. *Int. J. Eng. Res. Gen. Sci.* **3**(1), 91–97 (2015)
13. S. Kotiyal, H. Thapliyal, N. Ranganathan, Reversible logic based multiplication computing unit using binary tree data structure. *J. Supercomput.* **71**, 2668–2693 (2015)
14. S. Kotiyal, H. Thapliyal, N. Ranganathan, Circuit for reversible quantum multiplier based on binary tree optimizing Ancilla and Garbage bits, in *Proceedings of 27th International Conference on VLSI Design (VLSID)* (2014), pp. 545–550
15. R. Landauer, Irreversibility and heat generation in the computing process. *IBM J. Res. Dev.* **5**(3), 183–191 (1961)
16. C.C. Lin, A. Chakrabarti, N.K. Jha, QLib: quantum module library. *J. Emerg. Technol. Comput. Syst.* **11**(1), 7:1–7:20 (2014). <https://doi.org/10.1145/2629430>
17. D. Maslov, G.W. Dueck, Reversible cascades with minimal garbage. *IEEE Trans. CAD Integr. Circuits Syst.* **23**(11), 1497–1509 (2004)
18. M.Z. Moghadam, K. Navi, Ultra-area-efficient reversible multiplier. *Microelectron. J.* **43**, 377–385 (2012)
19. Z.M. Moghadam, K. Navi, M. Kalemami, A novel reversible design for double edge triggered flip-flops and new designs of reversible sequential circuits. *Int. J. Comput. Syst. Sci. Eng.* **29**, 197–204 (2014)
20. V.G. Moshnyaga, Design of minimum complexity reversible multiplier, in *Proceedings of IEEE Region 10 Conference (TENCON)* (2015), pp. 1–4
21. C.E. Muñoz, H. Thapliyal, Quantum circuit design of a T-count optimized integer multiplier. *IEEE Trans. Comput.* **68**(5), 729–739 (2019). <https://doi.org/10.1109/tc.2018.2882774>
22. M.A. Nielsen, I.L. Chuang, *Quantum computation and quantum information* (Cambridge University Press, Cambridge, 2000)
23. B. Parhami, Fault tolerant reversible circuits, in *Proceedings 40th Asilomar Conference Signals, Systems, and Computers, Pacific Grove, CA* (2006)
24. B. Parhami, *Computer Arithmetic—Algorithm and Hardware Designs* (Oxford University Press, Oxford, 2000)
25. A. Peres, Reversible logic and quantum computers. *Phys. Rev.* **32**, 3266–3276 (1985)
26. L.R. Perez, J.C.G. Escartin, Quantum arithmetic with the quantum Fourier transform. *Quantum Inf. Process.* **16**(6), 152 (2017). <https://doi.org/10.1007/s11128-017-1603-1>
27. M. Perkowski, A. Al-Rabadi, P. Kerntopf, A. Buller, M. Chrzanowska-Jeske, A. Mishchenko, et al., A general decomposition for reversible logic, in *Proceedings of RM* (2001), pp. 119–38

28. E. PourAliAkbar, M. Haghparast, K. Navi, Novel design of a fast reversible Wallace sign multiplier circuit in nanotechnology. *Microelectron. J.* **42**, 973–981 (2011)
29. E. PourAliAkbar, M. Mosleh, An efficient design for reversible wallace unsigned multiplier. *Theor. Comput. Sci.* **773**, 43–52 (2018)
30. N. Przigoda, G. Dueck, R. Wille, R. Drechsler, Fault detection in parity preserving reversible circuit, in *2016 IEEE 46th International Symposium on Multiple-Valued Logic* (2016)
31. X. Qi, F. Chen, Design of fast fault tolerant reversible signed multiplier. *Int. J. Phys. Sci.* **7**(17), 2506–2514 (2012)
32. H. Thapliyal, M.B. Srinivas, Novel reversible multiplier architecture using reversible TSG gate, in *Proceedings of the IEEE International Conference on Computer Systems and Applications* (2006), pp. 100–103
33. H. Thapliyal, M.B. Srinivas, Novel reversible TSG gate and its application for designing reversible carry look ahead adder and other adder architectures, in *Proceedings of the 10th Asia-Pacific Computer Systems Architecture Conference (ACSAC 05). Lecture Notes of Computer Science 3740* (Springer, 2005), pp. 775–786
34. T. Toffoli, Reversible computing. Technical memo MIT/LCS/TM-151, MIT Lab. for Computer Science (1980)
35. M. Valinataj, Novel parity-preserving reversible logic array multipliers. *J. Supercomput.* **73**, 4843–4867 (2017)
36. R. Zhou, Y. Shi, H. Wanga, J. Cao, Transistor realization of reversible “ZS” series gates and reversible array multiplier. *Microelectron. J.* **42**, 305–315 (2011)

**Publisher's Note** Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.