SHORT PAPER

A 99.43% Energy Saving Switching Scheme with Asymmetric Binary Search Algorithm for SAR ADCs

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Abstract

In this paper, a low-energy switching scheme based on the asymmetric binary search algorithm for successive approximation register (SAR) analog-to-digital converters (ADCs) is proposed. To reduce switching energy and area, the proposed scheme uses the single-side switching method and the least significant bit (LSB) capacitor is split into two one-half unit capacitors. Using the series capacitance scheme, the capacitance mismatch caused by process deviation is effectively improved. Compared with the conventional switching method, the switching energy of this scheme is decreased by 99.43% and the area is saved by 87.2%. MATLAB simulation results show that this scheme also has a low nonlinearity that the maximum differential nonlinearity is only 0.37 LSB and the maximum integral nonlinearity is only 0.43 LSB.

Keywords SAR ADCs · Switching scheme · Asymmetric binary search algorithm · Low-energy

1 Introduction

The Internet-of-Things (IOT) or even the Internet-of-Everything (IOE) has greatly promoted the development of low-power integrated circuits in the past decade [4, 8, 11]. As a bridge between analog and digital circuits, the ADC is an indispensable

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module in the IOE systems. The performance of the ADC will directly determine the performance of the entire IOE. Therefore, designing an ADC with low power becomes especially important.

Compared with several ADCs, SAR ADC has been paid more and more attention to by scholars because of its high efficiency [15]. For capacitive SAR ADC, the capacitor arrays of the digital-to-analog converter (DAC) may result in significant switching energy drawn from the reference voltages during conversion. To avoid the limitation, various approaches have been proposed. Recently, several schemes have been presented to reduce the switching energy and also the chip area, such as the capacitor-splitting scheme [9, 12], V_{CM}-based scheme [10], tri-level scheme [13], and V_{CM}-based monotonic scheme [14]. In this paper, a new switching method based on the asymmetric binary algorithm is presented, which splits the LSB capacitor into two one-half unit capacitors. Compared with the switching schemes proposed above, the proposed switching method achieves the most energy efficient by using three reference voltages: V_{REF}, V_{CM}, and GND.

The following sections are organized as follows. Section 2 introduces the comparison between the conventional binary search algorithm and the asymmetric binary search algorithm. Section 3 presents the proposed switching scheme. Section 4 gives the simulation results of the switching energy. Section 5 shows the simulation results of linearity and mismatch. Section 6 is a brief conclusion about this paper.

2 Comparison of Binary Search Algorithms

Figure 1a shows a 4-bit switching example of the conventional binary search algorithm. In the conventional binary switching method, the MSB capacitor is connected to V_{REF}, and the positive input signal is compared with 1/2 V_{REF}. If the input signal is less than 1/2 V_{REF}, the most significant bit (MSB) capacitor is connected to GND, and the MSB-1 capacitor is connected to V_{REF} [3]. The subsequent operations are similar. However, charging all capacitors by order is the main reason for binary search inefficiency.

Compared with the conventional binary search, the positive input signal is firstly compared with 1/4 V_{REF} in the asymmetric binary search method. If the input signal is more than 1/4 V_{REF}, the MSB capacitor is switched to achieve the comparison between the input signal and 3/4 V_{REF}. Otherwise, the MSB-2 capacitor is switched to achieve the comparison between the input signal and 1/8 V_{REF} [1]. A 4-bit switching example is shown in Fig. 1b. Although the comparison cycles for digitizing the input signal between $\pm 1/4$ and $\pm 3/4$ V_{REF} are slightly increased, the total comparison cycles will not change. Quantizing the input signal that is less than 1/4 V_{REF} requires only three comparison cycles. Besides, the discharging operation that switching from $\pm 3/4$ to $\pm 1/2$ V_{REF} consumes less energy compared with traditional charging operation. Thus, the switching power that quantizing the input signal between 0 and $\pm 3/4$ V_{REF} is greatly reduced, and digitizing the remaining range of the input signal consumes as much energy as the conventional binary switching.
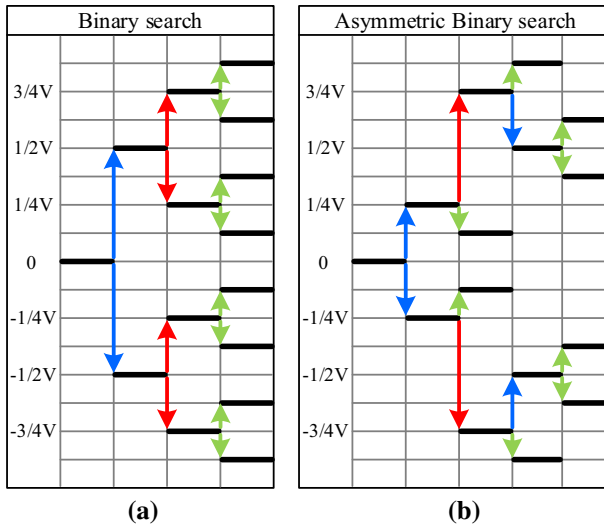
Fig. 1 Searching process of binary and asymmetric binary search algorithms. **a** Binary search (4-bit), **b** Asymmetric binary search (4-bit)

3 The Proposed Switching Scheme

The proposed switching scheme for a 5-bit SAR ADC is shown in Fig. 2. The switching energy of each step is indicated in the figure, and the switching processes A′, B′, C′, and D′ are opposite to A, B, C, and D. It is stipulated that "yes" means to switch up, and "no" means to switch down. In this design, the LSB capacitor is split into two one-half unit capacitors to avoid the process mismatch problem of small capacitors. And the one-half unit capacitor is achieved by connecting two unit capacitors in series.

In the sampling phase, the MSB capacitor is connected to GND, and the remaining capacitors are connected to V_{REF}. The input signal is sampled to the top plates of the differential capacitor arrays DACP and DACN through the sampling switches. To avoid the intermediate node floating all the time and the continuous accumulation of static electricity at the intermediate node, the intermediate node's voltage is preset to GND through a switch in each sampling phase. In the quantification phase, the switch will be turned off and the comparator performs the first comparison. When the digital code is determined, the MSB capacitor on the higher-voltage side remains unchanged, and the remaining capacitors are connected to V_{CM}, where $V_{CM} = 1/2\ V_{REF}$. And the input signal will be compared with $\pm 1/4\ V_{REF}$. Subsequently, the MSB capacitor is charged or the MSB − 1 capacitor is discharged to achieve the comparison between the input signal and $\pm 3/4\ V_{REF}$ or $\pm 1/8\ V_{REF}$. The later comparison process is like A or D. If compared with $\pm 3/4\ V_{REF}$, the input signal also needs to be compared with $\pm 1/2\ V_{REF}$ or $\pm 7/8\ V_{REF}$. If the input signal is compared with $\pm 1/2\ V_{REF}$, it is necessary to spend an extra comparison period compared with $\pm 5/8\ V_{REF}$ or $\pm 3/8\ V_{REF}$ to determine the LSB + 1 like B or C. The subsequent switching processes
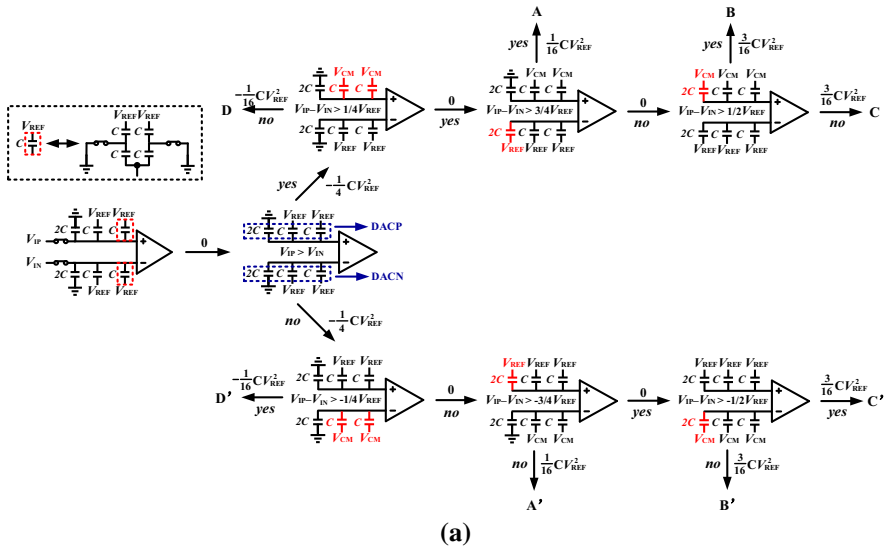
(a)

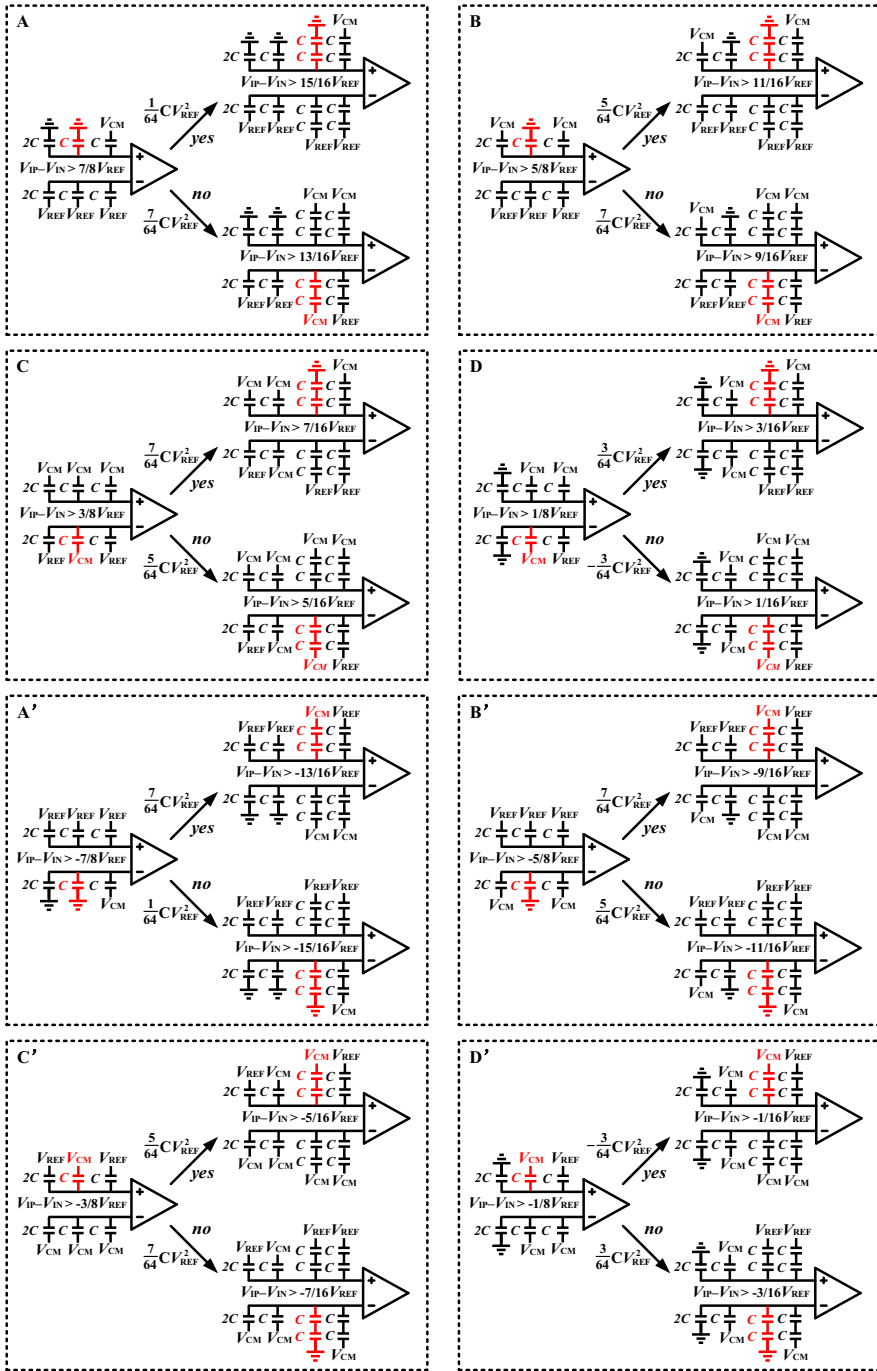**Fig. 2** Proposed switching scheme for a 5-bit SAR ADC

in A, B, C, and D follow the monotonic switching. The LSB capacitor is divided into two groups, and one of them on the higher-voltage side is switched from V_{CM} to GND or from V_{REF} to V_{CM} according to the comparison results.

In the proposed switching method, the sampling phase, the first two switching operations and the downward switching operation in D don't consume energy. Besides, the energy consumed by the remaining switching steps is not significantly increased compared with other switching methods [1, 9, 10, 12–14]. So, the proposed switching method achieves energy efficiency greatly.

Figure 3 shows the successive approximation waveform of the present scheme for a 5-bit SAR ADC and V_{REF} is equal to 1 V. Figure 3a–d, respectively, shows the successive approximation waveforms of the input signal in the range from 0 to 1/4 V_{REF}, 1/4 to 1/2 V_{REF}, 1/2 to 3/4 V_{REF}, and 3/4 to V_{REF}. As shown in Fig. 3a, it takes only four comparison cycles to get the 5-bit digital output, when the input signal is between 0 and 1/4 V_{REF}. And the digital codes are 1, 0, 1 and 1. Since the input signal is less than 1/4 V_{REF}, it is also less than 1/2 V_{REF}. Therefore, there is no need to switch the MSB capacitor to get the higher bit digital code "0." The input signal is compared with 1/8 V_{REF} and 3/16 V_{REF} in the following comparison cycles. Finally, the binary digital output is 10011. When the input signal is between 1/4 and ¾ V_{REF}, it is necessary to spend an additional comparison period getting the 5-bit digital output.

4 Switching Energy Analysis

Figure 4a shows the behavior level simulations of the proposed switching method and the existing switching methods presented in references [1, 10, 13, 14] in MATLAB. Compared with the existing switching methods, the proposed switching method consumes the lowest energy. Figure 4b shows the enlarged average switching energy of

(b)
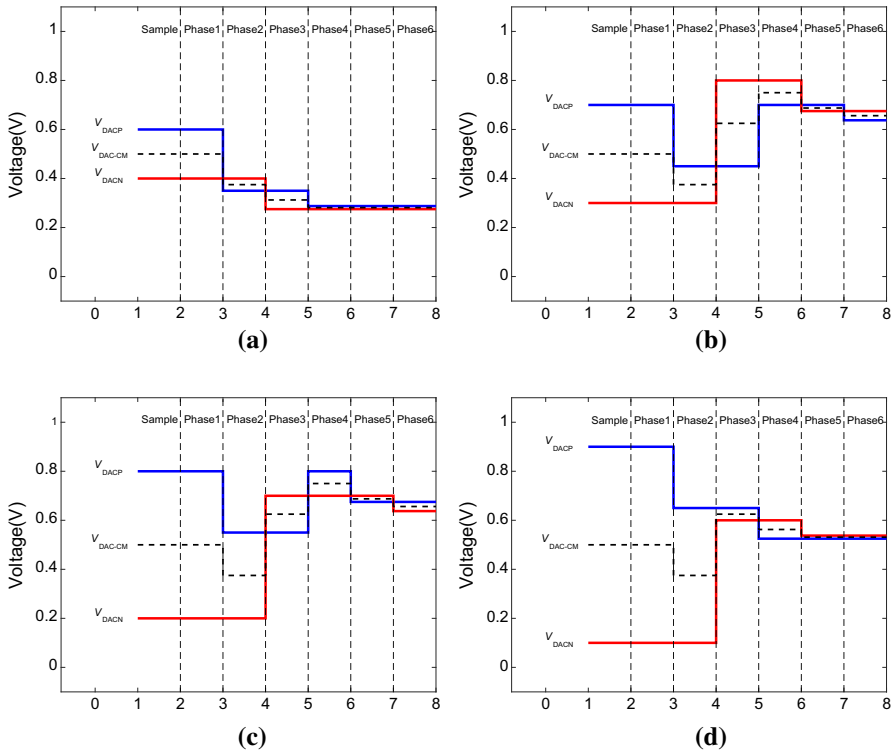
Fig. 2 continued

Fig. 3 Successive approximation waveform in four cases of 5-bit output. **a** $0 < V_{DACP} - V_{DACN} < 1/4 \, V_{REF}$, **b** $1/4 \, V_{REF} < V_{DACP} - V_{DACN} < 1/2 \, V_{REF}$, **c** $1/2 \, V_{REF} < V_{DACP} - V_{DACN} < 3/4 \, V_{REF}$, **d** $3/4 \, V_{REF} < V_{DACP} - V_{DACN} < V_{REF}$

the proposed switching scheme. It can be seen that there is a jump at 1/8, 3/8, 5/8, and 7/8 of the digital output code. These points divide the waveform into six segments that are 0–128, 129–384, 385–512, 513–640, 641–896, and 897–1024. And the six segments correspond to the six ranges of input signals that are $- V_{REF}$ to $- 3/4 \, V_{REF}$, $- 3/4 \, V_{REF}$ to $- 1/4 \, V_{REF}$, $- 1/4 \, V_{REF}$ to 0, 0 to $1/4 \, V_{REF}$, $1/4 \, V_{REF}$ to $3/4 \, V_{REF}$, and $3/4 V_{REF}$ to V_{REF}. The average switching energy of the proposed switching method is only 7.8 CV_{REF}^2. Compared with the conventional switching method [3], the proposed switching method achieves 99.43% energy reduction and 87.2% area optimization.

In Table 1, the average switching energy and the total DAC capacitor for different switching schemes are compared. The proposed switching method consumes only 7.8 CV_{REF}^2 average switching energy which results in a reduction of 99.43% over the conventional scheme. Moreover, the proposed scheme employs 262 unit capacitors and thus achieves 87.2% reduction in the total DAC capacitor compared with the conventional one. The asymmetric binary search algorithm is firstly used in [1], but its capacitors switching procedure is the V_{CM}-based switching method, which consumes a lot of switching energy. Besides, the number of unit capacitors in [1] is not further reduced compared to other switching methods. Compared with the methods in [2, 5], the proposed scheme is able to achieve similar energy saving while taking less
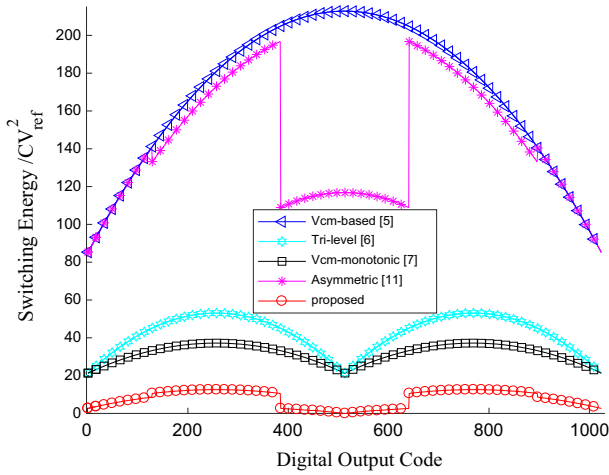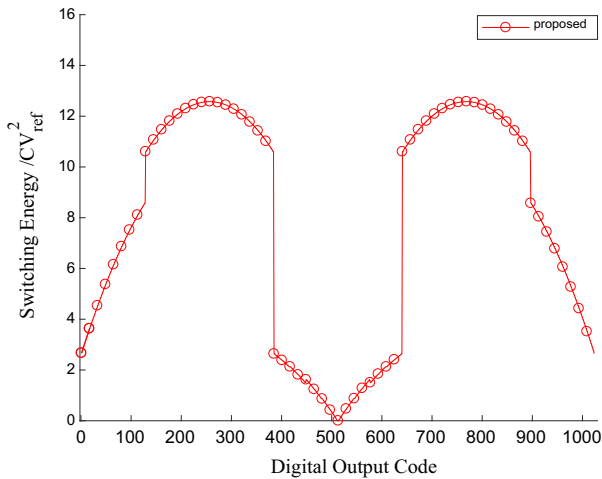
Fig. 4 Switching energy against output code. **a** Comparison between several switching methods, **b** proposed switching method

area, which will improve the switching timing requirements. In this work, the use of asymmetric binary search algorithms and the splitting LSB capacitor will increase the complexity of SAR logic. However, the measured power of the proposed scheme is extremely low when it is manufactured with the leading edge process technology.

Table 1 Comparison of different switching schemes for 10-bit DAC

Switching schemes	Number of unit capacitors	Area reduction (%)	Average switching energy $\left(CV_{REF}^2\right)$	Energy saving (%)	Logic complexity
Conventional	2048	Reference	1363.3	Reference	Low
V_{CM}-based [10]	1024	50	170.17	87.52	Low
Tri-level [13]	512	75	42.41	96.89	Medium
Zhu et al. [14]	512	75	31.88	97.66	Medium
Xie et al. [9]	512	75	42.17	96.91	Medium
Yazdani et al. [12]	1024	50	21.20	98.44	Low
Asymmetric [1]	1024	50	142.17	89.57	High
V_{aq}-Ref. [6]	256	87.5	17.6	98.71	High
Tong et al. [7]	512	75	15.8	98.84	Low
Two-stage [2]	292	85.7	2.9	99.79	Low
Multiplex [5]	288	86	8.6	99.37	Medium
This work	262	87.2	7.8	99.43	High

5 Linearity and Mismatch

The linearity of the switching scheme is directly related to the overall linearity of the SAR ADC. And the nonlinear distortion of the switching scheme is mainly caused by the mismatch of capacitors. A 10-bit SAR ADC using the proposed switching method is modeled in MATLAB. Figure 5 shows the 500 runs behavioral simulation results of INL and DNL with a mismatch of 1%. It indicates that the σ_{INL_MAX} and $\sigma_{DNL,MAX}$ of the proposed switching scheme are only 0.43 LSB and 0.37 LSB. The INL and DNL of [5], whose average switching energy is close to this work, are up to 0.451 LSB and 0.559 LSB. Thus, the proposed switching scheme has a good performance in linearity.

The accuracy of the reference voltage is critical for a multi-reference SAR ADC. And the intermediate reference voltage is usually obtained by dividing V_{REF}. However, in the actual process, due to the mismatch of the devices, the value of the reference voltage is not ideal. In order to evaluate how the accuracy of V_{CM} impacts the performance of the proposed switching scheme, the fast Fourier transform (FFT) simulation for a differential 10-bit SAR ADC is performed in MATLAB. In the scenario where the mismatch between V_{CM} and V_{REF} ranges from 0.1 to 0.5%, 500 runs are monitored and the simulation results are shown in Fig. 6. Effective number of bits (ENOB), signal-to-noise ratio (SNR), and signal-to-noise-and-distortion ratio (SNDR) are reduced by 0.26 bit, 1.61 dB, and 1.57 dB, respectively, when the mismatch between V_{CM} and V_{REF} is 0.3%. When the mismatch is 0.5%, the ENOB, SNR, and SNDR are reduced by 0.48 bit, 2.89 dB, and 2.71 dB, respectively.
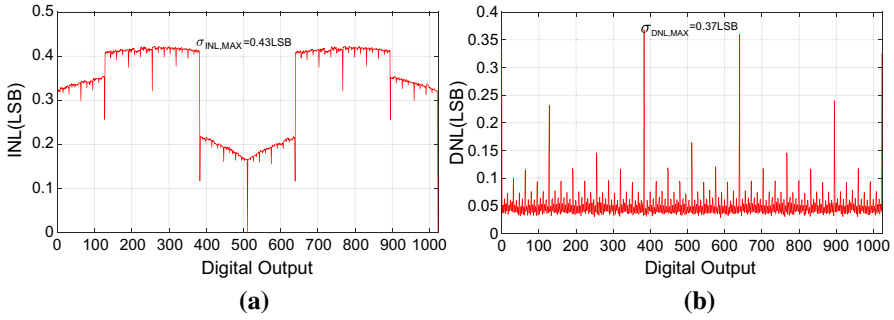
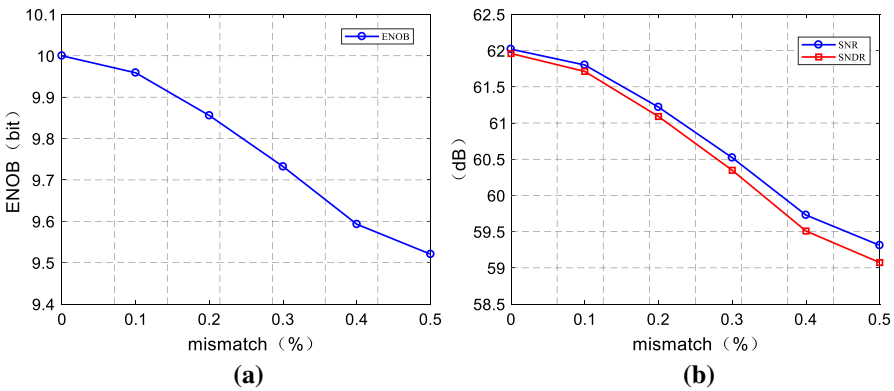**Fig. 5** Simulation results of INL and DNL. **a** INL, **b** DNL

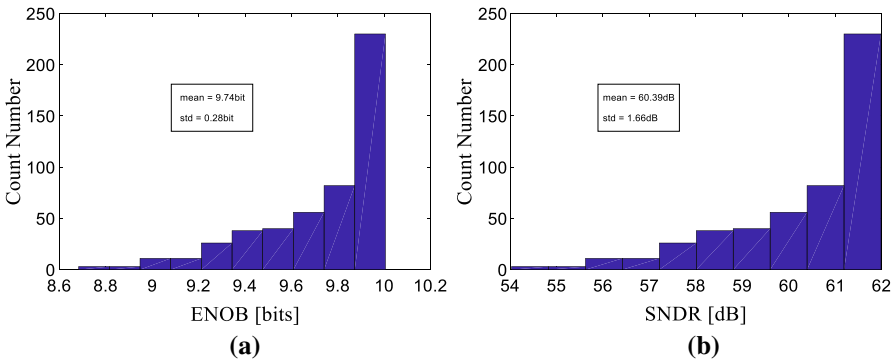**Fig. 6** Effect of mismatch on ENOB, SNR, and SNDR. **a** ENOB, **b** SNR and SNDR

Fig. 7 Histogram of ENOB and SNDR with a mismatch of 0.3%. **a** ENOB, **b** SNDR

Figure 7 shows the histogram of ENOB and SNDR when the mismatch is 0.3%. It shows that the simulation results of 500 runs that the average of ENOB is 9.74 bit and the average of SNDR is 60.39 dB. Generally, the actual mismatch is less than 0.3%, so the effect of mismatch between V_{CM} and V_{REF} is acceptable for the design of 10-bit SAR ADCs.

6 Conclusion

A low-energy switching scheme based on the asymmetric binary search algorithm is proposed. The one-half unit capacitor is used in the structure to achieve a further reduction in power consumption. Considering the mismatch problem of small capacitors, the proposed switching structure uses two unit capacitors in series to achieve a one-half unit capacitor. Compared with the conventional switching scheme, the proposed switching scheme achieves 99.43% energy reduction and 87.2% area optimization. Using three reference voltages, V_{REF}, V_{CM}, and GND, the proposed scheme has significant advantages in considering power and area and has application prospect in the design of low-power SAR ADCs.

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