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An Extremely Low-Voltage and High-Compliance Current Mirror

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Abstract

In this paper, a novel ultrahigh-compliance, low-voltage and low-power current mirror is proposed. The proposed structure utilizes the cooperative positive–negative local feedback to achieve ever-interesting high output voltage compliance. The structure takes the advantage of the current compensation scheme to boost the positive feedback at high current values, in which, otherwise the positive feedback and consequently the output voltage compliance tend to be degraded. The performance of the proposed architecture is validated by HSPICE simulation in TSMC 180 nm CMOS, BSIM 3 and Level 49 technology. The simulation results of the proposed structure show input/output minimum voltages of 0.059 V/0.038 V, output resistance of 121.36 GΩ and bandwidth of 211 MHz, while it consumes only 42.5 μW considering 1 V supply voltage. The current transfer error is interestingly less than 0.4% throughout its current dynamic range.

Keywords Positive and negative feedback · High precision · High compliance · Low voltage · Low power

1 Introduction

Current mirror (CM) is a versatile and fundamental analog block with widespread usage either as a DC biasing block or an AC signal path in most current mode and voltage mode circuits and systems, such as current conveyors, operational transconductance amplifiers, operational mirrored amplifiers, current feedback operational

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amplifiers, operational amplifiers, analog filters and analog-to-digital and digital-to-analog converters [3, 4, 6, 8–11, 14, 15]. The CM specification has an extremely impressive effect on the overall performance of the system in which it is utilized. Current dynamic range, current transfer precision, minimum input/output voltage, input/output resistance and bandwidth are of the most important parameters of a current mirror. Although each application has its specific requirements [1], it has always been desired to have a block which may effectively reach its ideal operation. Several studies have been recently reported trying to achieve this goal using novel structures and techniques [2, 7, 8, 10, 11, 13].

For example, a low-voltage structure is introduced in [17] which utilizes a complex and expensive multimode technique based simultaneously on bulk-driven, quasi-floating gate and self-biased schemes. Although it offers some improvements in terms of voltage and power, however, its current transfer error is high. A high-precision CM is proposed at [12] utilizing positive shunt feedback, but it suffers from large voltage requirement, low dynamic range and high input impedance.

A very high-compliance structure is proposed in [2] which exploits the benefits of the mutually cooperated negative and positive feedbacks.

In this architecture, for high enough output voltages, the output impedance is kept sufficiently high due to the strong negative feedback, the condition in which the positive feedback is extremely weakened [2]. As the output voltage drops below a specific value, the negative feedback misses the prior functionality, allowing the positive feedback to start functioning. This helps the structure to effectively preserve its high output impedance value. Unfortunately, as the input current increases, the structure deviates from its optimal operating condition and hence the output compliance is decreased substantially.

Some attempts are made to improve the efficiency of the structure trying to increase the strength of the negative feedback [5]. Although some improvements can be observed, the achievements are somewhat trivial, as the structure employs the more expensive bulk-driven process and also has deteriorated current transfer accuracy. Moreover, strengthening the negative feedback reduces the effect of the positive feedback which is not a desirable condition from the low-voltage operation point of view.

An ultrahigh-compliance, high-precision structure is presented in this paper. The proposed structure utilizes a current compensated scheme to boost the positive feedback. This helps the structure to more effectively maintain its optimal operation even at higher input current values. The performance of the structure is evaluated through formulation and validated by simulation results. The simulations are carried out with HSPICE using TSMC 180 nm CMOS standard technology.

The paper is organized as follows: In Sect. 2, the proposed current mirror structure is explained, and its principle of operation along with the small-signal characteristics is analyzed. The simulation results are presented in Sect. 3. Finally, Sect. 4 concludes the paper.

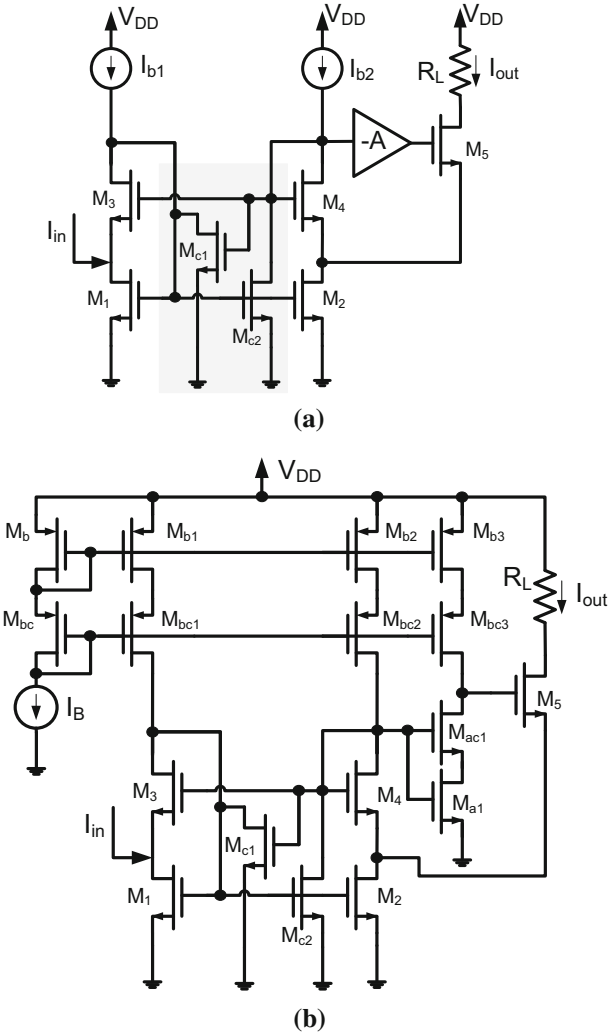


Fig. 1 Proposed current mirror: **a** conceptual scheme and **b** transistor-level implementation

2 Proposed Current Mirror Structure

2.1 Principle of Operation

The conceptual scheme of the proposed current mirror is shown in Fig. 1a, and its transistor-level implementation is depicted in Fig. 1b. The proposed work exploits the core structure (the unshaded part of Fig. 1a) of the circuit presented in [2] and is modified by inserting the current compensated transistors of M_{c1}-M_{c2} (the shaded part of Fig. 1a). The overall structure consists of the biasing currents, I_{b1} and I_{b2}, the amplifier '-A,' the mirror transistors M_1-M_2, the cascode transistors M_3-M_4 and the

output current buffer transistor M_5. The input current of I_{in} is injected to the drain of M_1, and the output current of I_{out} is delivered through the M_5 to the load impedance, R_L. Figure 1b shows the ultimate transistor-level realization of the proposed architecture, which includes the implementation of the amplifier and biasing currents, as well.

The conventional structure (the unshaded part of Fig. 1a) includes two local feedbacks: The positive feedback made up of transistors M_1-M_4 and the negative one built from amplifier '-A' and transistors M_2 and M_4-M_5. Typically, the negative feedback is used to boost the performance of the current mirror structures by stabilizing the output current against the output voltage variations. This is normally interpreted as the increased impedance at the output node of the structure. Unfortunately, the negative feedback fails to operate as the output voltage approaches to ground. This is mainly due to fact that the transistors incorporated in the feedback loop leave their saturation region, which destroy the feedback gain.

This restricts the application of the negative feedback in very low-voltage circuits, which opposes the modern technology trend.

An alternative approach is to utilize the positive feedback which is more compatible with the low-voltage applications. Although the positive feedback performs well at low voltages, it is prone to instability at relatively high voltages. Therefore, to maintain the stability of the circuit, the voltage variation in the sensitive node of the positive feedback needs to be limited.

In the conventional current mirror reported at [2], the negative and positive feedbacks are designed to cooperate well, resulting a robust and high performance structure. In this structure, at high output voltages, the negative feedback fixes the drain voltage of M_2 (the positive feedback sensitive node), against the output voltage variations, resulting an acceptable current transfer accuracy. This also practically inactivates the positive feedback and eliminates its potential instability. As the voltage drops, the negative feedback stops operating and leaves the sensitive node to follow the output voltage variations. This activates the positive feedback which helps the output current to preserve its value. Although this structure functions well for small input current ranges, however, as the input current increases, its operation is degraded. This is mainly due to the fact that at higher operating currents, the positive feedback gain becomes insufficient and fails to maintain the desired output current.

In the modified structure, the current compensated transistors M_{c1}-M_{c2} empower the positive feedback at high values of the input current. Fortunately, the influence of the current compensated scheme is proportional with the input current, which extends the low-voltage operation of the structure.

Let us explain the idea in more detail as follows:

Considering that the positive feedback can potentially make any system unstable, it must be utilized in an elaborately and strictly controlled manner. To do so, in [2], the concept is established by proposing a circuit structure with an appropriate and constant positive feedback gain. This idea performs well for a specific current range (lower boundary); unfortunately, the positive feedback strength becomes inadequate as the current signal grows more and more. Even though this issue could be solved by considering an initially powerful positive feedback, it would make the system instable at lower current ranges. In brief, one should choose an appropriate positive feedback strength proportional to the operating current value, i.e., powerful positive feedback

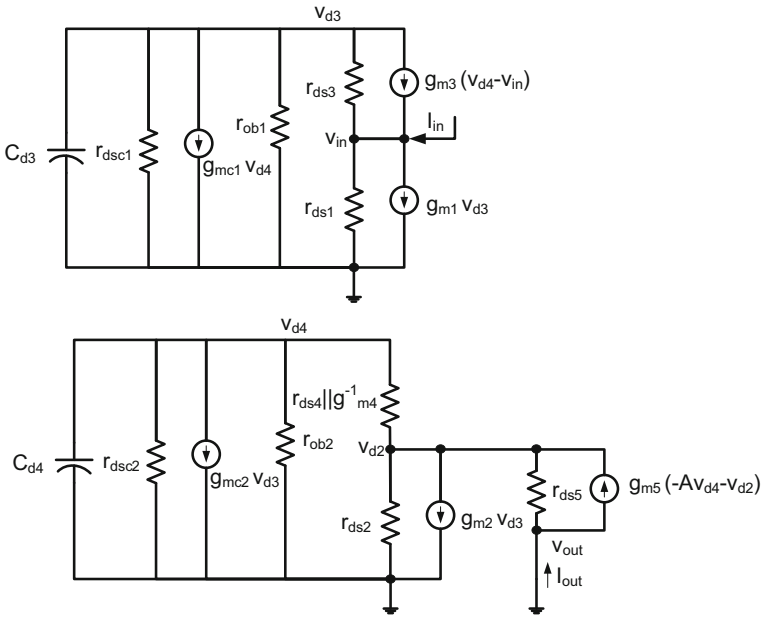


Fig. 2 Small-signal model of the proposed circuit

for large signals and weak positive feedback for small signals. The better solution is to adjust the positive feedback gain adaptively with the current strength, as is done in this work. Referring to Fig. 1a, which depicts the idea conceptually, two transistors M_{c1}-M_{c2} are embedded into the core structure of the traditional circuit [2].

These transistors are designed in a way that have a negligible influence at lower current ranges. Therefore, the positive feedback is mainly handled by the traditional structure at these low current ranges. As the input current increases, the original positive feedback becomes insufficient, and the M_{c1}-M_{c2} transistors start to play their roles. This phenomenon originates from the increased difference between the mirror transistors' (M_1-M_2) drain–source voltages caused by the large input current. This voltage difference is directly applied to the gates of the current compensated transistors (M_{c1}-M_{c2}) which starts to boost the positive feedback (proportionally with the input current value). To be more specific, consider the case that the output voltage is decreased to the very low values and caused the aforementioned voltage differences. This in turn decreases the M_{c1} transistor gate voltage and hence boosts the $V_{gs1,2}$. This strengthens the positive feedback in two ways: first by increasing the current of M_2 and second with reducing the current flown through M_4, both of which lead to increased output (M_5) current.

2.2 Circuit Frequency-Domain Small-Signal Analysis

The small-signal model of the proposed circuit is shown in Fig. 2. In this figure, only two capacitors, namely C_{d3} and C_{d4}, are considered at high-impedance nodes. This is

to make the analytical calculations feasible, but definitely the exact behavior of the circuit will not be achieved. Considering this figure and performing some simplifications, the following equations can be obtained.

$$-g_{m_4}V_{d_2}+g_{mc_2}V_{d_3}+\left(g_{m_4}+\frac{1}{\frac{1}{C_{d4}s}||R_2}\right)V_{d_4}=0 \tag{1}$$

where $R_2 = r_{dsc_2}||r_{ob_2}$, $C_{d4} = C_{gsc1}+C_{gsa1}+C_{dsc2}+C_{gdbc2}+(1+A)\times C_{gdac1}$, $\frac{1}{C_{d4}s}||R_2=\frac{R_2}{1+R_2C_{d4}s}$

$$I_{\text{out}}=\left(g_{m_4}+\frac{1}{r_{ds_2}}\right)V_{d_2}+g_{m_2}V_{d_3}-g_{m_4}V_{d_4} \tag{2}$$

$$I_{\text{out}}=\frac{1}{r_{ds_5}}V_{\text{out}}-g_{m_5}V_{d_2}-Ag_{m_5}V_{d_4} \tag{3}$$

$$-g_{m_3}V_{\text{in}}+\frac{V_{d_3}}{\frac{1}{C_{d3}s}||R_1}+(g_{mc_1}+g_{m_3})V_{d_4}=0 \tag{4}$$

where $R_1 = r_{dsc_1}||r_{ob_1}||r_{ds_3}$, $C_{d3}=C_{gs1}+C_{gs2}+C_{dsc1}+C_{gsc2}+C_{gdbc1}$, $\frac{1}{C_{d3}s}||R_1=\frac{R_1}{1+R_1C_{d3}s}$

$$I_{\text{in}}=\frac{1}{r_{ds_1}}V_{\text{in}}+g_{m_1}V_{d_3}+g_{mc_1}V_{d_4} \tag{5}$$

where $A=\frac{g_{m_{a1}}g_{m_{ac1}}r_{ds_{a1}}r_{ds_{ac1}}r_{ob_3}}{r_{ob_3}+g_{m_{ac1}}r_{ds_{ac1}}r_{ds_{a1}}}$ and $r_{ob_i}\simeq r_{ds_{b,i}}r_{ds_{cb,i}}g_{m_{cb,i}}$, $\quad i=1,\ldots,3.$

2.2.1 Frequency-Domain Input Impedance Analysis

Considering $V_{\text{out}}=0$ in Eq. (3) and substituting it into (2) give:

$$V_{d_2}=-\frac{g_{m_2}}{g_{m_4}+g_{m_5}}V_{d_3}+\frac{g_{m_4}-Ag_{m_5}}{g_{m_4}+g_{m_5}}V_{d_4} \tag{6}$$

Substituting V_{d_2} from (6) into (1) gives:

$$V_{d_4}=\frac{g_{m_2}g_{m_4}+g_{mc_2}\left(g_{m_4}+g_{m_5}\right)}{\left(\frac{g_{m_4}+g_{m_5}}{\frac{1}{C_{d4}s}||R_2}-g_{m_4}g_{m_5}(A+1)\right)}V_{d_3} \tag{7}$$

Performing some simplifications on (4), (5) and (7) gives:

$$R_{\text{in}}=r_{ds_1}||R_{\text{eq1}} \tag{8}$$

where

$$
\begin{aligned}
R_{\text{eq1}} &= \frac{N_1}{D_1} = \frac{K_{N11} + K_{N12}s + K_{N13}s^2}{K_{D11} + K_{D12}s} \\
K_{N11} &= \big(g_{m_2}g_{m_4} + g_{mc_2}\big(g_{m_4} + g_{m_5}\big)\big)\big(g_{mc_1} + g_{m_3}\big) \\
&\quad + \frac{1}{R_1}\left(\frac{1}{R_2}\big(g_{m_4} + g_{m_5}\big) - g_{m_4}g_{m_5}(A+1)\right) \\
K_{N12} &= \left(\frac{1}{R_2}\big(g_{m_4} + g_{m_5}\big) - g_{m_4}g_{m_5}(A+1)\right)C_{d3} + \frac{1}{R_1}\big(g_{m_4} + g_{m_5}\big)C_{d4} \\
K_{N13} &= \big(g_{m_4} + g_{m_5}\big)C_{d3}C_{d4} \\
K_{D11} &= g_{mc_1}g_{m_3}\big(g_{m_2}g_{m_4} + g_{mc_2}\big(g_{m_4} + g_{m_5}\big)\big) \\
&\quad + g_{m_1}g_{m_3}\left(\frac{1}{R_2}\big(g_{m_4} + g_{m_5}\big) - g_{m_4}g_{m_5}(A+1)\right) \\
K_{D12} &= g_{m_1}g_{m_3}\big(g_{m_4} + g_{m_5}\big)C_{d4}
\end{aligned}
\tag{9}
$$

Considering the DC value of the input impedance given at (9) and doing some simplifications, we have:

$$
R_{\text{eq1}}\big|_{s=0} = \frac{K_{N11}}{K_{D11}} = \frac{\big(g_{m_2}g_{m_4} + g_{mc_2}\big(g_{m_4} + g_{m_5}\big)\big)\big(g_{mc_1} + g_{m_3}\big) - g_{m_4}g_{m_5}\frac{1}{R_1}(A+1)}{g_{mc_1}g_{m_3}\big(g_{m_2}g_{m_4} + g_{mc_2}\big(g_{m_4} + g_{m_5}\big)\big) - g_{m_1}g_{m_3}g_{m_4}g_{m_5}(A+1)} \tag{10}
$$

Hence, the input impedance for dc frequency, i.e., $s = 0$, is given as:

$$
\begin{aligned}
R_{\text{in}} &= \frac{V_{\text{in}}}{I_{\text{in}}} = r_{ds_1} || R_{\text{eq1}} = r_{ds_1} || \\
&\quad \frac{g_{m_4}g_{m_5}\frac{1}{R_1}(1+A) - (g_{mc_1} + g_{m_3})\big[g_{m_2}g_{m_4} + g_{mc_2}(g_{m_4} + g_{m_5})\big]}{g_{m_3}\big[g_{m_1}g_{m_4}g_{m_5}(1+A) - g_{mc_1}\big[g_{m_2}g_{m_4} + g_{mc_2}(g_{m_4} + g_{m_5})\big]\big]}
\end{aligned}
\tag{11}
$$

Supposing $g_{m_1}g_{m_4}g_{m_5}(1+A) >> g_{mc_1}\big[g_{m_2}g_{m_4} + g_{mc_2}(g_{m_4} + g_{m_5})\big]$ and $r_{ds_1} >> R_{\text{eq1}}$, Eq. (11) can be simplified as:

$$
R_{\text{in}} = R_{\text{eq1}} = \frac{g_{m_4}g_{m_5}\frac{1}{R_1}(1+A) - (g_{mc_1} + g_{m_3})\big[g_{m_2}g_{m_4} + g_{mc_2}(g_{m_4} + g_{m_5})\big]}{g_{m_1}g_{m_3}g_{m_4}g_{m_5}(1+A)} \tag{12}
$$

Considering the actual values for the parameters in (12) gives rather small values for the input impedance. The input impedance value can even be adjusted to zero, by providing the following condition:

$$
g_{m_4}g_{m_5}\frac{1}{R_1}(1+A) = (g_{m_2}g_{m_4} + g_{mc_2}(g_{m_4} + g_{m_5}))(g_{m_3} + g_{mc_1}) \tag{13}
$$

This can simply be achieved by adjusting transistor aspect ratios.

If $g_{mc_1} = g_{mc_2} = 0$, the input impedance is equal with the one achieved at [2]. Comparing with [2] gives:

$$\frac{R_{\text{in}}}{R_{\text{in},[2]}} \simeq 1 - \frac{g_{mc_2} g_{m_3}(g_{m_4} + g_{m_5}) + g_{mc_1}\left[g_{m_2} g_{m_4} + g_{mc_2}(g_{m_4} + g_{m_5})\right]}{g_{m_4} g_{m_5} \frac{1}{R_1}(1 + A) - g_{m_2} g_{m_3} g_{m_4}} \tag{14}$$

Equation (14) shows that the input impedance value can be further decreased in the proposed circuit compared to the one derived at [2], thanks to the contribution of the g_{mc1} and g_{mc2}.

2.2.2 Frequency-Domain Output Impedance Analysis

In this subsection, the small-signal output impedance is analyzed.

To do so, replacing V_{in} from (5) into (4) with the assumption that I_{in} is zero and considering some simplifications give:

$$V_{d_3} = -\frac{\left(g_{mc_1} + g_{m_3} + g_{m_3} r_{ds_1} g_{mc_1}\right)}{\left(g_{m_3} r_{ds_1} g_{m_1} + \frac{1}{\frac{1}{C_{d3}s} || R_1}\right)} V_{d_4} \tag{15}$$

Substituting (15) into (1) and (2) gives:

$$V_{d_2} = \frac{1}{g_{m_4}} \left(\left(g_{m_4} + \frac{1}{\frac{1}{C_{d4}s} || R_2} \right) - \frac{g_{mc_2}\left(g_{mc_1} + g_{m_3} + g_{m_3} r_{ds_1} g_{mc_1}\right)}{\left(g_{m_3} r_{ds_1} g_{m_1} + \frac{1}{\frac{1}{C_{d3}s} || R_1}\right)} \right) V_{d_4} \tag{16}$$

$$I_{\text{out}} = \left(g_{m_4} + \frac{1}{r_{ds_2}} \right) V_{d_2} - \left(g_{m_4} + g_{m_2} \frac{\left(g_{mc_1} + g_{m_3} + g_{m_3} r_{ds_1} g_{mc_1}\right)}{\left(g_{m_3} r_{ds_1} g_{m_1} + \frac{1}{\frac{1}{C_{d3}s} || R_1}\right)} \right) V_{d_4} \tag{17}$$

Substituting (16) and (17) into (3) and assuming that $g_{m_4} r_{ds_5}(1 + A)\left[g_{m_1} g_{m_3} r_{ds_1} + (r_{dsc_1} || r_{ob_1} || r_{ds_3})^{-1}\right] >> g_{mc_2}(g_{mc_1} + g_{m_3} + g_{m_3} g_{mc_1} r_{ds_1})$ give:

$$\begin{aligned} R_{\text{out}} &= \frac{V_{\text{out}}}{I_{\text{out}}} = r_{ds_5}\left[1 + \frac{N_2}{D_2}\right] \\ N_2 &= K_{N21} + K_{N22} s + K_{N23} s^2 \\ D_2 &= K_{D21} + K_{D22} s + K_{D23} s^2 \end{aligned} \tag{18}$$

where

$$\begin{aligned} K_{N21} = &\left\{ A g_{m_5} + \frac{g_{m_5}}{g_{m_4}}\left[g_{m_4} + \frac{1}{R_2} \right] \right\} \left(g_{m_3} r_{ds_1} g_{m_1} + \frac{1}{R_1} \right) \\ &- g_{mc_2} \frac{g_{m_5}}{g_{m_4}} \left(g_{mc_1} + g_{m_3} + g_{m_3} r_{ds_1} g_{mc_1} \right) \end{aligned}$$

$$
\begin{aligned}
K_{N22} &= Ag_{m_5}C_{d3} + \frac{g_{m_5}}{g_{m_4}}\left(g_{m_4} + \frac{1}{R_2}\right)C_{d3} + \frac{g_{m_5}}{g_{m_4}}\left(g_{m_3}r_{ds_1}g_{m_1} + \frac{1}{R_1}\right)C_{d4} \\
K_{N23} &= \frac{g_{m_5}}{g_{m_4}}C_{d3}C_{d4} \\
K_{D21} &= \left[\frac{1}{r_{ds_2}} + \frac{1}{R_2}\left(1 + \frac{1}{g_{m_4}r_{ds_2}}\right)\right]\left(g_{m_3}r_{ds_1}g_{m_1} + \frac{1}{R_1}\right) \\
&\quad - \left(g_{mc_1} + g_{m_3} + g_{m_3}r_{ds_1}g_{mc_1}\right)\left((1 + \frac{1}{g_{m_4}r_{ds_2}})g_{mc_2} + g_{m_2}\right) \\
K_{D22} &= \left[\frac{1}{r_{ds_2}} + \frac{1}{R_2}\left(1 + \frac{1}{g_{m_4}r_{ds_2}}\right)\right]C_{d3} + \left(g_{m_3}r_{ds_1}g_{m_1} + \frac{1}{R_1}\right)(1 + \frac{1}{g_{m_4}r_{ds_2}})C_{d4} \\
K_{D23} &= \left(1 + \frac{1}{g_{m_4}r_{ds_2}}\right)C_{d3}C_{d4}
\end{aligned}
\tag{19}
$$

Considering the DC value of the output impedance given at (18) and (19) and with some simplifications, we have:

$$
\begin{aligned}
R_{\text{out}}|_{s=0} &= \left.\frac{V_{\text{out}}}{I_{\text{out}}}\right|_{s=0} = r_{ds_5}\left[\frac{K_{D21} + K_{N21}}{K_{D21}}\right] \\
&= \frac{g_{m_1}g_{m_3}g_{m_4}g_{m_5}r_{ds_1}r_{ds_2}(1+A) + g_{m_1}g_{m_3}g_{m_4}r_{ds_1} - \left(g_{mc_2}g_{m_5}r_{ds_2} + g_{m_4}r_{ds_2}\left[g_{mc_2} + g_{m_2}\right]\right)\left(g_{m_3} + g_{m_3}r_{ds_1}g_{mc_1}\right)}{g_{m_1}g_{m_3}g_{m_4}r_{ds_1} - \left(g_{mc_2} + g_{m_4}r_{ds_2}\left[g_{m_2} + g_{mc_2}\right]\right)\left(g_{mc_1} + g_{m_3} + g_{m_3}r_{ds_1}g_{mc_1}\right)}
\end{aligned}
\tag{20}
$$

Since for extremely large output impedance, the denominator must approach zero value, hence, the component $g_{m_1}g_{m_3}g_{m_4}r_{ds_1} - \left(g_{mc_2}g_{m_5}r_{ds_2} + g_{m_4}r_{ds_2}\left[g_{mc_2} + g_{m_2}\right]\right)\left(g_{m_3} + g_{m_3}r_{ds_1}g_{mc_1}\right)$ can be eliminated from nominator.

$$
R_{\text{out}}|_{s=0} = \frac{g_{m_1}g_{m_3}g_{m_4}g_{m_5}r_{ds_1}r_{ds_2}r_{ds_5}(1+A)}{g_{m_1}g_{m_3}g_{m_4}r_{ds_1} - (g_{mc_2} + g_{m_4}r_{ds_2}(g_{mc_2} + g_{m_2}))(g_{mc_1} + g_{m_3} + g_{m_3}g_{mc_1}r_{ds_1})}
\tag{21}
$$

If $g_{mc_1} = g_{mc_2} = 0$, the output impedance is equal with the one achieved at [2]. Comparing with [2] gives:

$$
\frac{R_{\text{out}}}{R_{\text{out},[2]}} = \frac{1}{1 - \frac{g_{mc_2}(1+g_{m_4}r_{ds_2})(g_{mc_1}(1+g_{m_3}r_{ds_1})+g_{m_3})+g_{mc_1}g_{m_2}g_{m_4}r_{ds_2}(1+g_{m_3}r_{ds_1})}{g_{m_1}g_{m_3}g_{m_4}r_{ds_1} - g_{m_2}g_{m_3}g_{m_4}r_{ds_2}}}
\tag{22}
$$

Equation (22) shows that the output impedance value can be further increased in the proposed circuit compared to the one derived at [2], thanks to the contribution of the g_{mc1} and g_{mc2}.

2.2.3 Frequency-Domain Current Transfer Analysis

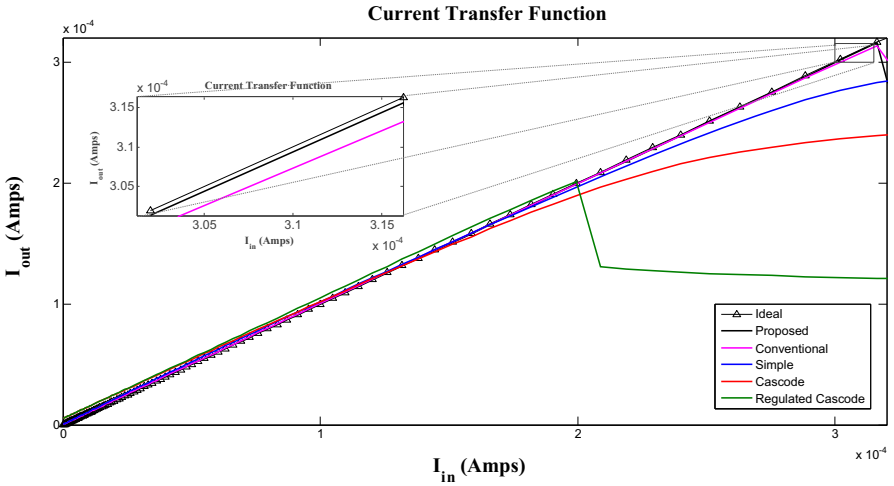
In this subsection, the small-signal current transfer function of the proposed circuit is obtained.

Considering $V_{\text{out}} = 0$ and replacing V_{d_2} from (2) in (3) and (1) give:

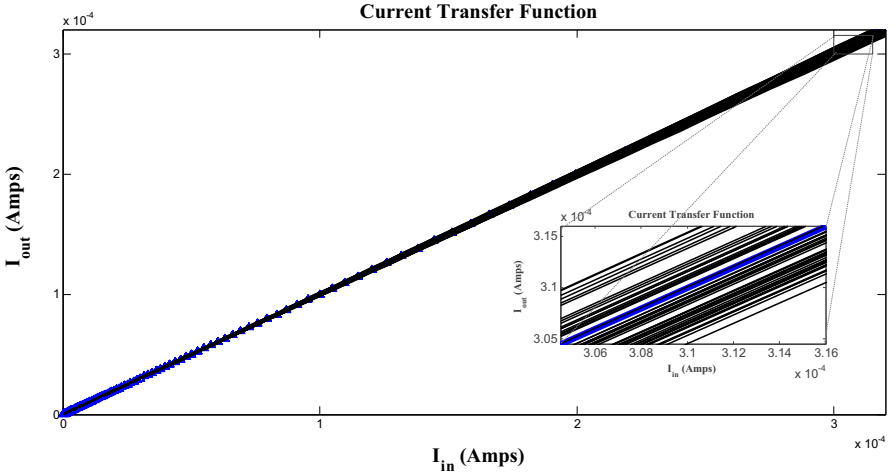
$$V_{d_4} = \frac{g_{m_2} g_{m_5} V_{d_3} - I_{out}\left(g_{m_4} + g_{m_5}\right)}{g_{m_4} g_{m_5}(1 + A)} \tag{23}$$

Table 1 Transistors aspect ratios

M_1-M_2	M_3-M_4	M_{c1}-M_{c2}	M_5	M_{a1}	M_{ac1}
45/0.54	29.7/0.18	0.36/4.86	36/0.18	36/0.18	4.5/0.18

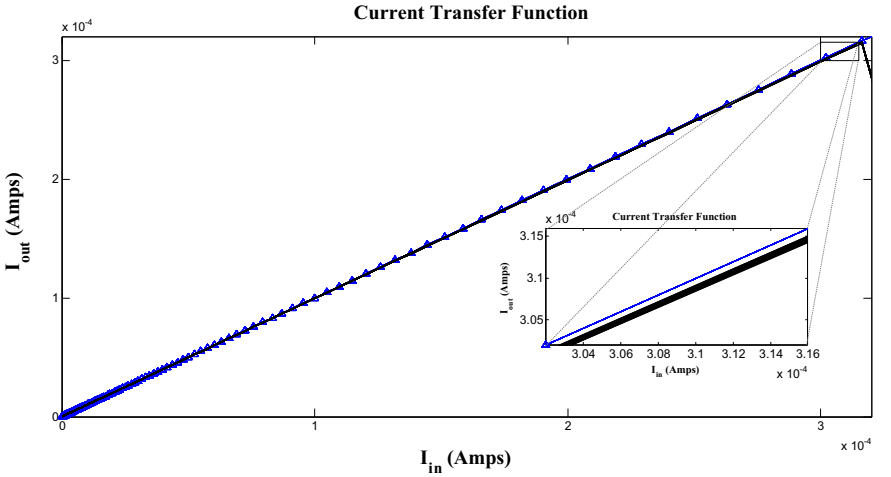


(a)

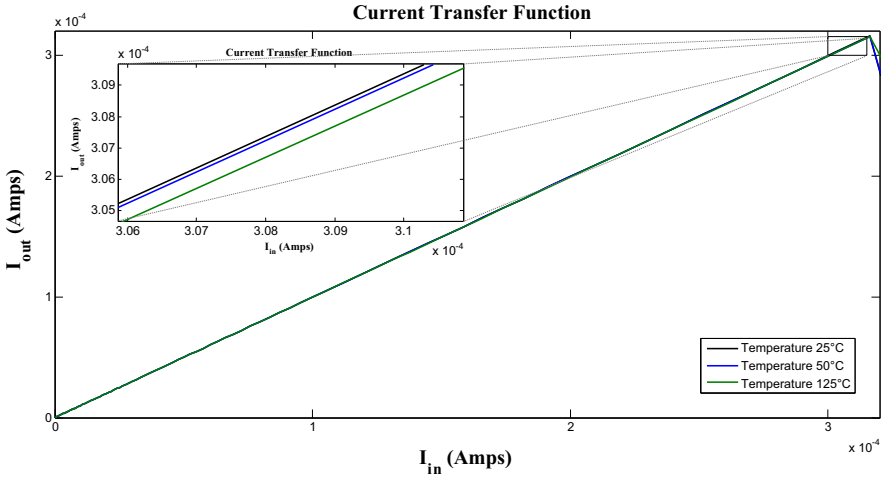


(b)

Fig. 3 I_{out} versus I_{in} **a** typical case in comparison with other structures, **b** Monte Carlo analysis applying 5% process (W/L and V_{TH}) variations, **c** 10% variation in biasing currents and **d** temperatures of 25 °C, 50 °C and 125 °C



(c)



(d)

Fig. 3 continued

$$I_{\text{out}} = \left(1 + \frac{1}{g_{m_4} r_{ds_2}}\right) C_{d4} s V_{d_4} + \left[g_{m_2} + g_{mc_2}\right] V_{d_3} \tag{24}$$

Substituting (23) and (24) into (4) and (5), respectively, and doing some simplification give:

$$V_{\text{in}} = \frac{I_{\text{out}}}{g_{m_3}} \left[\frac{\left(g_{m_4} g_{m_5}(1+A) + \left(g_{m_4} + g_{m_5}\right) C_{d4} s\right)\left(\frac{1}{R_1} + \frac{g_{m_2}\left(g_{mc_1} + g_{m_3}\right)}{g_{m_4}(1+A)} + C_{d3} s\right)}{\left(\left(g_{m_2} + g_{mc_2}\right) g_{m_4} g_{m_5}(1+A) + g_{m_2} g_{m_5} C_{d4} s\right)} - \frac{\left(g_{m_4} + g_{m_5}\right)\left(g_{mc_1} + g_{m_3}\right)}{g_{m_4} g_{m_5}(1+A)} \right] \tag{25}$$

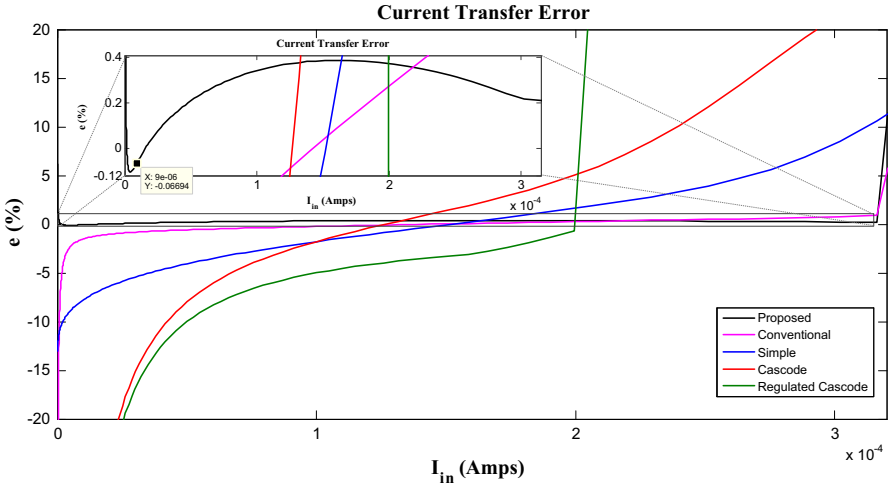


Fig. 4 Current transfer error for input current swept from 0 to 320 μA

$$I_{\text{in}} = \frac{1}{r_{ds_1}} V_{\text{in}} + \left\{ \frac{\left[g_{m_1} + \frac{g_{mc_1} g_{m_2}}{g_{m_4}(1+A)} \right] \left[1 + \left(1 + \frac{1}{g_{m_4} r_{ds_2}} \right) \frac{(g_{m_4}+g_{m_5})}{g_{m_4} g_{m_5}(1+A)} C_{d4} s \right]}{\left[(g_{m_2} + g_{mc_2}) + \left(1 + \frac{1}{g_{m_4} r_{ds_2}} \right) \frac{g_{m_2}}{g_{m_4}(1+A)} C_{d4} s \right]} - \frac{g_{mc_1}(g_{m_4} + g_{m_5})}{g_{m_4} g_{m_5}(1+A)} \right\} I_{\text{out}} \tag{26}$$

Simplifying (25) and (26) gives the current transfer function as:

Simplifing:

$$\begin{aligned} \lambda &= \frac{I_{\text{out}}}{I_{\text{in}}} = \frac{N_3}{D_3} \\ N_3 &= K_{N31} + K_{N32} s \\ D_3 &= K_{D31} + K_{D32} s + K_{D33} s^2 \end{aligned} \tag{27}$$

where

$$\begin{aligned} K_{N31} &= g_{m_3} g_{m_4} g_{m_5} r_{ds_1} (1+A)\left(g_{m_2} + g_{mc_2}\right) \\ K_{N32} &= g_{m_2} g_{m_3} g_{m_5} r_{ds_1} C_{d4} \\ K_{D31} &= \frac{g_{m_4} g_{m_5}(1+A)\left(1 + g_{m_1} g_{m_3} r_{ds_1} R_1\right)}{R_1} \\ &\quad - \left(g_{m_2} g_{m_4} + g_{mc_2}\left(g_{m_4} + g_{m_5}\right)\right)\left(g_{mc_1}\left(1 + g_{m_3} r_{ds_1}\right) + g_{m_3}\right) \\ K_{D32} &= g_{m_4} g_{m_5}(1+A) C_{d3} + \left(\frac{1}{R_1} + g_{m_1} g_{m_3} r_{ds_1} \right)\left(g_{m_4} + g_{m_5}\right) C_{d4} \\ K_{D33} &= \left(g_{m_4} + g_{m_5}\right) C_{d3} C_{d4} \end{aligned} \tag{28}$$

Considering the DC gain of the current mirror gives:

$$\lambda|_{s=0} = \frac{K_{N31}}{K_{D31}} = \frac{g_{m_3} g_{m_4} g_{m_5} r_{ds_1} (1+A)\left(g_{m_2} + g_{mc_2}\right)}{\frac{g_{m_4} g_{m_5} (1+A)\left(1+g_{m_1} g_{m_3} r_{ds_1} R_1\right)}{R_1} - \left(g_{m_2} g_{m_4} + g_{mc_2}\left(g_{m_4} + g_{m_5}\right)\right)\left(g_{mc_1}\left(1 + g_{m_3} r_{ds_1}\right) + g_{m_3}\right)} \tag{29}$$

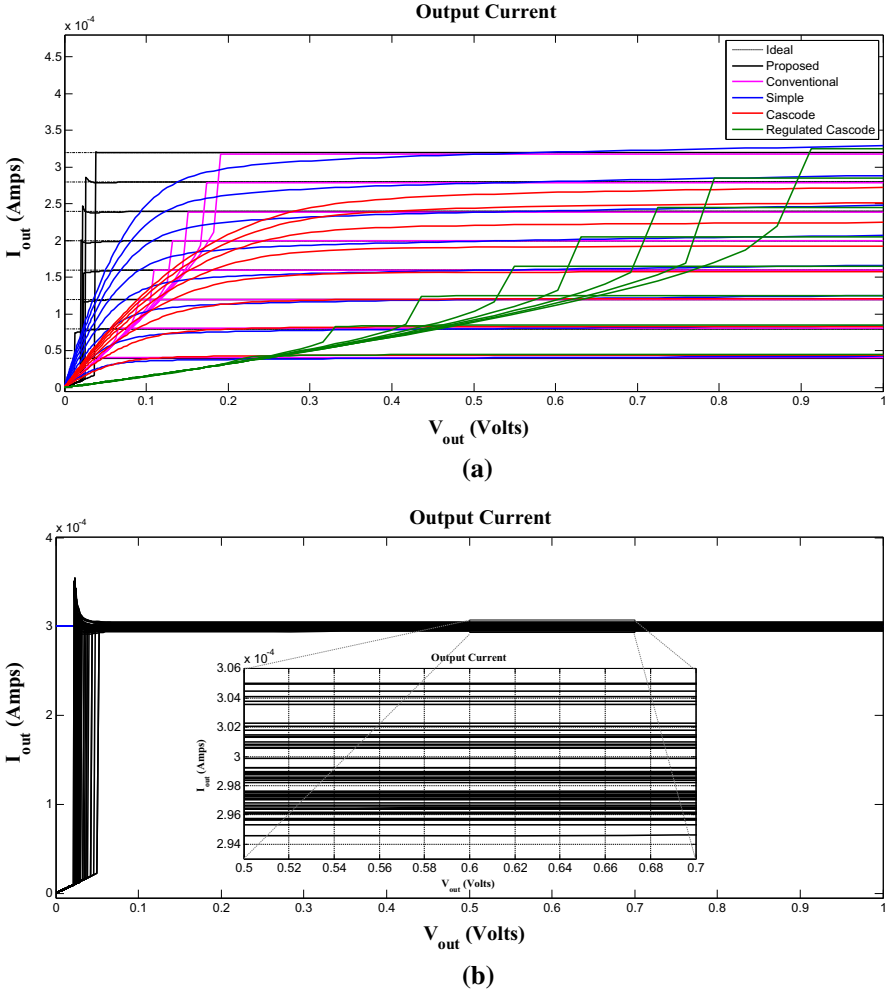
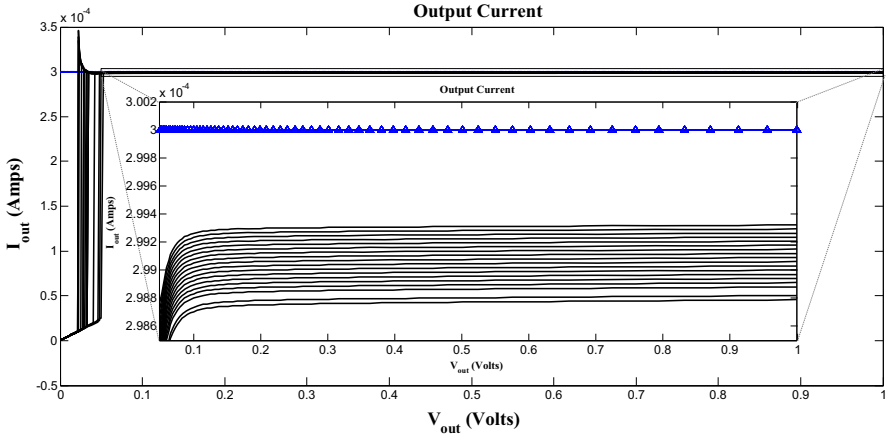


Fig. 5 I_{out} versus V_{out} **a** typical case in comparison with other structures, **b** Monte Carlo analysis applying 5% process (W/L and V_{TH}) variations, **c** 10% variation in biasing currents and **d** temperatures of 25 °C, 50 °C and 125 °C



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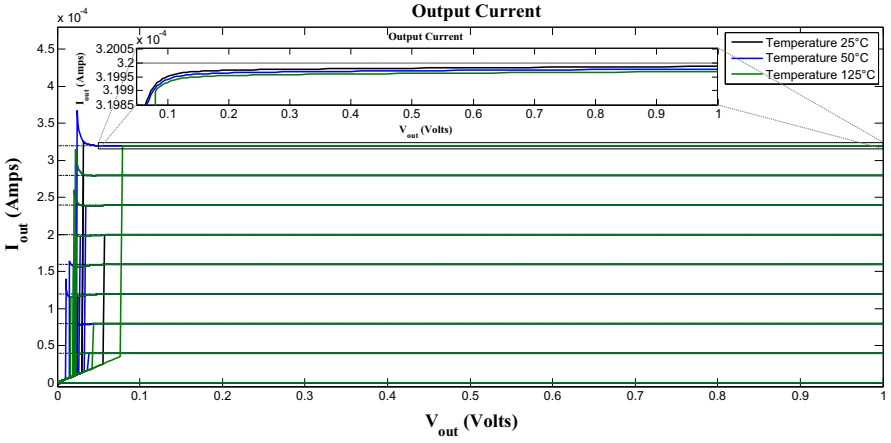


(d)

Fig. 5 continued

3 Simulation Results

All simulations are accomplished by HSPICE using TSMC 180 nm BSIM3, Level49 CMOS technology in room temperature. To examine the well functionality of the proposed structure under real circumstances, the Monte Carlo simulations considering the temperature and biasing currents' variations are performed on all of the design parameters. The results show well robustness of the design on the various PVT variations and mismatch condition. The performance of the proposed structure is compared with some other similar structures including simple, regulated cascode and low-voltage cascode, and the conventional structure presented at [2]. Except for the proposed structure whose transistor aspect ratios are listed in Table 1, the specification of other topologies is adopt from [2].

Although the circuit can operate at lower supply voltages, it is adjusted to function utilizing a single 1 V power supply to be compared with its conventional version. Bias currents provided by M_{b1}, M_{b2} and M_{b3} are $I_{b1} = 5\,\mu A$, $I_{b2} = 5\,\mu A$ and $I_{b3} = 2.5\,\mu A$, respectively, and the load resistance is selected to be 3 KΩ.

To analyze the operating performance of the proposed structure, some of the most important parameters including current transfer function, voltage compliances, frequency bandwidth and transient response are investigated through HSPICE simulations.

To investigate the current dynamic range and the current transfer accuracy, the output versus the input current of the proposed structure is compared with other current

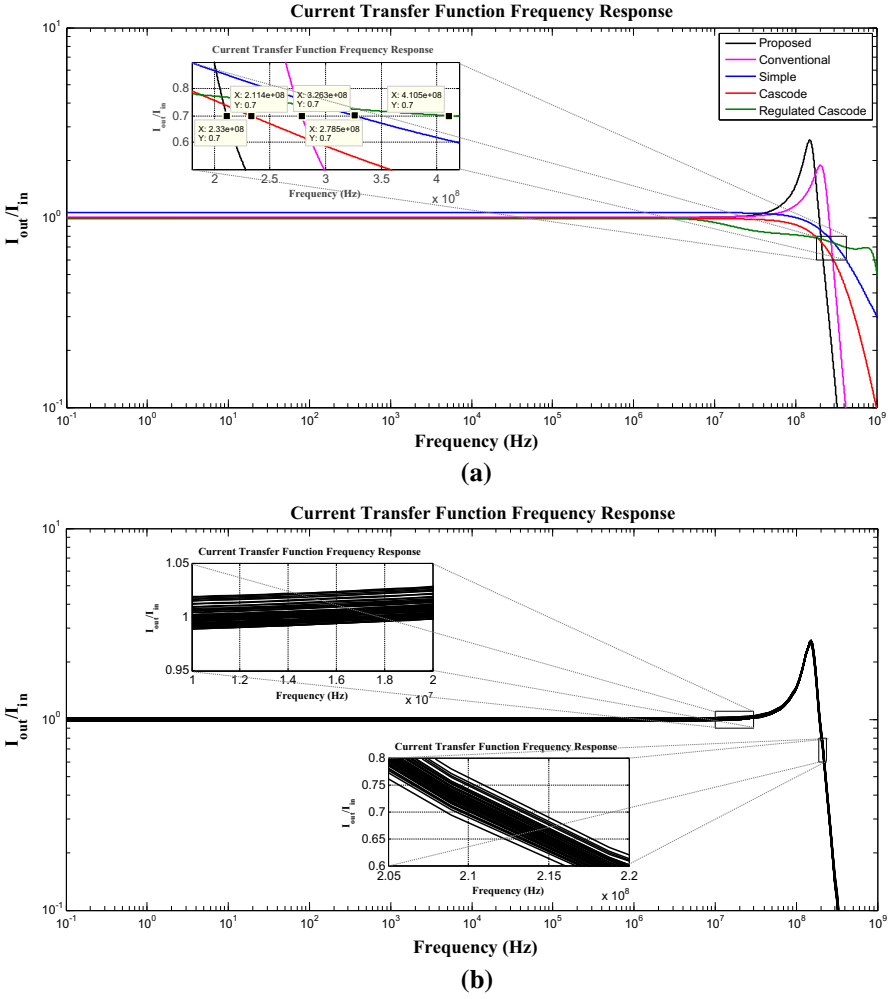
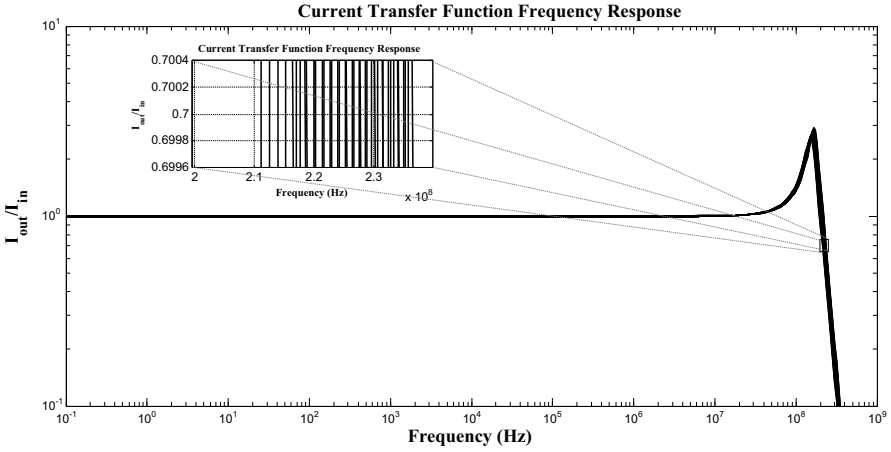
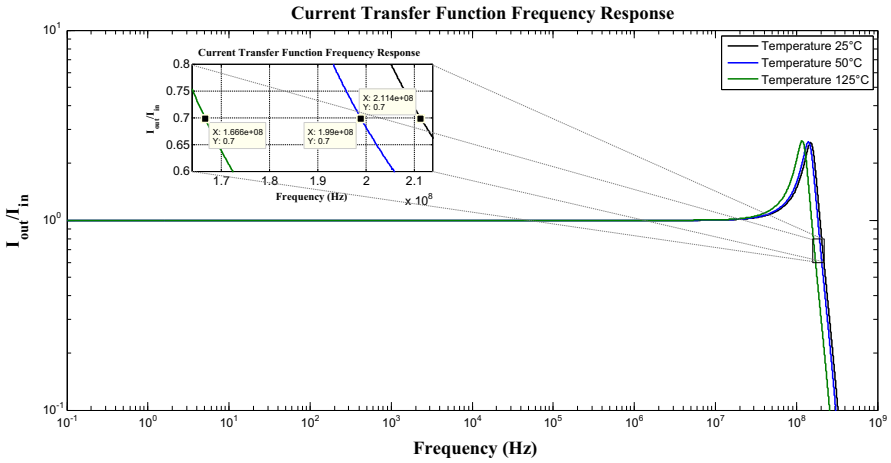


Fig. 6 Frequency response **a** typical case in comparison with other structures, **b** Monte Carlo analysis applying 5% process (W/L and V_{TH}) variations, **c** 10% variation in biasing currents and **d** temperatures of 25 °C, 50 °C and 125 °C



(c)



(d)

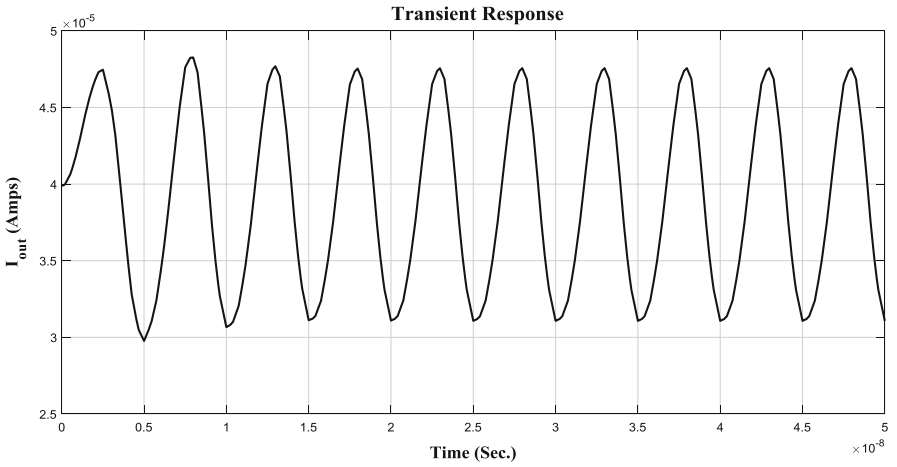
Fig. 6 continued

mirror structures as shown in Fig. 3a. This results are validated through PVT analysis which are shown in parts: Monte Carlo analysis applying 5% mismatch in transistors' both aspect ratios and threshold voltage values, 10% variations in biasing currents and temperature analysis considering operating temperatures of 25 °C, 50 °C and 125 °C as shown in Fig. 3.

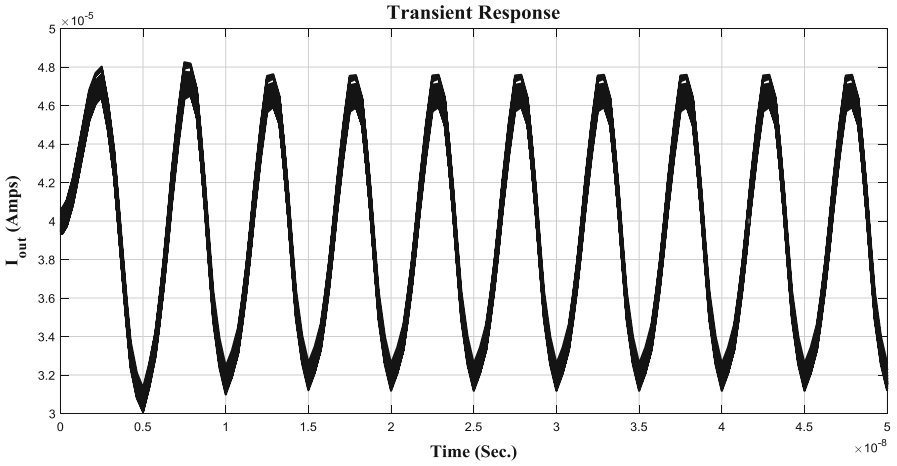
It is shown here that the current dynamic range of the proposed current mirror is wider than all other structures. The higher current transfer accuracy is another parameter that can be noticed from Fig. 3. To further investigate this parameter, the current transfer error is evaluated in Fig. 4. As this figure shows, the proposed structure exhibits very less current transfer error, which interestingly is preserved throughout its wide current dynamic range.

The current transfer error is calculated by $100(I_{\text{ideal}} - I)/I_{\text{ideal}}\%$ throughout the whole dynamic range from 0 to 320 μA. As is shown in Fig. 4, the current transfer error of the proposed circuit remains less than 0.4%, while for others, this value is more than 10 at the best condition. It is already known that using the DMOS technique [16] which is developed based on the MOS transistors' physical behavior and considering the transistor channel length and width modulation effects, the designer can further enhance the current mode circuits precision.

Figure 5 shows the output characteristics with V_{out} DC swept from 0 to 1 V and I_{in} stepped from zero to 320 μA in steps of 40 μA. As is shown, the proposed circuit exhibits much higher compliance voltages compared to other structures. The interest-

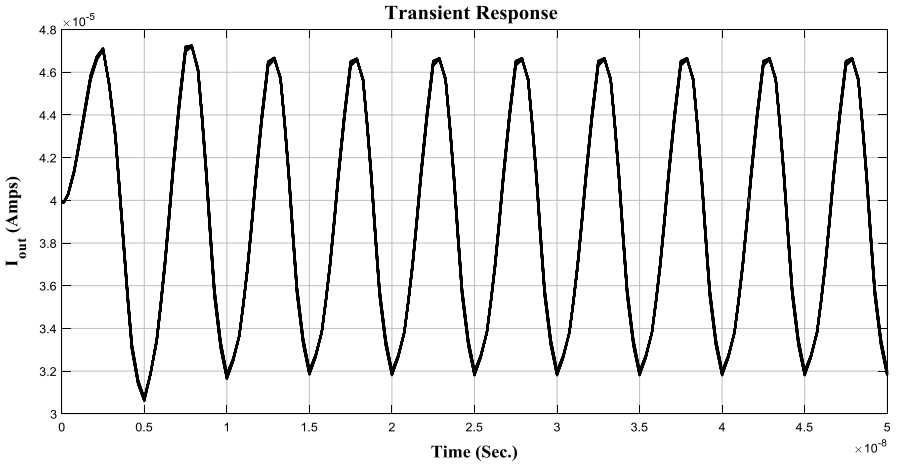


(a)

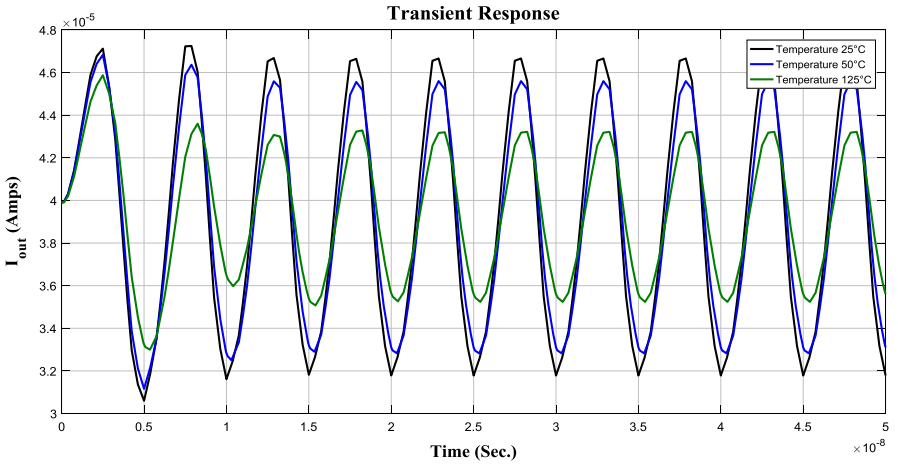


(b)

Fig. 7 Transient response **a** typical case, **b** Monte Carlo analysis applying 5% process (W/L and V_{TH}) variations **c** 10% variation in biasing currents and **d** temperatures of 25 °C, 50 °C and 125 °C



(c)



(d)

Fig. 7 continued

ing point here is that this high value of output voltage compliance is well-preserved, about 0.95 V, at high current values in the order of hundreds of μA, while, for the conventional current mirror of [2], which has the highest compliance among all other structures, the compliance drops from 0.95 to 0.8 V as its current increases from 40 to 320 μA. Another merit of the proposed structure that can be derived from Fig. 5 is its output resistance which is measured to be 121.3 GΩ at $I_{\text{in}} = 40$ μA.

The frequency performance of the proposed circuit is investigated in Fig. 6. As this figure shows, the proposed circuit presents 211 MHz–3 dB cutoff frequency. Although this is slightly less than that of its conventional version, it still has sufficient value for most applications. The output current transient response applying sinusoidal input current of "$40u + 10u \times \sin(2{*}\pi{*}200 \times 1E+6t)$" is shown in Fig. 7. Figure 8 shows

the circuit step response applying a full-scale input current signal as large as 300 μA. The simulation results approve the stability of the circuit. The total power consumption of the proposed current mirror is about 42.5 μW. In Table 2, the results of the proposed current mirror are compared with its conventional counterpart along with some other similar works in the field.

Figure 9 shows the noise performance of the proposed structure versus the conventional one [2]. The maximum output noise current is less than one nanoampere which is well below microampere dynamic range of the current mirror. The output noise current of the proposed and conventional structures is 0.8661 nA and 0.7821 nA at 10 Hz, respectively. Even though the noise contributions of the current compensated

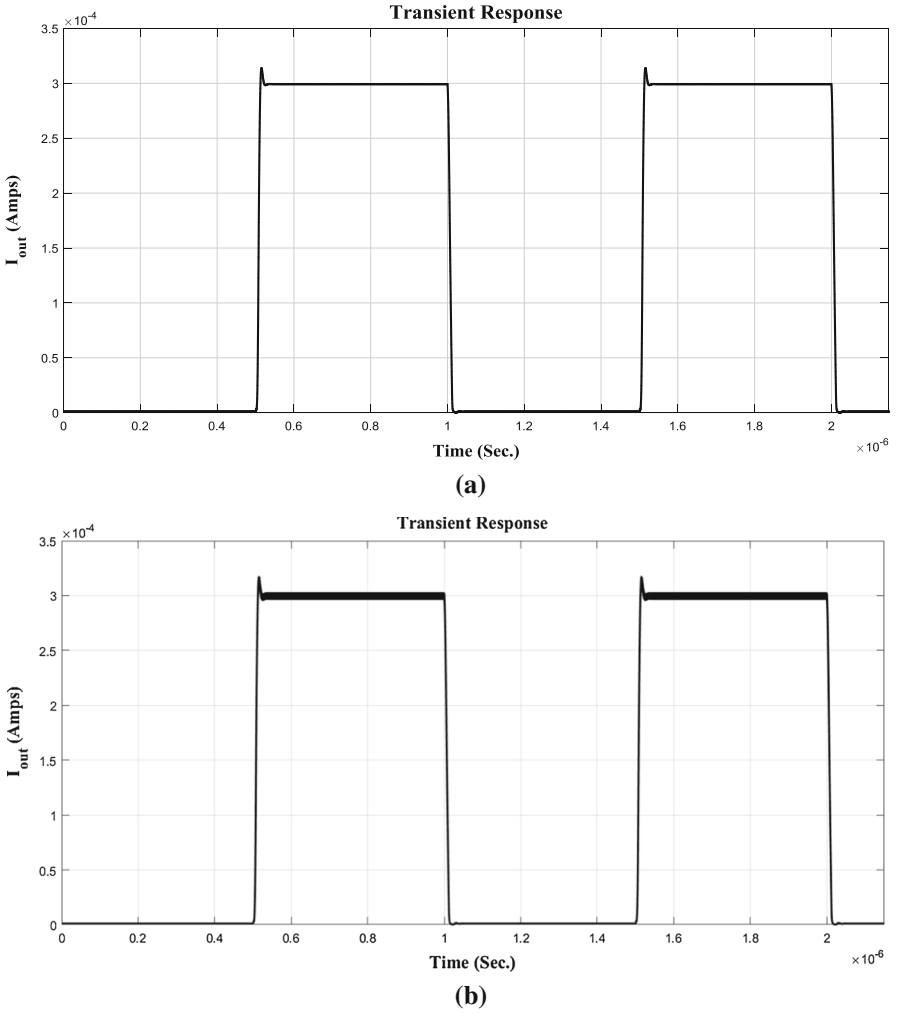
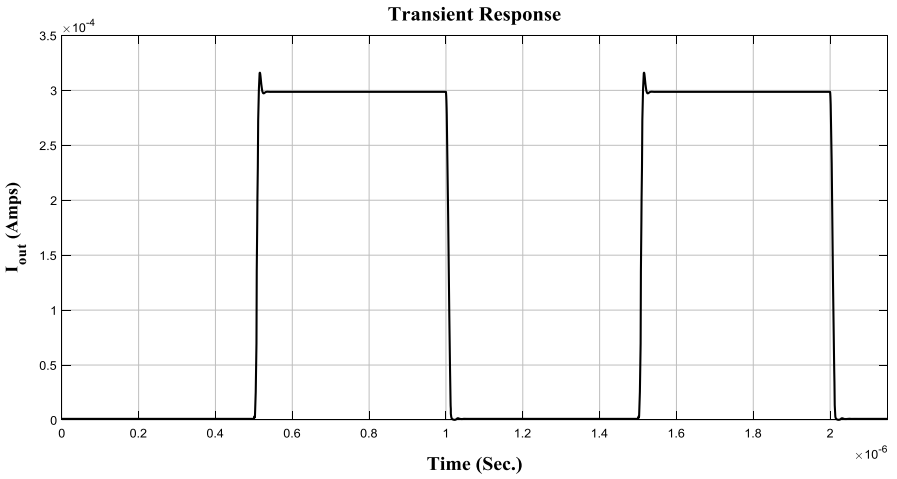
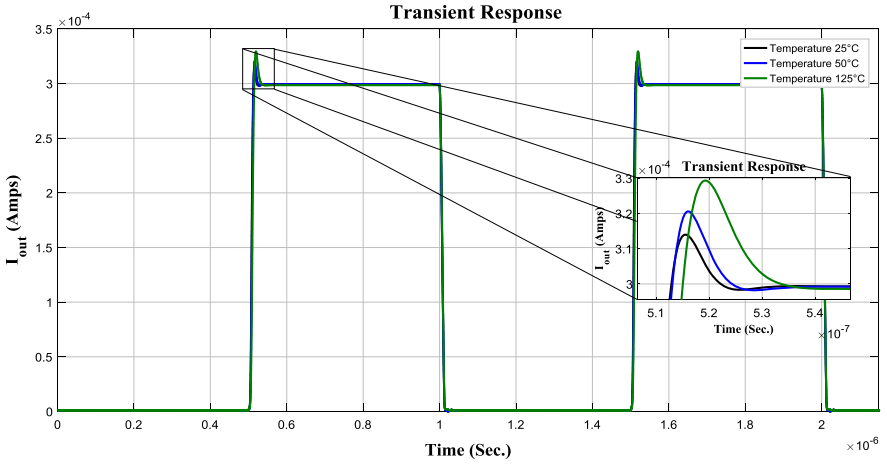


Fig. 8 Step response **a** typical case, **b** Monte Carlo analysis applying 5% process (W/L and V_{TH}) variations **c** 10% variation in biasing currents and **d** temperatures of 25 °C, 50 °C and 125 °C



(c)



(d)

Fig. 8 continued

transistors, namely M_{c1}-M_{c2}, have increased the overall output noise, it is still in an acceptable range.

The "simulation versus calculation" behavior of the input and output impedances is compared in Figs. 10 and 11, respectively. These figures exhibit well matching of the simulation results with the analytically calculated equations provided earlier in the previous section.

The normalized harmonics applying sinusoidal input current of "$40u + 10u \times \sin(2{*}\pi{*}200 \times 1E + 6t)$" is shown in Fig. 12. The total harmonic distortion for conventional and proposed circuits is 4.1247% and 9.0854%, respectively.

Table 2 Comparative results

Reference	[7]	[17]	[12]	[5]	Simple	Reg. cascode	Cascode	[2][c]	Proposed
I_{in} (μA)	NA	15	160	96	15	15	15	15	15
CDR (μA)[a]	500	100	250	100	250	200	150	320	320
RL	NA	3 K	100	NA	3 K	3 K	3 K	3 K	3 K
I_b (μA)	NA	5	20,40,160	NA	NA	5	5	5	5
$V_{in,min}$ (V)	Very large	0.058	NA	11.5% × 3.3	0.22	0.363	0.375	0.058	0.059
$V_{out,min}$ (V)	Very large	0.055	0.1 of 0.4	0.93% × 3.3	0.125	0.422	502	< 0.19@320 μA	< 0.038@320 μA
R_{in} (Ω)	679	12.8	240	16 K	1266	266.6	333	13.3	10
R_{out} (Ω)	482 M	39.5 G	19.5 G	320 G	561 K	22.5 M	4.29 G	34.3 G	121.36 G
BW(MHz)	2260	216	285	100	326–270	410	233	278	211
CTE (%)[b]	[− 2 ~ 6]	NA	[− 4–16]	0.1	[− 13–4]	[− 5 K–4]	[− 5 K–2]	[− 19.5–0.9]	[− 0.1–0.38]
P (μW)	NA	42.5	349	570	30	40	50	42.5	42.5
V supply (V)	1	1	±0.2	3.3	1	1	1	1	1
Tech.	TSMC 180 nm	TSMC180 nm	UMC180 nm	IBM130 nm	TSMC180 nm	TSMC180 nm	TSMC180 nm	TSMC180 nm	TSMC180 nm

[a]Current dynamic range
[b]Current transfer error
[c]Conventional re-simulated

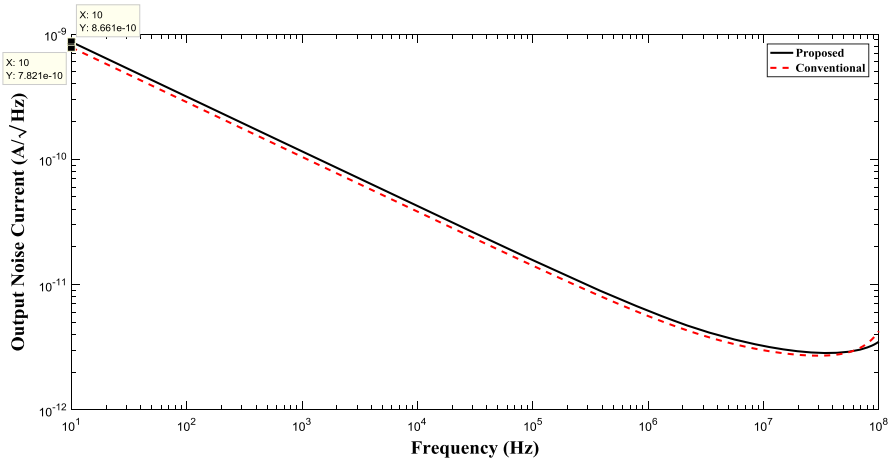


Fig. 9 Noise performance of the proposed structure versus the conventional one

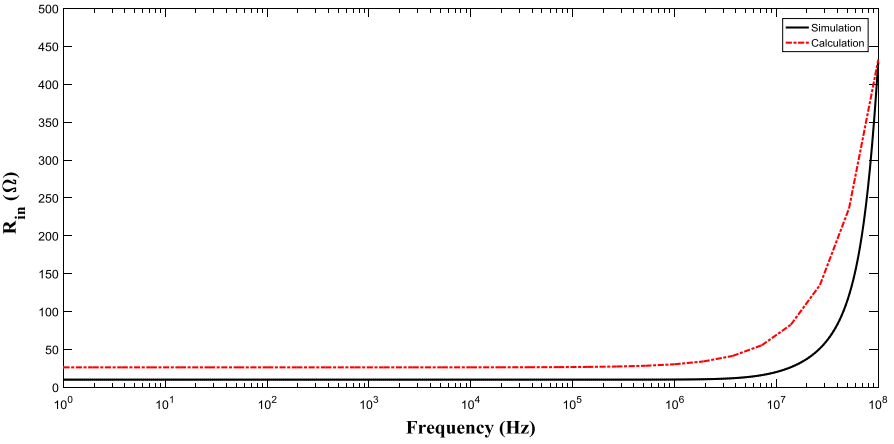


Fig. 10 Input impedance frequency-domain "simulation versus calculation" behavior comparison

4 Conclusion

In this paper, a novel ultrahigh-compliance, low-voltage and low-power current mirror was presented. The utilization of the cooperative positive–negative local feedback which was boosted by current compensation scheme exhibited the promising performance for the proposed structure in terms of the output voltage compliance and the low-voltage operation. The performance of the proposed architecture was validated by HSPICE simulation in TSMC 180 nm CMOS, BSIM3 and Level49 technology. Some of the most important parameters such as voltage compliance and frequency bandwidth were investigated by HSPICE simulations. The simulation results showed

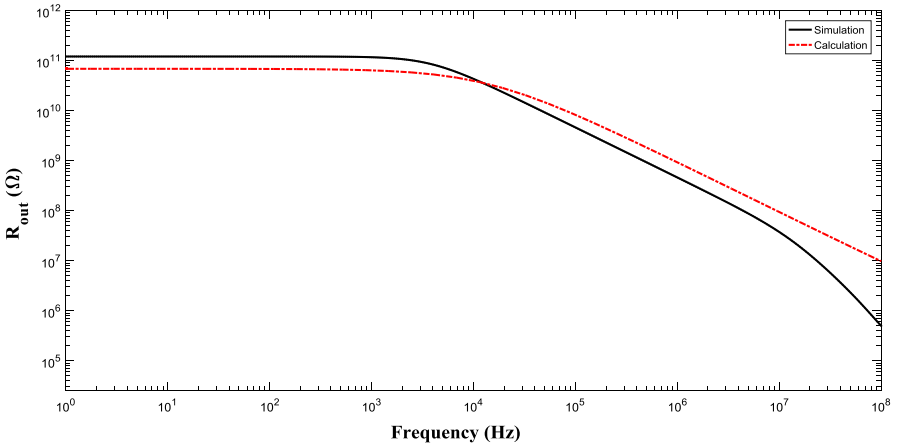


Fig. 11 Output impedance frequency-domain "simulation versus calculation" behavior comparison

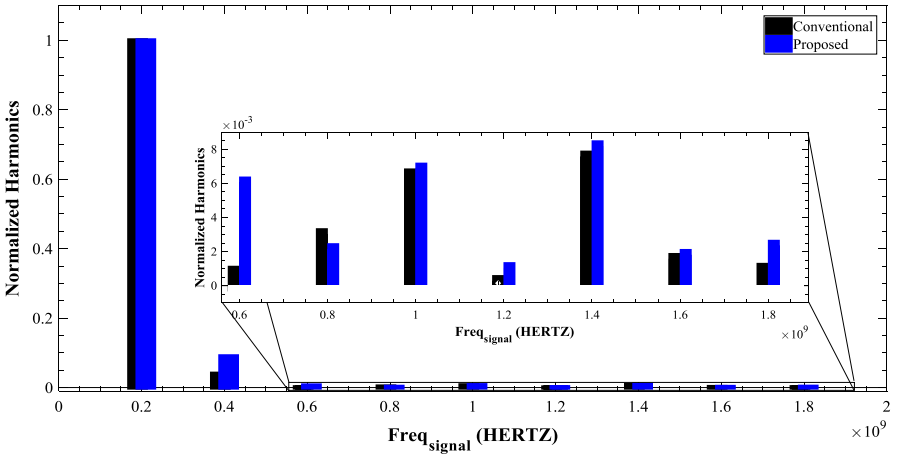


Fig. 12 Normalized harmonics for conventional and proposed circuits

input/output minimum voltages of 0.059 V/0.038 V, output resistance of 121.36 GΩ and bandwidth of 211 MHz, while it consumed only 42.5 μW from 1 V supply voltage, and its current transfer error remained less than 0.4% throughout its current dynamic range.

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