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A 99.8% Energy-Reduced Two-Stage Mixed Switching Scheme for SAR ADC Without Reset Energy

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Abstract
An ultra-low power consumption two-stage mixed switching scheme for successive approximation register (SAR) analog-to-digital converter (ADC) is presented. Using two simple switches, the novel switching scheme divides the capacitor arrays into two sub-arrays: stage-one and stage-two arrays. The two sub-arrays convert high and low bits cycles, respectively. Once the high bits conversion cycles are completed, the corresponding sub-arrays are split off from the capacitor arrays. This decreases the number of capacitors used in the rest conversion procedure. Thus, the proposed method improves the energy efficiency of SAR ADC. Thanks to C–$2C$ dummy capacitors and two-stage capacitor arrays, the novel architecture achieves 86% reduction in capacitor area than conventional SAR ADC. Furthermore, based on the charge sharing technique and monotonic switching method, the proposed switching scheme does not consume reset energy and achieves 99.8% less switching energy than the conventional switching method. In addition, the proposed scheme is less sensitive to capacitor mismatch because of its great performance in linearity.

Keywords SAR ADC · Ultra-low power consumption · Two stage · Charge sharing · C–$2C$ dummy capacitor · Switching scheme

1 Introduction

Successive approximation register (SAR) analog-to-digital converter (ADC) is widely used in low-power areas such as sensor networks [1, 12] and biomedical devices [6,

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19, 30] owing to its suitability for nanometer CMOS processes. SAR ADC mainly consists of DAC capacitor arrays, bootstrapped switches, a comparator, SAR logic units and voltage reference circuits. These are the dominant power-limiting factors [7, 20, 24, 33]. As DAC switching energy is one of the major consumption sources [2, 5, 15, 23, 34], numerous studies have been conducted to improve the power efficiency of DAC capacitor arrays.

Compared with conventional switching scheme for SAR ADC, the monotonic [10] and the V_{CM}-based [31] schemes require a large number of capacitors, causing extra area consumption. Some schemes introduced in Refs. [14, 27, 29, 32] decrease the switching energy effectively, which save energy without taking the parasitic capacitance into consideration. The methods reported in Refs. [16, 18, 22, 26] reduce switching energy by 98.83%, 98.83%, 98.4% and 98.4%, respectively, which ignore the reset energy between two sampling periods. Recently, there have been some mixed switching schemes which combine several techniques to make the scheme more energy efficient, such as Wang [21] and Liang [9]. The method reported in Ref. [21] requires 26.54 CV_{REF}^2 switching energy by splitting the MSB capacitor and applying the one-side two-level switching scheme. Unfortunately, the method reported in Ref. [21] has no advantage in power consumption after taking the parasitic capacitance into consideration and requires more switches because of split capacitors. The scheme reported in Ref. [9] consumes 7.94 CV_{REF}^2 switching energy by combining two energy-saving methods. The two methods do not require power consumption in the second comparison cycle and decrease the negative switching energy. However, the scheme reported in Ref. [9] ignores the reset energy, making the scheme energy-inefficient.

To overcome the above disadvantages, an ultra-low power consumption two-stage mixed switching scheme is presented for SAR ADC. In the proposed SAR ADC, two-stage capacitor arrays are used. The two sub-arrays (stage-one and stage-two arrays) which convert high and low bits cycles separately are connected using two simple switches. Once the high bits conversion cycles are completed, the corresponding sub-arrays are split off from the capacitor arrays, reducing the number of capacitors used in the rest conversion procedure. Thanks to C–$2C$ dummy capacitors and two-stage capacitor arrays, the novel architecture achieves 43% reduction in capacitor area over the methods reported in Refs. [9, 21]. The number of switches used in the proposed scheme is only 62.5% of that reported in Ref. [21]. Top-plate sampling is utilized in the generation of MSB to reduce energy in the first comparison. To further reduce the power, the switching scheme combines the charge sharing technique and monotonic switching method from the third comparison. The two-step method is also applied to avoid the reset energy in the proposed scheme, while the reset energy is 128 CV_{REF}^2 in [9]. Thus, the proposed switching scheme achieves 99.8% less switching energy compared with the conventional method. Even by considering parasitic capacitance, the switching energy of the proposed method is reduced by 86.8% compared with the method reported in Ref. [21].

The rest of this paper is organized as follows: the structure of proposed SAR ADC is described in Sect. 2. Section 3 illustrates the proposed switching scheme. The simulation and comparison of energy consumption based on the analysis of reset energy and parasitic capacitance are discussed in Sect. 4. Section 5 provides an explanation on non-ideal factors, including the analysis of parasitic capacitance and mismatch of

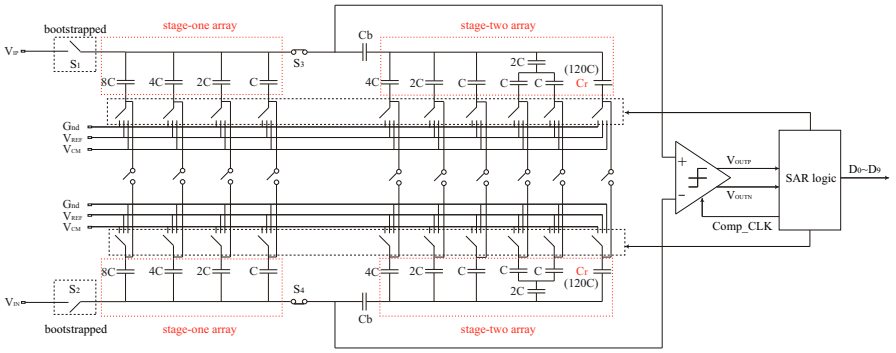

Fig. 1 Structure of SAR ADC based on proposed capacitor arrays

capacitor. Section 6 analyzes the choice of factor M. Section 7 introduces the simulation results. Section 8 reports the conclusion of entire switching scheme.

2 Structure of Proposed SAR ADC

An ultra-low power consumption two-stage mixed switching scheme is proposed for SAR ADC benefitting from the charge sharing and C–$2C$ dummy capacitor techniques in this letter. To suppress supply voltage noise and achieve good common-mode noise rejection, a fully differential architecture is used. The N-bit structure of the proposed SAR ADC consists of stage-one and stage-two arrays which determine high M bits and low N–M bits, respectively. C_b is the bridge capacitor which connects the two-stage capacitor arrays. The integral structure of the proposed switching scheme for 10-bit SAR ADC is shown in Fig. 1 with $M = 6$ (C is the unit capacitance).

The proposed SAR ADC consists of DAC capacitor arrays, bootstrapped switches S_1 and S_2, a comparator and SAR logic units. Switches S_3 and S_4 connect stage-one arrays and stage-two arrays. Through switches S_3 and S_4, the stage-one arrays are split off from the capacitor arrays after high 6 bits conversion cycles are completed, which reduces the energy consumed by DAC capacitor arrays in the following conversion cycles. The dummy capacitors of the stage-two arrays are replaced by C–$2C$ capacitors to add one-bit accuracy. For the binary matching of the whole voltage, the stage-two arrays need a redundant capacitor C_r. The value of redundant capacitor is $(2^{N-3}–2^{N-M-1})\ C$. In a 10-bit SAR ADC, the redundant capacitor is required to be $120C$ when $M = 6$. For a 10-bit SAR ADC, the proposed structure only needs 292 unit capacitors.

3 The Analysis of Switching Scheme

3.1 The Charge Sharing Technique

An equivalent model of DAC capacitor arrays is shown in Fig. 2 to illustrate the principle of the charge sharing technique. The differential DAC capacitor arrays consist

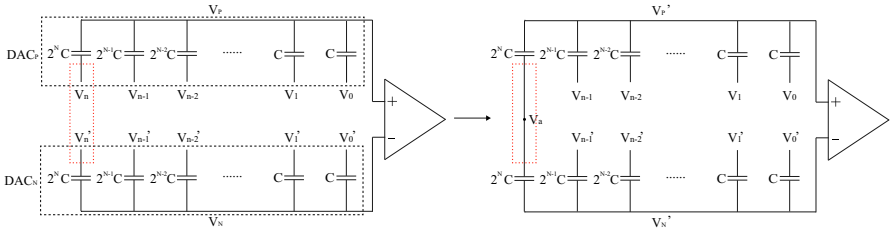

Fig. 2 Illustration of charge sharing technique

of two parts DAC_P and DAC_N as shown in Fig. 2. Before charge sharing, the initial voltages of top plate of DAC_P and DAC_N are V_P and V_N, respectively. The voltages of bottom plate of MSB capacitor are V_n and $V_n{}'$. After charge sharing, the voltages of bottom plate of MSB capacitor are set to the same voltage V_a. As a result, the voltage of top plate of DAC_P and DAC_N is changed to $V_P{}'$ and $V_N{}'$, respectively. During the procedure, the voltages of bottom plate of the rest capacitors remain unchanged. The charge sharing technique follows the principle of charge conservation.

Charge conservation of top plate on DAC_P capacitor array:

$$\begin{aligned} &2^N C \cdot (V_P - V_n) + 2^{N-1} C \cdot (V_P - V_{n-1}) + 2^{N-2} C \\ &\quad \cdot (V_P - V_{n-2}) + \cdots + C \cdot (V_P - V_1) + C \cdot (V_P - V_0) \\ &\quad = 2^N C \cdot (V_P' - V_a) + 2^{N-1} C \cdot (V_P' - V_{n-1}) + 2^{N-2} C \\ &\quad \quad \cdot (V_P' - V_{n-2}) + \cdots + C \cdot (V_P' - V_1) + C \cdot (V_P' - V_0) \end{aligned} \tag{1}$$

Charge conservation of top plate on DAC_N capacitor array:

$$\begin{aligned} &2^N C \cdot (V_N - V_n') + 2^{N-1} C \cdot (V_N - V_{n-1}') + 2^{N-2} C \\ &\quad \cdot (V_N - V_{n-2}') + \cdots + C \cdot (V_N - V_1') + C \cdot (V_N - V_0') \\ &\quad = 2^N C \cdot (V_N' - V_a) + 2^{N-1} C \cdot (V_N' - V_{n-1}') + 2^{N-2} C \\ &\quad \quad \cdot (V_N' - V_{n-2}') + \cdots + C \cdot (V_N' - V_1') + C \cdot (V_N' - V_0') \end{aligned} \tag{2}$$

Charge conservation of bottom plate of MSB capacitors:

$$2^N C \cdot (V_n - V_P) + 2^N C \cdot (V_n' - V_N) = 2^N C \cdot (V_a - V_P') + 2^N C \cdot (V_a - V_N') \tag{3}$$

Equations (1)–(3) explain the principle of charge sharing technique. After charge sharing, the voltage of bottom plate of MSB capacitor can be expressed as follows:

$$V_a = (V_n + V_n')/2 \tag{4}$$

For example, a 6-bit proposed SAR ADC is explained in detail in Fig. 3. Figure 3 shows the second bit cycle of the proposed scheme when MSB = 1 and second MSB = 0. The initial voltages of V_n and $V_n{}'$ are V_{CM} ($V_{\mathrm{CM}} = 1/2 V_{\mathrm{REF}}$) and V_{REF}, respectively.

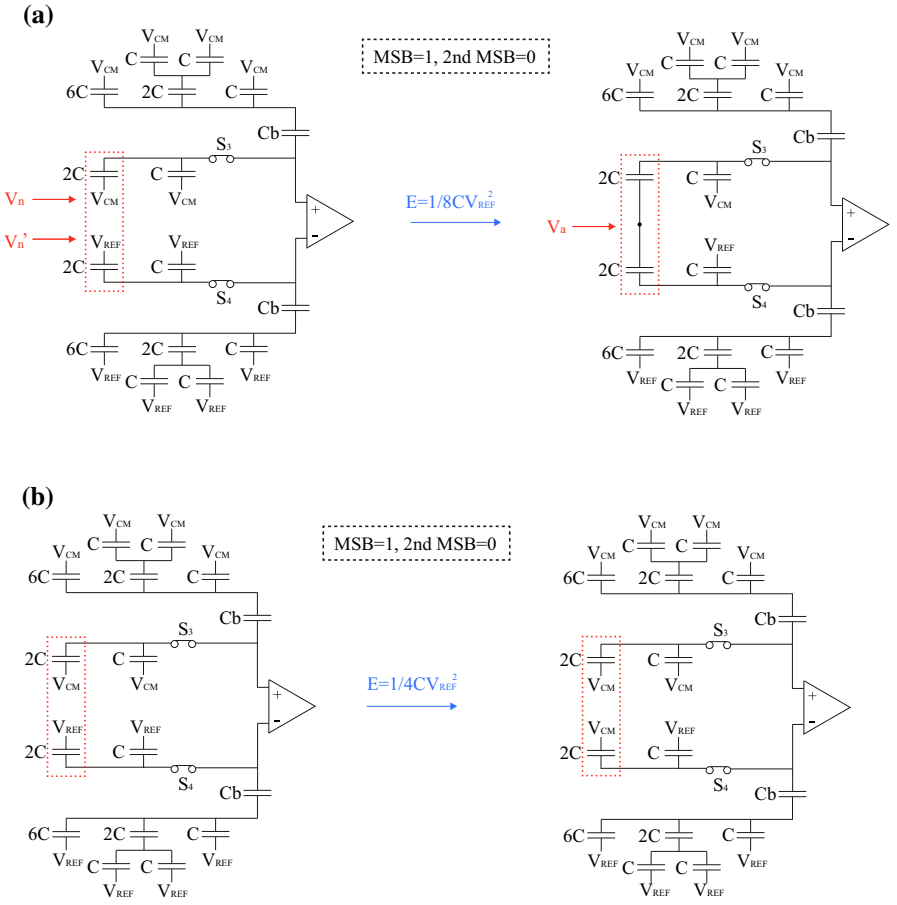

Fig. 3 Comparison of switching energy between two techniques. **a** Charge sharing technique, **b** monotonic technique

After charge sharing, the voltage V_a of bottom plate is changed to $3/4V_{\mathrm{REF}}$. As shown in Fig. 3, the charge sharing technique consumes less energy than the monotonic switching mode, thus significantly reducing overall power consumption.

3.2 Proposed Switching Scheme

The flowchart of the proposed switching scheme is shown in Fig. 4. V_P and V_N are the voltages of top plates of differential capacitor arrays. S_P and S_N represent the switches between the bottom plates of capacitors and reference voltages. A 6-bit differential SAR ADC with $M = 4$ is used to illustrate the proposed scheme shown in Fig. 5. Because the switching scheme is symmetrical, for simplicity, Fig. 5 shows the switching scheme when MSB $= 1$. At the sampling phase, switches S_1, S_2, S_3 and S_4 close. The differential input signals are sampled to the top plates of both capacitor

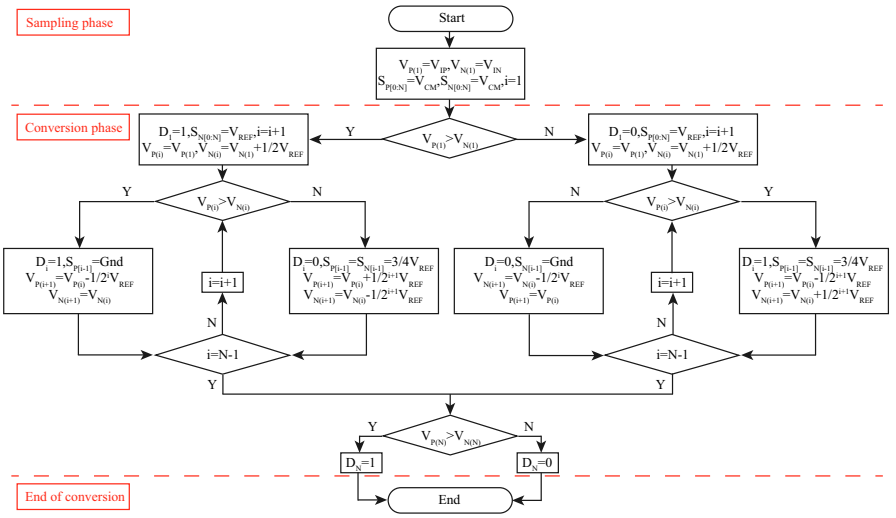

Fig. 4 Flowchart of the proposed switching scheme

arrays at the same time, and the bottom plates of all the capacitors are connected with V_{CM} ($V_{\mathrm{CM}} = 1/2V_{\mathrm{REF}}$). After the sampling phase, bootstrapped switches S_1 and S_2 open and the DAC arrays start working. At the conversion phase, the MSB is directly determined without any switching energy because of the top-plate sampling. After the first comparison, the bottom plates of capacitor array which samples the lower input voltage are connected to V_{REF} and the other capacitor array remains unchanged. After the switching activity, the voltage level of capacitors on the lower voltage side is increased by $1/2V_{\mathrm{REF}}$. Then, the comparator begins the second comparison and the second MSB is achieved. To further reduce the power, the combined monotonic and charge sharing switching method obtained from the third comparison is utilized. In this switching procedure, as soon as the potential of capacitor array which samples the lower input voltage is higher, the positive array and negative array capacitors are merged by charge sharing. In other cases, the DAC capacitor arrays perform by using the monotonic switching method. The ADC finishes the conversion of stage-one arrays until the fourth comparison is done. Before the fifth comparison, switches S_3 and S_4 are turned off, and the stage-one arrays are split off from the DAC capacitor arrays. Hence, the switching energy of the stage-one arrays in the remaining comparisons is reduced to improve the performance of SAR ADC. Then, stage-two arrays are operated to generate the rest bits. Stage-two arrays operate similarly as stage-one arrays by using the switching scheme shown in Fig. 5. Besides, the least significant bit (LSB) in stage-two is performed by reusing the unit capacitor.

The common-mode voltage variation of comparator inputs leads to input-dependent dynamic offset that deteriorates the performance of ADC. Reducing the output common-mode variation of capacitor array is important for decreasing the input-dependent offset of comparator. The waveform of the 6-bit SAR ADC is illustrated in Fig. 6. As shown in Fig. 6, the common-mode voltage variation of the proposed method is $1/4V_{\mathrm{REF}}$. Therefore, the proposed method can ease the effect of common-mode

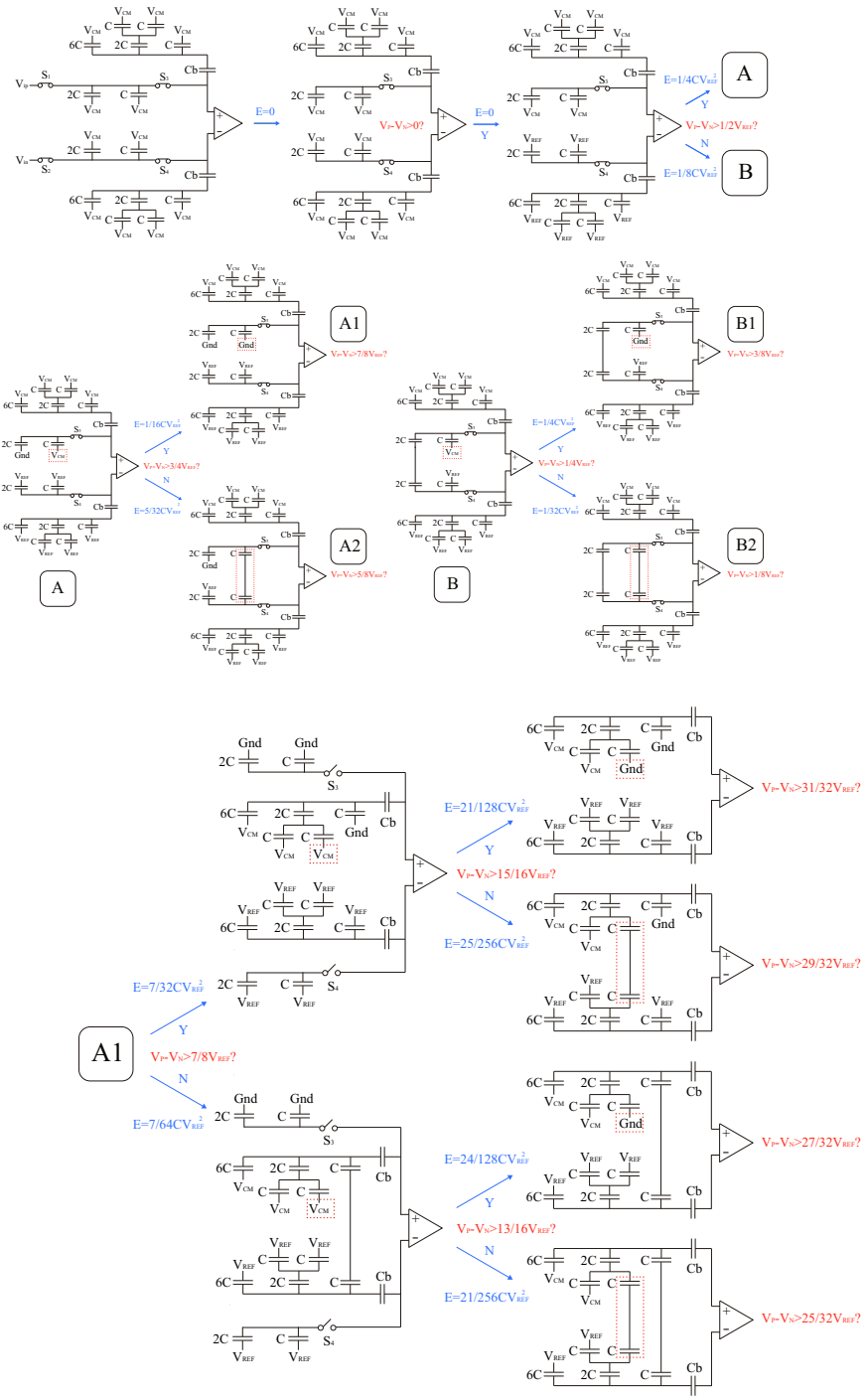

Fig. 5 Proposed switching scheme of a 6-bit SAR ADC

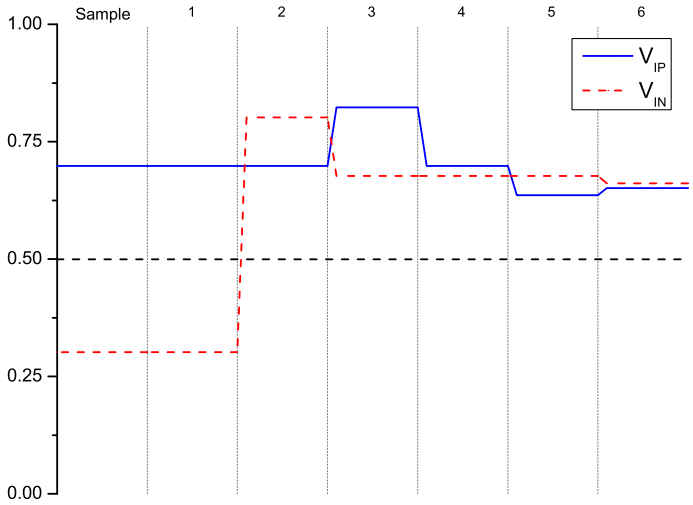

Fig. 6 Waveform of the proposed switching scheme

voltage variation on the performance of comparator. A comparison of common-mode voltage variation between the proposed scheme and existing schemes is shown in Table 2.

The generation of MSB is independent of V_{CM} because of top-plate sampling. Only one-side capacitor array switches when the second bit is generated. This makes the SAR ADC operation sensitive to the accuracy of V_{CM} from the second bit. As a result, the accuracy of V_{CM} should be ensured in the proposed method. A comparison of sensitivity to the accuracy of V_{CM} between the proposed scheme and existing schemes is shown in Table 2.

3.3 Bridge Capacitor

The proposed DAC capacitor arrays are divided into two sub-arrays through the bridge capacitor C_{b}. To make the total weight of stage-two array equal to the weight of the lowest bit in the whole array, a bridge capacitor that is non-integer times relative to the unit capacitor is inserted. The value of bridge capacitor C_{b} should be calculated using the following equations:

$$C_{\mathrm{u}} = \frac{C_{\mathrm{b}} \cdot C_{\text{stage - two}}}{C_{\mathrm{b}} + C_{\text{stage - two}}} \tag{5}$$

$$C_{\mathrm{b}} = \frac{C_{\mathrm{u}} \cdot C_{\text{stage - two}}}{C_{\text{stage - two}} - C_{\mathrm{u}}} = \frac{2^{N-3}}{2^{N-3}-1} C \tag{6}$$

C_{u} is the unit capacitor, and $C_{\text{stage-two}}$ is the value of the capacitance in the stage-two array. Besides, in the proposed structure, the accuracy of capacitance value of C_{b} has no influence on the conversion of the low bits cycle. A 6-bit SAR ADC is shown in Fig. 7 to illustrate the effect of bridge capacitor on low bits cycle. As shown in Fig. 7,

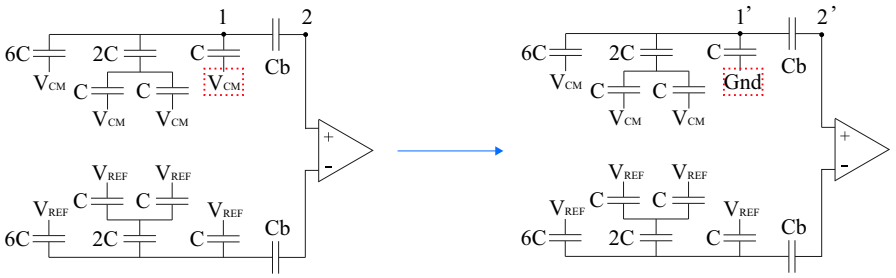

Fig. 7 Illustration for effect of bridge capacitor on low bits cycle

V_1 and V_2 are the initial voltages of nodes 1 and 2, whereas $V_1{}'$ and $V_2{}'$ are the voltages after the conversion. Nodes 1 and 2 follow the principle of charge conservation.

Charge conservation of node 1:

$$8C \cdot (V_1 - V_{\mathrm{CM}}) + C_b \cdot (V_1 - V_2) = 7C \cdot (V_1' - V_{\mathrm{CM}}) + C \cdot (V_1' - Gnd) + C_{\mathrm{b}} \cdot (V_1' - V_2') \tag{7}$$

Charge conservation of node 2:

$$C_{\mathrm{b}} \cdot (V_2 - V_1) = C_{\mathrm{b}} \cdot (V_2' - V_1') \tag{8}$$

$$\begin{aligned} \Delta V_1 &= V_1 - V_1' \\ \Delta V_2 &= V_2 - V_2' \\ \Delta V_1 &= \Delta V_2 = (1/16) V_{\mathrm{REF}} \end{aligned} \tag{9}$$

ΔV_1 is the voltage variation of top plates of stage-two capacitor array in the low bits cycle, whereas ΔV_2 is the voltage variation of input port of comparator. From above analysis, it can be concluded that ΔV_2 follows ΔV_1, which is not affected by C_{b}. Hence, the size of C_{b} does not affect the function of SAR ADC during the low bits cycle.

3.4 DAC Control Logic Analysis

A 6-bit SAR ADC introduced above is used to analyze the DAC control logic. N_i and P_i are the control signals of the ith bit (i = 1–6). DAC control logic of the proposed circuit is shown in Fig. 8. The control logics of the ith (i = 1–5) capacitor and the redundant capacitor are different. These logics have acceptable complexity. As the process technology improves, the total area and energy consumption in SAR logic are small enough compared to the switching capacitor array. A comparison of logic complexity between the proposed scheme and existing schemes is shown in Table 2.

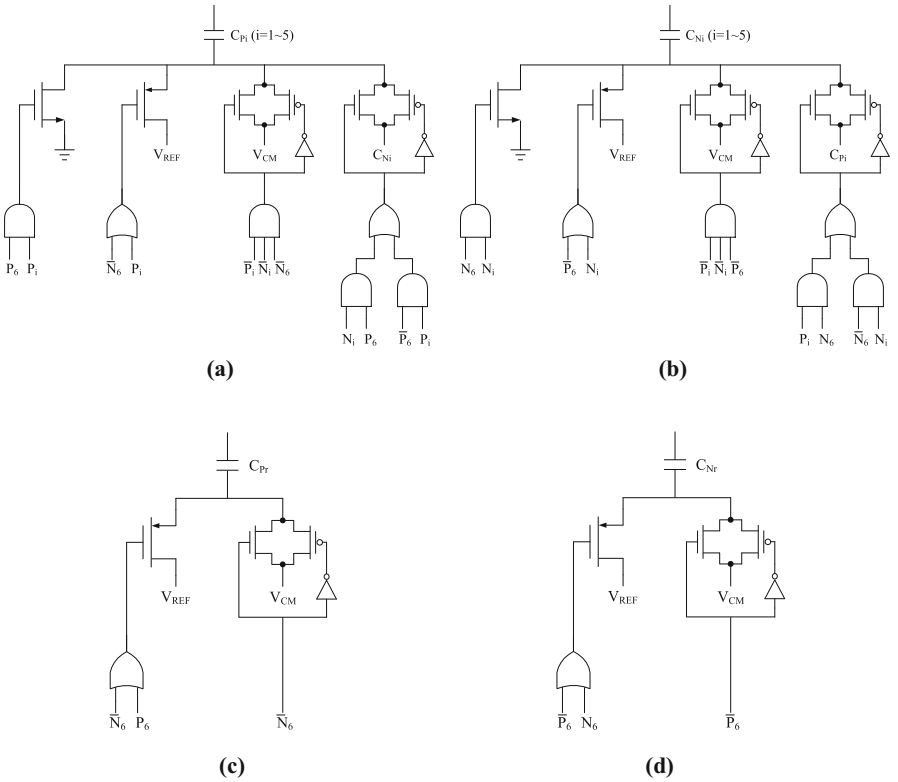

Fig. 8 Control logics of the proposed switching scheme. **a** Control logic of the *i*th ($i = 1$–5) capacitor in positive side, **b** control logic of the *i*th ($i = 1$–5) capacitor in negative side, **c** control logic of the redundant capacitor in positive side, **d** control logic of the redundant capacitor in negative side

4 Switching Energy

4.1 Switching Energy Analysis and Comparison

The behavior simulations of a differential 10-bit SAR ADC based on the switching schemes mentioned in Refs. [10, 18, 29, 31, 32] and the proposed switching scheme with $M = 6$ were performed in MATLAB. Figure 9 shows a comparison of switching energy for several switching schemes. The average switching energy for the proposed scheme is 2.9 CV_{REF}^2 and achieves 99.8% energy saving. Moreover, the proposed switching scheme achieves an area reduction of 86% with respect to conventional switching scheme.

4.2 Reset Energy Analysis and Comparison

The DAC capacitor arrays need to preload the corresponding capacitor sequences before a conversion cycle. The reset energy is needed in the procedure. A complete

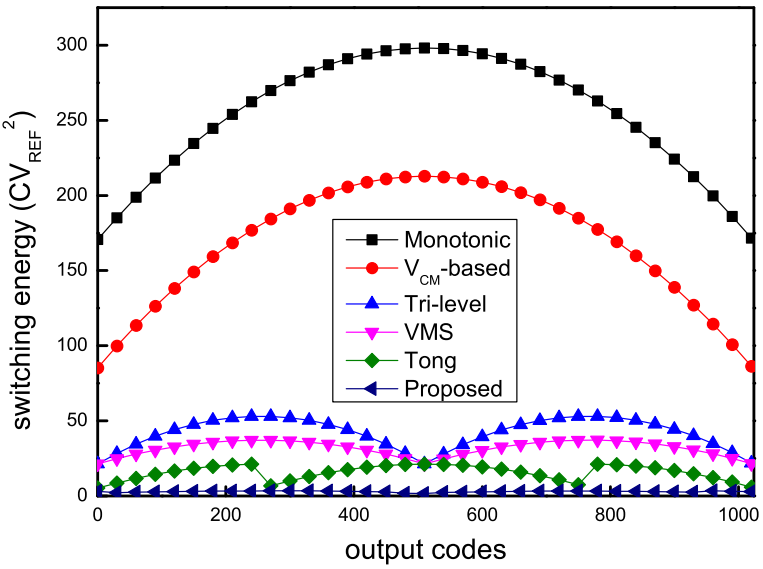

Fig. 9 Switching energy against output codes

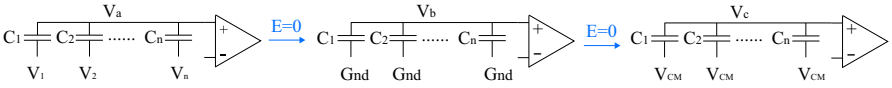

Fig. 10 Analysis of reset energy for proposed scheme

setting process for the DAC capacitor arrays consists of the switching and reset of capacitor arrays. However, all the schemes mentioned in [16, 18, 22, 26] ignored the reset energy between two sampling periods. Thus, the reset energy must be considered for an overall energy evaluation [17, 25]. According to the two-step reset method in [13], the reset process of the proposed switching scheme is shown in Fig. 10. Figure 10 shows an equivalent model of the proposed DAC arrays.

We suppose the final state as $[V_1, V_2, \ldots V_n]$. When the final state is converted to [Gnd…Gnd…Gnd], the reset energy $E_{\text{reset(step1)}}$ can be obtained as follows:

$$E_{\text{reset(step1)}} = \text{Gnd} \cdot \sum_{i=1}^{n} C_i \cdot [(\text{Gnd} - V_i) - (V_b - V_a)] = 0 \tag{10}$$

When all the capacitor states are set from [Gnd…Gnd…Gnd] to $[V_{\text{CM}} \ldots V_{\text{CM}} \ldots V_{\text{CM}}]$, the reset energy $E_{\text{reset(step2)}}$ can be obtained as follows:

$$E_{\text{reset(step2)}} = V_{\text{CM}} \cdot \sum_{i=1}^{n} C_i \cdot [(V_{\text{CM}} - \text{Gnd}) - (V_c - V_b)] \tag{11}$$

$$V_{\text{c}} - V_{\text{b}} = \frac{\sum_{i=1}^{n} (V_{\text{CM}} - G_{\text{nd}}) \cdot C_i}{\sum_{i=1}^{n} C_i} = V_{\text{CM}} - \text{Gnd} \tag{12}$$

By substituting (12) into (11):

$$E_{\text{reset(step2)}} = V_{\text{CM}} \cdot \sum_{i=1}^{n} C_i \cdot [(V_{\text{CM}} - \text{Gnd}) - (V_{\text{CM}} - \text{Gnd})] = 0$$
$$E_{\text{reset(total)}} = E_{\text{reset(step1)}} + E_{\text{reset(step2)}} = 0 \tag{13}$$

Through the above equations, the proposed method consumes zero reset energy thanks to the two-step reset method. It should be noted that the reset power is zero and independent of the final state because the initial state of the capacitor array is the same. In other words, the voltages connected to the bottom plates of all the capacitors are identical.

4.3 Effect of Parasitic Capacitance on Switching Energy

Because parasitic capacitance exists between the capacitor plates and substrate in reality, the effect of these parasitic capacitors should be considered for analyzing the switching energy consumption of SAR ADCs. Figure 11 shows a simple model for analyzing the effect of parasitic capacitors. As shown in Fig. 11, C_{pt} represents the

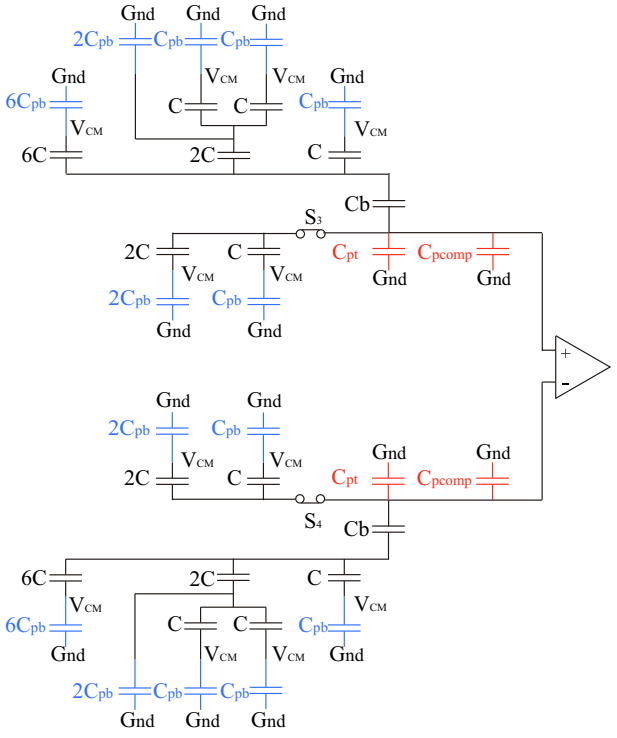

Fig. 11 Simple model for analysis of parasitic capacitance

equivalent parasitic capacitance of two stages between top plates and substrate. C_{pcomp} represents the parasitic capacitance between the input of comparator and substrate. The parasitic capacitance of a unit capacitor between bottom plates and substrate is represented as C_{pb}. Clearly, the parasitic capacitance should also be charged during the conversion cycle, thus increasing the power consumption of switching method.

After considering the parasitic capacitance, the behavior simulations of a differential 10-bit SAR ADC were performed in MATLAB. The parasitic capacitance is assumed to be $C_{\text{pt}} + C_{\text{pcomp}} = 10\%C_{\text{t}}$ and $C_{\text{pb}} = 15\%C$. C_{t} is the total capacitance, and C is the unit capacitor in the capacitor array. The average switching energy of this proposed scheme is 8.3 CV_{REF}^2, achieving energy saving by 99.5% compared with the conventional switching scheme. As discussed above, the proposed switching scheme is still energy efficient after taking the parasitic capacitance into consideration. In other words, the proposed method has low sensitivity to parasitic capacitance. A comparison of sensitivity to parasitic capacitance between the proposed scheme and existing schemes is shown in Table 1.

Tables 1 and 2 summarize the main features of the proposed switching scheme and the switching schemes mentioned in Refs. [3, 4, 8–10, 14, 16, 18, 21, 22, 26–29, 31, 32].

5 Analysis of Non-ideal Factors

5.1 Analysis of Effect of Parasitic Capacitance on Gain Error

In the proposed switching scheme, stage-one array connects stage-two array through the bridge capacitor C_{b}. In the high bits cycle, the capacitor array is equivalent to the full binary structure of capacitor array structure. In the low bits cycle, the bridge capacitor couples the voltage at node A to the input of comparator. Figures 12 and 13 illustrate the parasitic capacitance [11] of positive input port of the comparator in the high bits cycle and the low bits cycle, respectively. C_{p1} and C_{p4} are the parasitic capacitance on the top plates of stage-one array and stage-two array, respectively. C_{p2} and C_{p3} are equivalent to the parasitic capacitance on the top plate and bottom plate of the bridge capacitor, respectively. C_{p5} represents the parasitic capacitance on the top plate of the C–$2C$ capacitor.

For example, in high bits cycle, setting C_1 from V_{CM} to Gnd, the voltage change at the input port of the comparator can be obtained as follows:

$$\begin{aligned} V_{H2} - V_{H1} &= \frac{(\text{Gnd} - V_{\text{CM}}) \cdot C_1}{C_1 + C_2 + C_{p1} + C_{p2} + C_{eq1}} \\ &= \frac{-V_{\text{CM}} \cdot C_1}{C_1 + C_2 + C_{eq2}} \cdot \frac{C_1 + C_2 + C_{eq2}}{C_1 + C_2 + C_{p1} + C_{p2} + C_{eq1}} \end{aligned} \tag{14}$$

$$\begin{aligned} C_{eq1} &= C_b//[C_3 + C_5 + C_{p3} + C_{p4} + C_4//(C_6 + C_7 + C_{p5})] \\ C_{eq2} &= C_b//[C_3 + C_5 + C_4//(C_6 + C_7)] \end{aligned} \tag{15}$$

Table 1 Comparison of energy between different schemes for 10 bit SAR ADC

Switching scheme	Average switching energy (CV^2_{REF})		Energy saving (%)	Reset energy (CV^2_{REF})	Total energy (CV^2_{REF})	Total energy saving (%)
	$C_{pt} + C_{pcomp} = C_{pb} = 0$	$C_{pt} + C_{pcomp} = 10\%C_t$ $C_{pb} = 15\%C$				
Conventional	1363.3	1686.1	Reference	0	1363.3	Reference
Monotonic [10]	255.5	255.5	81.26	0	255.5	81.26
V_{CM}-based [31]	170.17	209.2	87.52	0	170.17	87.52
Tri-level [29]	42.42	74.8	96.89	0	42.42	96.89
VMS [32]	31.88	56.3	97.66	0	31.88	97.66
Sanyal and Sun [14]	21.3	33.15	98.4	95.75	117.05	91.4
Charge redistribution [27]	31.88	38.86	97.66	117.2	149.08	89.06
Tong and Ghovanloo [16]	15.88	43.7	98.83	50.84	66.72	95.1
Xie [26]	21.2	26.7	98.4	121.2	142.4	89.55
Wu and Wu [22]	21.3	N.A.[b]	98.4	64	85.3	93.74
Tong [18]	15.88	21.3	98.83	83.59	99.47	92.7
Wang [21]	26.54	62.65	98.05	0	26.54	98.05
Liang [9]	7.94	N.A.[b]	99.4	128[a]	135.94	90.02
Asymmetric [8]	13.53	17.6	99.01	0	13.53	99.01
Trade-off [3]	26.54	N.A.[b]	98.05	0	26.54	98.05
LSB split [4]	10.8	16.78	99.2	48.12	58.92	95.6
Yousefi [28]	0	N.A.[b]	100	62[a]	62	95.45
Proposed	2.9	8.3	99.8	0	2.9	99.8

[a]Not provided by authors, estimation made in this paper according to the method in [13]
[b]The values are not provided by authors

Table 2 Comparison of other features between different schemes for 10 bit SAR ADC

Switching scheme	Total number of unit capacitors	Area reduction (%)	Logic complexity	Maximum common-mode variation	Sensitivity to the accuracy of V_{CM}
Conventional	2048	Reference	Low	0	No
Monotonic [10]	1024	50	Low	$V_{REF}/2$	No
V_{CM}-based [31]	1024	50	Low	0	No
Tri-level [29]	512	75	Medium	$V_{REF}/2$	From second bit
VMS [32]	512	75	Medium	$V_{REF}/4$	From second bit
Sanyal and Sun [14]	512	75	Medium	$V_{REF}/4$	From third bit
Charge redistribution [27]	512	75	Low	N.A.[a]	No
Tong and Ghovanloo [16]	512	75	Low	N.A.[a]	From third bit
Xie [26]	512	75	N.A.[a]	1LSB	Only LSB
Wu and Wu [22]	512	75	N.A.[a]	0.5LSB	Only LSB
Tong [18]	512	75	Low	$V_{REF}/2$	From second bit
Wang [21]	512	75	Medium	$V_{REF}/4$	From second bit
Liang [9]	512	75	Low	$V_{REF}/4$	From third bit
Asymmetric [8]	384	81.25	Medium	$V_{REF}/4$	From second bit
Trade-off [3]	512	75	N.A.[a]	$V_{REF}/2$	From second bit
LSB split [4]	256	87.5	Medium	$V_{REF}/4$	From third bit
Yousefi [28]	248	87.8	High	0	No
Proposed	292	86	Low	$V_{REF}/4$	From second bit

[a]The values are not provided by authors

Therefore, the gain error in high bits is

$$\text{Gain\_error}_H = \frac{C_1 + C_2 + C_{eq2}}{C_1 + C_2 + C_{p1} + C_{p2} + C_{eq1}} \tag{16}$$

In low bits cycle, when C_3 is set from V_{CM} to Gnd, the voltage change at node A should be:

$$V_{A2} - V_{A1} = \frac{(\text{Gnd} - V_{CM}) \cdot C_3}{C_3 + C_5 + C_{p3} + C_{p4} + C_4//(C_6 + C_7 + C_{p5}) + C_b//C_{p2}}$$

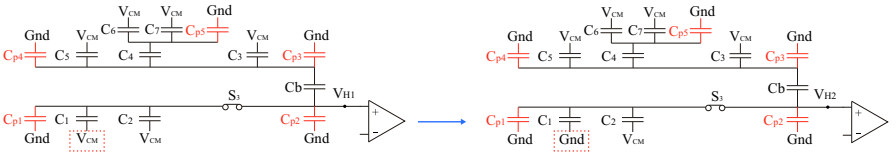

Fig. 12 Analysis of parasitic capacitance in the high bits cycle

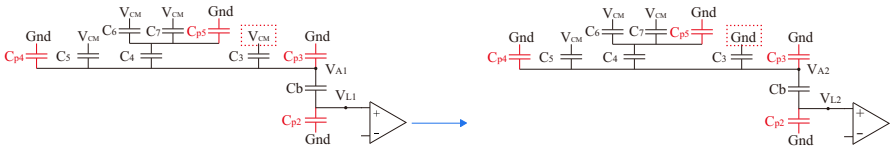

Fig. 13 Analysis of parasitic capacitance in the low bits cycle

$$= \frac{-V_{\mathrm{CM}} \cdot C_3}{C_3 + C_5 + C_4//(C_6 + C_7) + C_{\mathrm{b}}} \cdot \frac{C_3 + C_5 + C_4//(C_6 + C_7) + C_{\mathrm{b}}}{C_3 + C_5 + C_{\mathrm{p3}} + C_{\mathrm{p4}} + C_4//(C_6 + C_7 + C_{\mathrm{p5}}) + C_{\mathrm{b}}//C_{\mathrm{p2}}} \tag{17}$$

The voltage change at the input port of the comparator should be:

$$V_{L2} - V_{L1} = \frac{(V_{A2} - V_{A1}) \cdot C_b}{C_b + C_{p2}} = \frac{-V_{CM} \cdot C_3}{C_3 + C_5 + C_4//(C_6 + C_7) + C_b} \cdot \frac{C_b}{C_b + C_{p2}} \cdot \frac{C_3 + C_5 + C_4//(C_6 + C_7) + C_b}{C_3 + C_5 + C_{p3} + C_{p4} + C_4//(C_6 + C_7 + C_{p5}) + C_b//C_{p2}} \tag{18}$$

Therefore, the gain error in low bits is

$$\mathrm{Gain\_error}_L = \frac{C_b}{C_b + C_{p2}} \cdot \frac{C_3 + C_5 + C_4//(C_6 + C_7) + C_b}{C_3 + C_5 + C_{p3} + C_{p4} + C_4//(C_6 + C_7 + C_{p5}) + C_b//C_{p2}} \tag{19}$$

If the value of parasitic capacitance on top plates is linear to the total value of DAC arrays, defaulting the ratio as η, the value of parasitic capacitance can be defined as follows:

$$C_{p1} = \eta \cdot (C_1 + C_2), C_{p2} = \eta \cdot C_b, C_{p3} = \eta \cdot C_b, C_{p4} = \eta \cdot (C_3 + C_4 + C_5), C_{p5} = \eta \cdot (C_6 + C_7) \tag{20}$$

$$\mathrm{Gain\_error}_H = \frac{1}{1 + \eta} \tag{21}$$

$$\mathrm{Gain\_error}_L \approx \frac{1}{(1 + \eta)^2} \tag{22}$$

From the above analysis, it can be found that the bridge capacitor slightly affects the gain error of parasitic capacitance. Besides, the high bits comparison and low bits comparison have different gain errors.

5.2 Analysis of Effect of Capacitor Mismatch on Linearity

Due to process variation, the practical capacitance of each unit capacitor deviates from the nominal value. Capacitor mismatch is very important, and it determines the linearity of the SAR ADC [3, 8]. Some existing methods pursue the reduction of power dissipation but neglect the decrease in linearity, which require large unit capacitor and consume more energy. After taking the capacitor mismatch into account, simulation building with the unit capacitor obeys a Gaussian distribution, modeled with a nominal value of C_u and a standard deviation of σ_u.

For a given digital input, the analog output of N-bit capacitive DAC for the proposed switching scheme can be expressed as follows:

$$V_{\mathrm{DAC}}(X) = \left(\frac{\sum_{i=N-M}^{N-3} (2^{i-(N-M)} C_u + \delta_i) d_{p,i}}{2^{M-2} C_u} + \frac{\sum_{i=0}^{N-M-1} (2^{i-1} C_u + \delta_i) d_{p,i}}{2^{N-3} C_u} - \frac{\sum_{i=N-M}^{N-3} (2^{i-(N-M)} C_u + \delta_i) d_{n,i}}{2^{M-2} C_u} - \frac{\sum_{i=0}^{N-M-1} (2^{i-1} C_u + \delta_i) d_{n,i}}{2^{N-3} C_u} \right) V_{\mathrm{REF}} \tag{23}$$

where $d_{(p,n),i}$ is equal to 0, 1/2 or 1 representing the DAC connecting to Gnd, V_{CM}, V_{REF} for bit i, respectively. M is the bits that the stage-one determines.

INL can be expressed as:

$$\mathrm{INL}(X) = V_{\mathrm{DACP,real}}(X) - V_{\mathrm{DACP,ideal}}(X) \tag{24}$$

$$\mathrm{INL}(X) = \left(\frac{\sum_{i=N-M}^{N-3} \delta_i \cdot d_{p,i}}{2^{M-2} C_u} + \frac{\sum_{i=0}^{N-M-1} \delta_i \cdot d_{p,i}}{2^{N-3} C_u} - \frac{\sum_{i=N-M}^{N-3} \delta_i \cdot d_{n,i}}{2^{M-2} C_u} - \frac{\sum_{i=0}^{N-M-1} \delta_i \cdot d_{n,i}}{2^{N-3} C_u} \right) V_{\mathrm{REF}} \tag{25}$$

$$\sigma^2_{\mathrm{INL}}(X) = \left(\frac{\sum_{i=N-M}^{N-3} (\delta_i \cdot d_{p,i})^2}{(2^{M-2} C_u)^2} + \frac{\sum_{i=0}^{N-M-1} (\delta_i \cdot d_{p,i})^2}{(2^{N-3} C_u)^2} - \frac{\sum_{i=N-M}^{N-3} (\delta_i \cdot d_{n,i})^2}{(2^{M-2} C_u)^2} - \frac{\sum_{i=0}^{N-M-1} (\delta_i \cdot d_{n,i})^2}{(2^{N-3} C_u)^2} \right) V^2_{\mathrm{REF}} \tag{26}$$

DNL can be expressed as:

$$\mathrm{DNL}(X) = \mathrm{INL}(X) - \mathrm{INL}(X-1) \tag{27}$$

$$\mathrm{DNL}(X) = \left(\frac{\sum_{i=N-M}^{N-3} \delta_i \cdot \Delta d_{p,i}}{2^{M-2} C_u} + \frac{\sum_{i=0}^{N-M-1} \delta_i \cdot \Delta d_{p,i}}{2^{N-3} C_u} - \frac{\sum_{i=N-M}^{N-3} \delta_i \cdot \Delta d_{n,i}}{2^{M-2} C_u} - \frac{\sum_{i=0}^{N-M-1} \delta_i \cdot \Delta d_{n,i}}{2^{N-3} C_u} \right) V_{\mathrm{REF}} \tag{28}$$

$$\sigma^2_{\mathrm{DNL}}(X) = \left(\frac{\sum_{i=N-M}^{N-3} (\delta_i \cdot \Delta d_{p,i})^2}{(2^{M-2} C_u)^2} + \frac{\sum_{i=0}^{N-M-1} (\delta_i \cdot \Delta d_{p,i})^2}{(2^{N-3} C_u)^2} - \frac{\sum_{i=N-M}^{N-3} (\delta_i \cdot \Delta d_{n,i})^2}{(2^{M-2} C_u)^2} - \frac{\sum_{i=0}^{N-M-1} (\delta_i \cdot \Delta d_{n,i})^2}{(2^{N-3} C_u)^2} \right) V^2_{\mathrm{REF}} \tag{29}$$

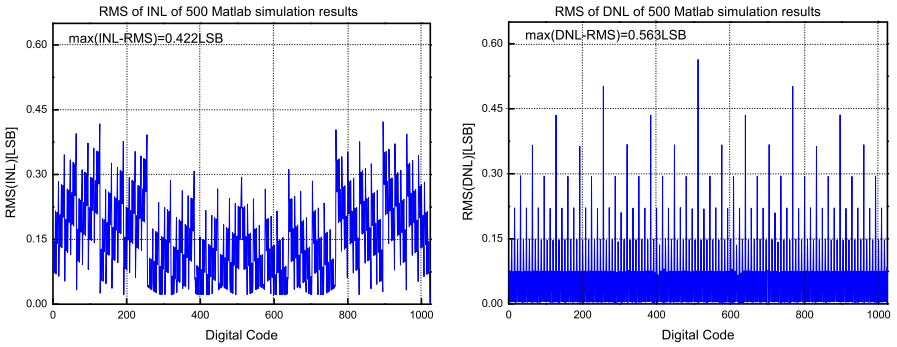

Fig. 14 Simulation results of INL and DNL for the conventional switching scheme

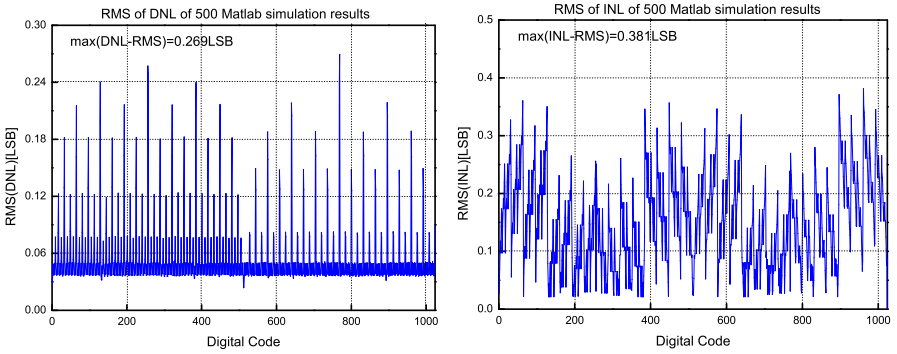

Fig. 15 Simulation results of DNL and INL for the proposed switching scheme

5.3 Linearity Simulation

A 500-runs Monte–Carlo simulation of a 10-bit SAR ADC was performed in MATLAB for the effect of capacitor mismatch on linearity, with the mismatch of unit capacitor satisfying $3\sigma_u = 0.01C$ [4, 28]. Figures 14 and 15 show the simulation results of DNL and INL for the conventional switching scheme and the proposed switching scheme. The root-mean-square (RMS) values of maximum DNL and INL for the proposed switching scheme are 0.269LSB and 0.381LSB, respectively. The simulation results indicate that the proposed switching scheme has good performance in linearity.

6 Choose of Factor *M*

For a 10-bit SAR ADC, the value of M can be different. The switching energy and area reduction were simulated in MATLAB at different values of M for proposed 10-bit SAR ADC, and the result is shown in Fig. 16. The effects of different M on the linearity, switching energy and number of capacitors are shown in Table 3. Table 3 indicates that with the increase in M value, the number of capacitors increases, reducing the mismatch of capacitor arrays and improving the linearity of the proposed scheme.

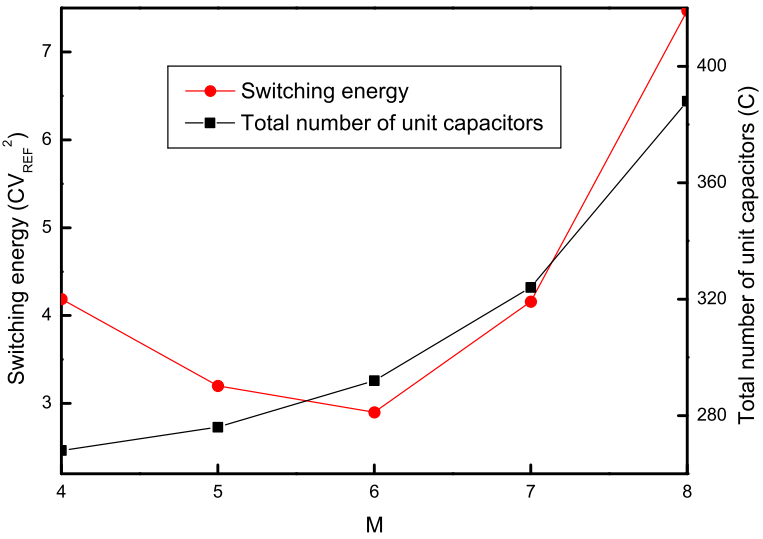

Fig. 16 Switching energy and number of capacitors with M varying from 4 to 8

Table 3 Features of the proposed switching scheme with M varying from 4 to 8

The value of M	Value of C_r (C)	Total number of unit capacitors (C)	Average switching energy (CV_{REF}^2)	DNL (LSB)	INL (LSB)
4	96	268	4.19	0.618	0.836
5	112	276	3.18	0.403	0.563
6	**120**	**292**	**2.9**	**0.269**	**0.381**
7	124	324	4.16	0.186	0.264
8	126	388	7.47	0.128	0.185

Bold values indicate the optimal choice for a 10-bit SAR ADC with the proposed switching scheme

When M is 6, the number of capacitors, switching energy and linearity achieve a balance.

7 Simulation Results

A 40 MS/s 10-bit 1 V SAR ADC used in the proposed switching scheme was implemented in MATLAB. The simulation was implemented after taking V_{CM} variations and capacitance mismatch into account. The deviation in V_{CM} value and mismatch of capacitor are set as 10 mV and $\sigma = 1\%$, respectively. A 16384-point fast Fourier transform (FFT) of the 40 MS/s SAR ADC when the input frequency is 12.47 MHz is shown in Fig. 17. The signal-to-noise and distortion ratio (SNDR) and the spurious-free dynamic range (SFDR) can reach 61.40 and 82.52 dB, respectively. Figure 18

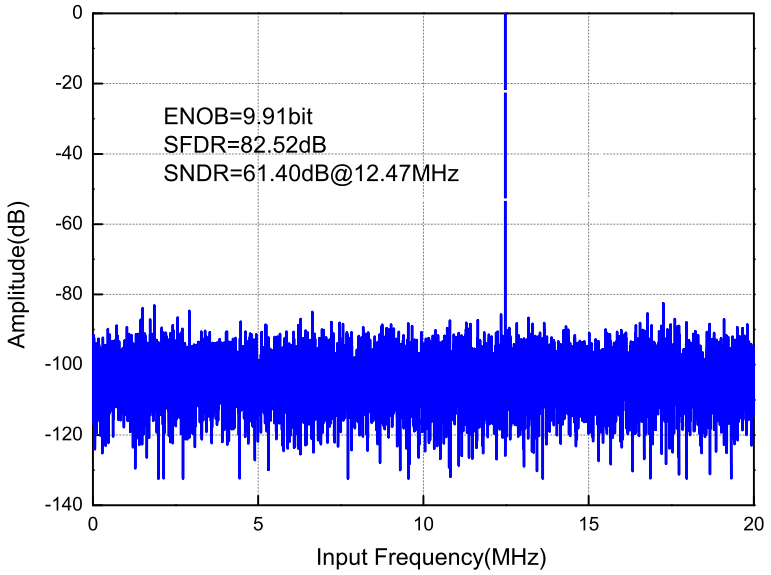

Fig. 17 16384-point FFT spectrum at 40 MS/s with Nyquist input

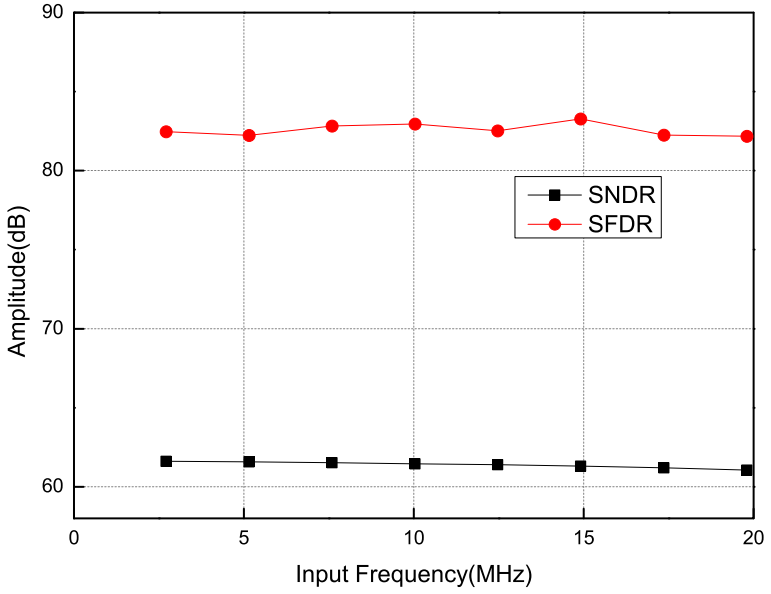

Fig. 18 Dynamic performance of the SAR ADC versus the input

exhibits the dynamic performance as the input frequency is swept at 40 MS/s. The ADC achieved a peak SNDR of 61.62 dB.

8 Conclusion

This paper proposes an ultra-low power consumption two-stage mixed switching scheme which applies to SAR ADC. The proposed switching scheme adopts two-stage capacitor arrays with a novel mixed method. Thanks to C–$2C$ dummy capacitors and two-stage capacitor arrays, the novel architecture achieves 86% reduction in capacitor area over the conventional SAR ADC. Furthermore, based on the charge sharing technique and monotonic switching method, the proposed switching scheme does not consume reset energy and achieves 99.8% less switching energy compared with the conventional switching method. In addition, the proposed scheme is less sensitive to capacitor mismatch because of its great performance in linearity. Therefore, the proposed switching scheme is suitable for the ultra-low power consumption SAR ADC, which is more energy efficient and area efficient among the reported switching schemes.

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