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SHORT PAPER

Design and Analysis of Low-Power Adiabatic Logic Circuits by Using CNTFET Technology

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Abstract
Miniaturization of semiconductor industries paved the way for rapid development in the field of digital electronics. In DSM range, power dissipation has become a major concern due to leakage currents; hence, researchers are continuously trying to evolve ways to mitigate this. Out of many such ways the use of carbon nanotube technology is a promising way to design low-power circuits, as carbon has a property of providing variable threshold voltage (V_{TH}) in N-type transistors. Here simulation results confirm that CNTFET has better performance than MOS and FinFET technologies in low-power world. In this paper existing and proposed adiabatic logic is implemented by CNTFET technology at 32 nm in HSPICE by using Predictive Technology Model (PTM). Comparison of simulation results shows that proposed CNTFET-based ON–OFF-DCDB-PFAL adiabatic logic saves average power 94.33% in Buffer/NOT, 93.13% in NAND/AND, 93.14% in NOR/OR, 91.76% in XOR/XNOR when compared with 2N2N2P circuit at 10 MHz frequency.

Keywords CNTFET · Chirality · Diameter · Threshold voltage · Energy gap · PFAL

1 Introduction

Shrinking transistor dimensions for achieving higher density and performance is steadily going on resulting in various types of leakage currents inside the devices. Carbon nanotube field effect transistor (CNTFET) is a device which can mitigate these leakage currents. Static power dissipation is a critical issue in DSM range to be minimized because devices like cellular phones, multimedia devices and

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personal note books have dependency on battery which is having limited power. As the device size reduces, power consumption increases due to millions of transistor built on system on chip (SoC) and also increase of leakage currents in DSM range, and researchers are evolving various power minimization ways at different levels of design [6, 21]. Total power dissipation in CMOS circuit is due to dynamic and static (leakage) power [7]. Scaling the power supply in circuit is the most dominating method for reducing the dynamic and short-circuit power dissipation, but this increases propagation delay; hence, supply voltage of critical path is not altered because of speed constrain of the design [20, 21].

The main aim of the adiabatic circuit design is to reduce the loss of energy during charging/discharging in CMOS design. Charging and discharging of the load capacitance takes time, so transition becomes slow which results in no emission of heat inside the adiabatic circuits. This is achieved by using AC power supply rather DC power supply to initially charge the load capacitance during specific adiabatic phases and then discharge it to recover the supplied charge. The AC supply used is a constant charging current source that is a linear voltage ramp. If the constant current source delivers the charge $\left(Q = \mathrm{CV_{DD}}\right)$ during the time period T, the energy dissipated in the channel resistance R is given by

$$E = I^2RT = \left(\frac{CV_{\mathrm{DD}}}{T}\right)^2 RT = \frac{RC}{T}CV_{\mathrm{DD}}^2 \tag{1}$$

where V_{DD} is supply voltage. R is resistance of FET. C is node capacitance. From the above equation, as the T is increased linearly, power dissipation will decrease. If T is made sufficiently larger than RC, the energy dissipation will be nearly zero and here lies the principle of adiabatic switching. Adiabatic logic proves to be better choice instead of CMOS logic, and in DSM range, the use of CNTFET proves to be better counter part of MOSFET (including FinFETs [7]).

Carbon nanotube-based FET CNTFET is the best material to the silicon-based MOSFET due to its quasi-ballistic transportation ability, negligible temperature dependency, high carrier mobility, high current density, easy integration with high-k dielectric material with easy fabrication feasibility [2, 12]. CNTFET has lower intrinsic gate delay, energy consumption, f current and variable threshold and can be used as multi-threshold voltage transistor in devices. A single-wall carbon nanotube (SWCNT) is made up with rolling a single graphene sheet, and multi-wall carbon nanotube (MWCNT) is made up with rolling multiple sheets of graphene. CNT has a perfect crystalline graphene structure that contains strong covalent C–C bond strongest material ever tested [19].

The objective of this manuscript is to compare average power dissipation in adiabatic circuits made with technologies like MOS, FinFET and CNTFET. The rest of this paper is organized as follows: Study of basic structure of CNTFET in Sects. 2 and 3 working of existing adiabatic circuit is discussed. Section 4 describes the proposed ON–OFF-DCDB-PFAL adiabatic circuit for mitigation of power dissipation. Section 5 is of results and discussion, and here average power,

delay, PDP and EDP are calculated by using CNTFET-based adiabatic circuits. Finally, conclusion is offered in Sect. 5.

2 CNTFET

Carbon nanotube (CNT) is made up of rolling a sheet of graphene. On the basis number of concentric layers of CNT, it is called single-walled or multi-walled CNT, and on the basis of vector direction a_1 and a_2 of rolling a sheet (also called chirality), it can act as metallic or semiconducting. The chirality index (m, n) is used to identify the direction of rolling of graphene sheet, Fig. 1. The carbon nanotube is metallic if $m=n$ or the difference $(m-n)=3$ k where k is an integer; otherwise, it acts as semiconducting material [10, 18]. Conductive or metallic is used as connection wire on chip, and semiconducting CNTs are used as channel of transistor or SWCNT and MWCNT channel. The diameter of CNT is given by Eq. (2) [11]

$$D_{\mathrm{CNT}} = a\sqrt{\frac{m^2+n^2+mn}{\pi}} \tag{2}$$

where m and n are chirality index of CNT and a is the lattice constant (2.49 Å). Top view of CNTFET is shown in Fig. 2. Width of the CNTFET gate $\left(W_{\mathrm{gate}}\right)$ is calculated by Eq. (3) [11]

$$\approx \mathrm{Max}\left(W_{\mathrm{min}}, N \times \mathrm{Pitch}\right) \tag{3}$$

where Pitch is the distance between centers of two neighboring SWCNTs under the same gate, W_{min} is minimum gate width, and N is the no. of nanotubes.

The layout of CNTFET is approximately the same to traditional MOSFET except the channel between source and drain region is replaced by carbon tubes of nano-range dimensions. The source and drain regions are heavily doped, and these are interconnected by using heavily doped CNTs. There is high-k dielectric such as zirconium oxide (ZrO_2) and hafnium oxide (HfO_2) forming the gate oxide above CNTs;

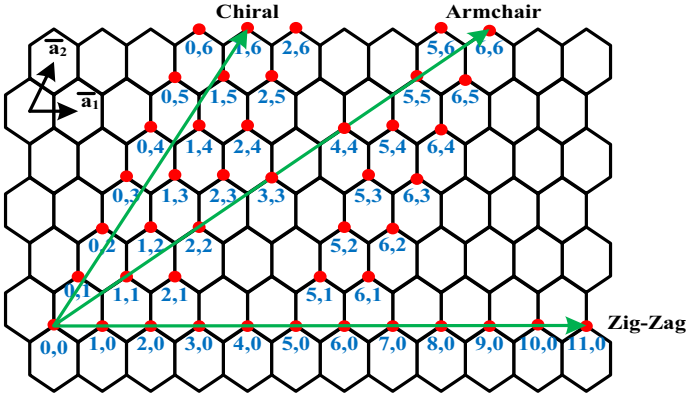

Fig. 1 Chirality vector of graphene sheet

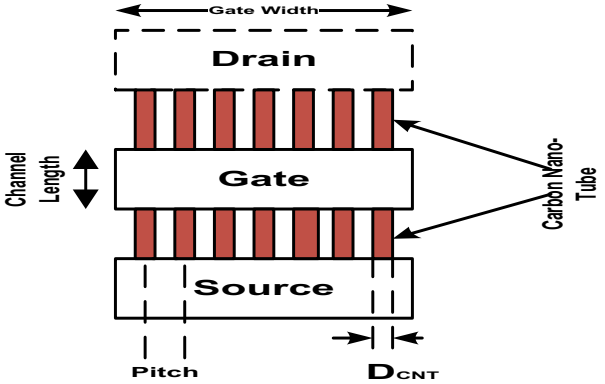

Fig. 2 Top view of CNTFET

then, metal gate connection is made over this dielectric. Substrate is fully covered by insulating thick SiO_2 layer. A single CNTFET channel is formed by multiple parallel carbon nanotubes aligned in accordance with width of gate. CNT has property that its energy gap (E_g) is inversely proportional to its diameter which allows to alter its band gap by varying the diameter of CNTs. The threshold voltage (V_{TH}) of the CNTFET can be approximated as half of the CNT band gap [9, 24] as

$$V_{TH} = \frac{E_g}{2q} = \frac{1}{\sqrt[2]{3}} \frac{aV_\pi}{qD_{CNT}} \tag{4}$$

where $V_\pi = 3.033$ eV the carbon–carbon bond energy and q is the electronic charge, and by substituting these constant values, the equations can be simplified into

$$E_g = \frac{0.872}{D_{CNT}} \quad \text{and} \quad V_{TH} = \frac{0.436}{D_{CNT}} \tag{5}$$

where D_{CNT} is in *nm* as shown in Table 1. Thus, by changing the diameter of CNT threshold voltage can be changed and energy gap of CNTs is changed and ON

Table 1 Different chirality vector with diameter of the CNTFET with variation of V_{TH} and E_g [18]

Chirality	Diameter (nm)	V_{TH} (V)	E_g (eV)
(4,0)	0.313	1.392	0.626
(7,0)	0.548	0.795	1.096
(10,0)	0.783	0.556	1.566
(13,0)	1.018	0.428	2.036
(16,0)	1.251	0.348	2.502
(19,0)	1.486	0.293	2.972
(22,0)	1.720	0.253	3.440
(25,0)	1.955	0.223	3.910

current of device is also controlled. Increasing the diameter of CNTs decreases the threshold voltage and increases the ON current because the sub-band of the channel becomes closer and more number of sub-band can be shifted toward Fermi energy level [18, 24]. The diameter dependency on the threshold voltage of CNTFET can make multi-V_{TH} implementation of CNTFET-based circuit which is the most powerful characteristics of CNTs. Once the diameter is fixed as required, and by fixing the pitch of the nanotube at optimal value, for increasing the current in the device the number of nanotubes of the channel has to be increased. But if pitch of CNTs is smaller, then package density of CNTFET is high, because this ON current reduces by concealing the gate field line by neighboring nanotubes when they come near [16]. Hence, a optimal solution for number of CNTs is found.

Another unique feature of CNTFET is that both p-channel and n-channel have approximately the same mobility, because these ON and OFF currents for an identical dimensions are the same [18, 25, 28]. This is because of electron–hole symmetricity in CNT band structure for smaller range of energy very close to Fermi energy. Since both types of CNTFET can draw similar current, n-channel and p-channel CNTFET does not require any sizing to draw the same current.

3 Adiabatic Logic Technique

A lot of circuit technologies like multi-threshold technology [7] and sub-threshold circuits [6] have been introduced to reduce the dynamic power. In this section, the principle of adiabatic logic is described to lower the peak supply current for resistance [14]. The main aim of the adiabatic switching is to reduce the energy loss during charging and discharging of the transistor.

Term 'adiabatic' comes from 'thermodynamics,' which describes a process wherein no exchange of energy with the environment takes place, so no energy loss due to dissipation occurs, whereas in semiconductor devices, the charge transfer between different nodes is the process of energy exchange. So, different techniques can be utilized to minimize this energy loss due to charge transfer. While fully adiabatic operation would be the ideal condition of a circuit operation, in practical cases partial adiabatic operation of circuit gives acceptable performance without much complexity [4, 27].

Figure 3a and b is the RC models of CMOS logic step voltage and adiabatic logic ramped step voltage, respectively. Figure 3c graph shown is the comparison of the peak current traces of the conventional CMOS logic and adiabatic logic using respective equivalent RC model. In this figure for CMOS, a large amount and sudden flow of current are observed as indicated with black line and a gradual increase of supply current peak can be seen in the same figure with red color line. Adiabatic circuit is showing low peak current than that of the CMOS peak current. As the amount of power dissipated in the circuit is a function of voltage and instant current, the overall current which flows in adiabatic circuit is less than CMOS and the power dissipation will be definitely lower compared to the CMOS logic [15].

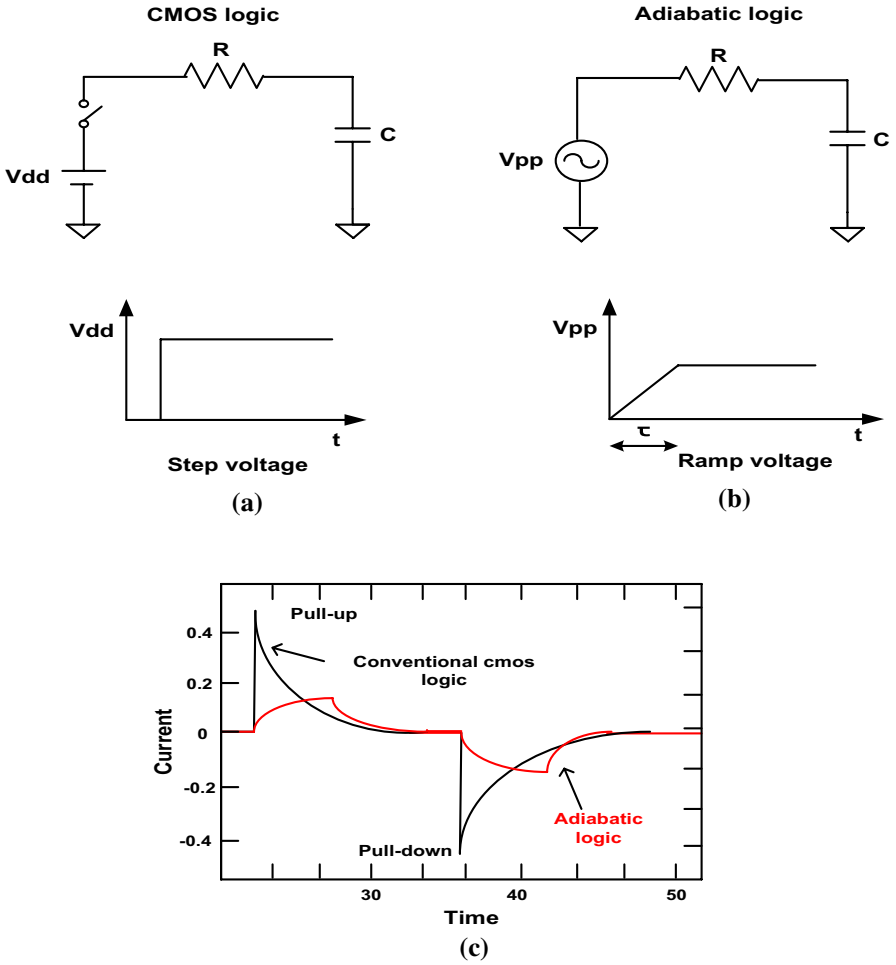

Fig. 3 Equivalent RC models of the **a** CMOS logic step voltage and **b** adiabatic logic ramped step voltage. **c** Graph of peak supply current in converting CMOS and adiabatic logic under the same parameters and condition

3.1 Adiabatic Logic Family

There are two fundamental classes of adiabatic circuits; here focus on one of the classes, namely partially energy recovery adiabatic circuit, is made. In partially adiabatic circuits, some charge is transferred to the ground. They have simple architecture and power clock system. The adiabatic loss occurs when current flows through non-ideal switch, which is directly proportional to the frequency of the power clock [3, 4, 15].

Partial/quasi-adiabatic methods are:

- Efficient charge recovery logic (ECRL)

- 2N–2N2P adiabatic logic
- Positive feedback adiabatic logic (PFAL)
- NMOS energy recovery logic (NERL)

3.2 Stages of Adiabatic Logic

Usually, in four phases adiabatic circuit operates [1, 5, 22] that is evaluate, hold, recover and wait. Quarter of period is the phase difference between adjacent phases. Adiabatic buffer structures consist of two cross-coupled P-CNTFET and two N-CNTFET. N-CNTFET determines discharging of the transistor known as evaluation logic, and P-CNTFET is used to charge the adiabatic logic. Also, time sequence of the adiabatic trapezoidal waveform known as clock depicting four phases is described below and as shown in Fig. 4 [13].

Evaluate (E) In the evaluation phase, the outputs are evaluated with respect to input, and the power clock rises toward V_{dd} from zero during this phase which is known as V_{EVF} signal, where T_{EV} is the duration of evaluation, and RC is the time constant.

$$V_{EVF} = V_C(T_1) = V_{DD} - \frac{RC}{T_{EV}} V_{DD}\left(1 - E^{\frac{T_{EV}}{RC}}\right) \tag{6}$$

Hold (H) The outputs are kept stable in the hold state for providing the input for succeeding stages, and power clock remains high during this phase.

$$V_{HF} = V_{DD} - \left(V_{DD} - V_{EVF}\right) e^{\frac{-T_H}{RC}} \tag{7}$$

where T_H is the duration of the hold phase. In the worst case, capacitor is not fully charged after the hold phase, and we introduce V_{HF} representing the capacitor voltage at T_2.

Recover (R) After that the power clock starts to fall toward zero from V_{dd}, this phase is called recovery phase. The recovery of charge from load capacitor is taking place at this phase.

$$V_{RECF} = \frac{RC}{T_{REC}} V_{DD}\left(1 - e^{\frac{-T_{REC}}{RC}}\right)\left(V_{DD} - V_{HF}\right) e^{\frac{-T_{REC}}{RC}} \tag{8}$$

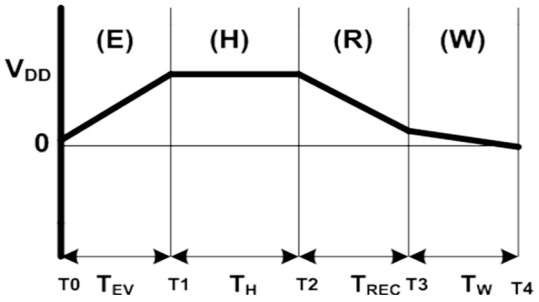

Fig. 4 Four phases of trapezoidal waveform

As the capacitor might not be fully discharged when the recovery phase is over, we introduce V_{RECF} as the capacitor voltage at T_3.

Wait (W) A wait state is also inserted because it gives the power clock symmetry and generation of power clock becomes easier, and also the input gets pre-evaluated at this phase. The waiting phase occurs between T_3 and T_4. Finally, the capacitor is fully discharged during the waiting time.

$$V_1(t) = V_{\mathrm{RECF}} e^{-\frac{t-T_3}{RC}}; T_3 \leq t \leq T_4 \tag{9}$$

The difference between the other phases is that the final capacitor voltage is zero due to the reset which is mandatory in order to insure the logic function of the gate. If the result of the function is the logic state '1,' then the capacitor voltage will follow VΦ; otherwise, it will remain at zero.

Figure 5 illustrates the *I–V* characteristics of 32-nm N-type MOS, SG mode FinFET, LP mode FinFET and CNTFET. Simulation results show that CNTFET achieves higher I_{ON} state current than MOSFET, which gives higher driving strength than MOSFET; moreover CNTFET has lower I_{OFF} than MOS and FinFET which results in better suppression of leakage current. As a result CNTFET achieves faster switching speed which results in high-frequency application.

The most commonly existing adiabatic logics are 2N2P, 2N2N2P, PFAL and DCPAL, which are shown in Fig. 6. In the 2N2N2P logic design, two more N-CNTFETs with P-CNTFET make two cross-coupled inverters to increase the stability of the outputs logic without degrading the performance of the circuit. PFAL also has a latch element formed with two cross-coupled inverters similar to 2N–2N2P [23]. The basic difference between these two is, in PFAL, the functional N block is in parallel with P-CNTFET and in 2N–2N2P functional block is situated in the lower part parallel with N-CNTFET. The advantage of PFAL among others is that it consumes less power when compared to others. As the functional blocks are in parallel with the transmission P-CNTFET, the equivalent resistance of the charging path is comparatively smaller when node capacitance is getting charged. In DCPAL a gating N-CNTFET is added in the PDN which helps in mitigation of leakage current. So, reduction of dynamic power is achieved by different existing adiabatic circuit design [1, 8, 17].

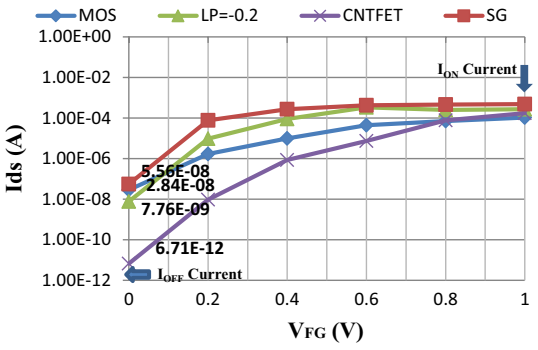

Fig. 5 *I–V* characteristics of 32-nm MOS, FinFET (SG, LP mode) and CNTFET

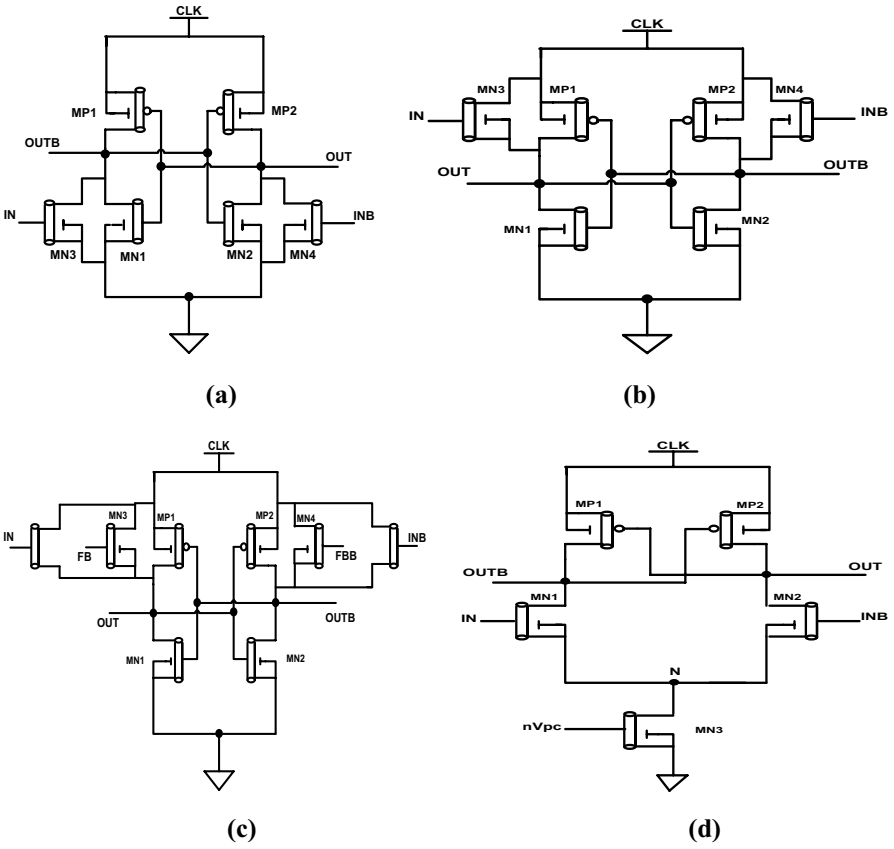

Fig. 6 Adiabatic circuit (**a**) 2N2N2P, (**b**) 2N2N2P, (**c**) PFAL, (**d**) DCPAL

Proposed circuit is influenced by PFAL circuit and hence a modification of PFAL. PFAL is a dual-rail logic family constructed using a pair of cross-coupled inverters. The voltage is supplied using clock. As shown in Fig. 6c, this logic is constructed using N-CNTFET devices which are attached between the clock and the output. Complementary inputs are given to these N-CNTFET transistors; this produces a low resistance between the power clock and the asserted output. The non-asserted path is given a high impendence. When the voltage difference between these two points is substantially high, then only the operation is performed. Using this technique, we can recover the outputs by using reverse-flowing data; thus, we can decrease the power loss due to leakage.

In an ideal adiabatic system loss E is given by Eq. (1), i.e., $E = 2(\mathrm{RC}/T)CV_{\mathrm{DD}}^2$, but shrinking devices into the sub-μm regime leads to additional loss mechanisms. With ongoing shrinking, leakage currents have more impact on the overall dissipation of static CNTFET gates. Junction leakage exists, and in state-of-the-art CNTFET processes leakage currents tunnel through the thin gate oxide.

In PFAL, during evaluation, hold and recovery, leakage currents flow from the voltage supply to ground, leading to dissipation of charge that cannot be recovered. All leakage mechanisms can be summarized in a mean current I_{leak} that leads to the energy dissipation consumption per cycle of $E_{leak} = V_{DD}\ I_{leak}(1/f)$. Leakage-related dissipation increases for lower frequencies, as leakage losses are accumulated over a longer time interval. Discharging a gate in PFAL leads to a residual voltage at the output node that is in the range of the threshold voltage of the P-CNTFET device. As long as the gate evaluates the same input in the next cycle in PFAL, this charge is dissipated when the output signal changes, as in the evaluate interval the output is then connected to ground via the N-CNTFET device in the latch. If the output state remains the same, the charge is dissipated in the wait interval, as the MP1 and MN1 transistors are turned on and connect the output to the power clock (power clock is at ground potential in the wait interval) [26]. This residual voltage dissipation given by Eq. (9) is a disadvantage and is being removed in proposed modified PFAL.

4 Proposed Work

4.1 Proposed ON–OFF-DCDB-PFAL

Proposed circuit has additional ON–OFF-DCDB-PFAL circuit below PDN in PFAL, which helps to mitigate the residual voltage dissipation described in the above section. It is named as ON–OFF-DCDB-PFAL (diode connected DC biased-positive feedback adiabatic logic).

Additional ON–OFF-DCDB-PFAL circuit has two transistors MN3 and MP3 which are introduced in conventional PFAL as shown in Fig. 7.

- Here the gate of MN3 is connected to drain of MP3.
- The source of MN3 is connected to Vdc
- The drain terminal of MN3 is connected to MN1 and MN2 simultaneously.
- Gate of MP3 is connected to source of MN1 as well as MN2.
- The source of MP3 is connected to power clock pck.
- The drain of MP3 is connected to gate of MN3 transistor.

From Fig. 7 when the residual voltage across V1 given by Eq. (9) is present, it becomes high, the gate of MP3 is high, and transistor MP3 becomes OFF. The residual charge then goes back to battery in wait state, minimizing the power dissipation to the ground. When voltage across V_1 is 0, it turns ON the MP3 transistor. The drain terminal of MP3 transistor is connected to gate terminal of MN3 transistor, which works in saturation region when pck is in wait stage as shown in Fig. 8.

When $V_{DS} > V_{GS} - V_T$ where V_T is threshold voltage then circuit is in saturation region which turns ON the MN3 transistor, and this acts like a diode when $V_{GS} \geq V_T$; then, calculation of I_{DS} is given by

$$\boldsymbol{I}_{DS} = \boldsymbol{K}\left(\boldsymbol{V}_{GS} - \boldsymbol{V}_T\right)^2 = \boldsymbol{K}\left(\boldsymbol{V}_{DS} - \boldsymbol{V}_T\right)^2 \tag{10}$$

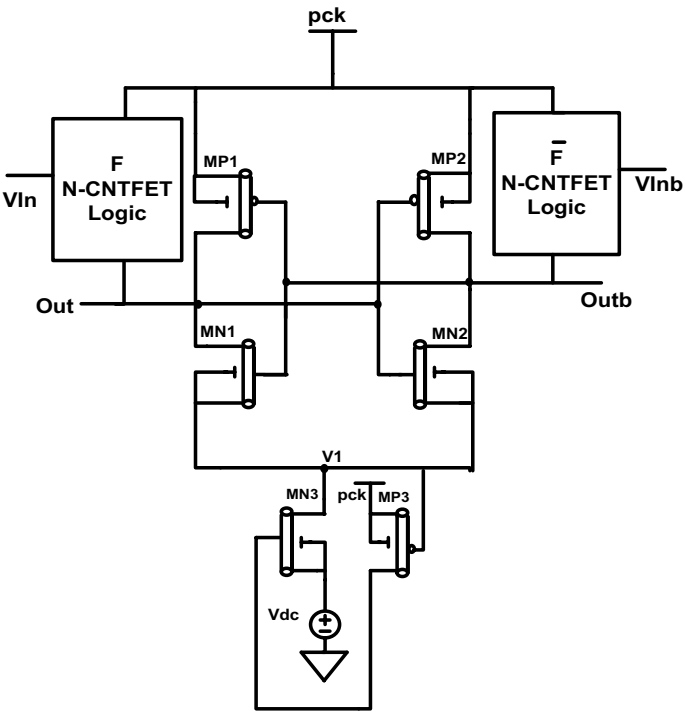

Fig. 7 Proposed ON–OFF-DCDB-PFAL circuit

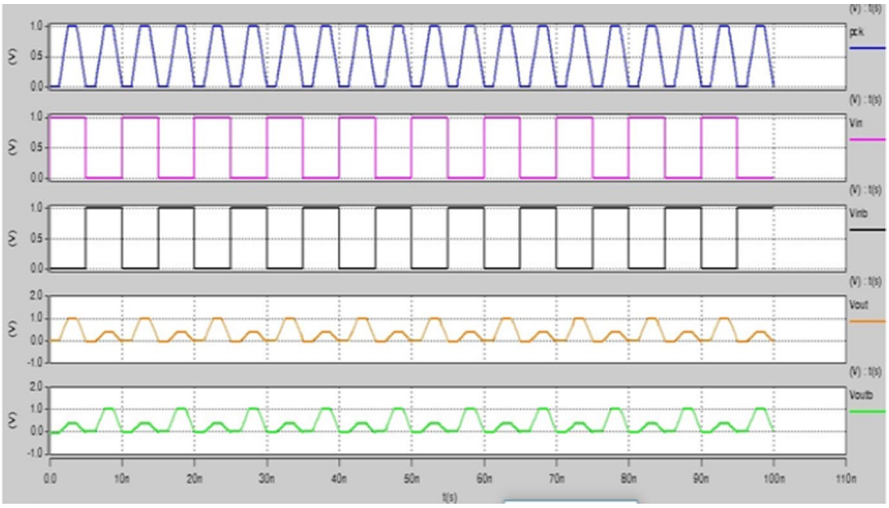

Fig. 8 Output waveform of proposed circuit

From the above equation drain current totally depends upon the gate to source voltage and threshold voltage of the transistor.

In proposed approach source terminal of MN3 is connected to positive DC voltage V_{dc} which is connected to Gnd. Thus, we see that the source voltage $V_S = V_{\mathrm{dc}}$. And so, $V_{\mathrm{DS}} = V_D - V_{\mathrm{dc}}$. The equation can be represented as.

$$\boldsymbol{I}_{\mathrm{DS}} = \boldsymbol{K}\left(\boldsymbol{V}_{\mathrm{DS}} - \boldsymbol{V}_T\right)^2 = \boldsymbol{K}\left(\left(\boldsymbol{V}_D - \boldsymbol{V}_{\mathrm{dc}}\right) - \boldsymbol{V}_T\right)^2 \tag{11}$$

Circuit consumes lower power because DC source is connected in series with MN3 transistor. The proposed logic reduces the gate to source voltage; hence, saving of leakage power takes place. Positive DC voltage source is used which is connected in between MN3 transistor and GND; the N-CNTFET transistor provides the proper stacking which does not allow to discharge the excess charge from pck to GND for saving of the power dissipation of the circuit without any logic degradation of the circuit. The proper DC voltage, i.e., V_{dc}, should be applied for proper working of the circuit; here V_{dc} applied is 0.1 V. Its value ranges from 0.1 to 0.3 V as the logic may be. Here by using adiabatic logic design different types of logic functions are implemented such as NOT/BUFFER, AND/NAND, OR/NOR, XOR/XNOR by using existing and proposed adiabatic logic circuits. The same AC power supply trapezoidal clock is used in the realization of all these circuits.

The functional blocks of NMOS (MN3) logic are connected in parallel with the PMOS (MP3) transistors of the latch forming the transmission gates similar to PFAL logic. The difference lies in the pull-down block with an NMOS diode and a DC voltage source connected between the pull-down NMOS transistors and the ground. The idea behind the use of a diode at the bottom of NMOS tree is that it will help in controlling the discharging path by decreasing the rate of discharge of internal nodes of the logic circuit. And to further incorporate the advantage of level shifting technique, a positive DC voltage source is connected between the diode and the ground. (Level shifting technique reduces the gate to source voltage at the output transistors and reduces gate current and leakage current. The circuit attains low-power operation because a low DC source is connected to the circuit in series.)

5 Results and Discussion

For further verification and demonstration of adiabatic logic, we have calculated the average power consumption of existing and proposed adiabatic design. Simulations are conducted at 32 nm by using CNTFET technology, and output capacitance is set 1fF with the variation of frequency from 10 MHz to 1 GHz, and (7,0), (22,0) is a chirality vector. CNTFET model parameters taken for simulation are given in Table 2. Here four adiabatic designs are investigated: 2N2N2P, PFAL, DCPAL and proposed ON–OFF-DCDB. In order to prove that CNTFET-based adiabatic logic has more advantageous than MOS and FinFET, we have to calculate $\mathrm{I_{ON}}$ and $\mathrm{I_{OFF}}$ currents, and there is huge reduction in $\mathrm{I_{OFF}}$ current by using CNTFET as shown in Fig. 3. Also from Fig. 9 the limiting frequency of CNTFET is more than the CMOS and FinFET (SG and LP mode) technology.

Table 2 CNTFET model parameters used in simulation [16, 18, 25]

Parameters	Values
Physical channel length (L_{ch})	32 nm
Length of doped CN source side (L_s)	32 nm
Length of doped CN drain side (L_d)	32 nm
Top of gate dielectric material constant (K_{gate}) HfO_2	16
Thickness of top gate dielectric material (t_{ox})	4 nm
Coupling capacitor (C_{sub})	40 pF/m
CNT work function	4.5 eV
Pitch P-CNTFET and N-CNTFET	5 and 10
No. of tubes	1
V_{DD}	0.9 V
The length of doped CNT drain and source-side region	32 nm
The mean free path in p+/n+- doped CNT	15 nm
V_{th}	PUN = 0.795, PDN = 0.253 V

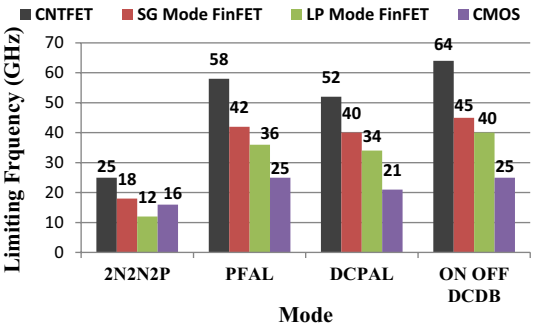

Fig. 9 Limiting frequency of adiabatic logic

5.1 Average Power

From Table 3, it is observed that proposed ON–OFF-DCDB-PFAL adiabatic logic saves average power of 94.33% in Buffer/NOT, 93.13% in NAND/AND, 93.14% in NOR/OR, 91.76% in XOR/XNOR when compared with 2N2N2P circuit. Similarly proposed circuit saves average power of 92.57% in Buffer/NOT, 90.80% in NAND/AND, 90.85% in NOR/OR, 90.17% in XOR/XNOR when compared with PFAL circuit. When compared with DCPAL proposed circuit saves average power of 62.01% in Buffer/NOT, 59.81% in NAND/AND, 59.94% in NOR/OR, 61.56% in XOR/XNOR when operating frequency of the circuit is 10 MHz.

From Table 4 it is observed that proposed ON–OFF-DCDB-PFAL adiabatic logic saves average power of 80.71% in Buffer/NOT, 86.86% in NAND/AND, 85.78% in NOR/OR, 81.41% in XOR/XNOR when compared with 2N2N2P circuit. Similarly proposed circuit saves average power of 77.86% in Buffer/NOT, 84.53% in NAND/

Table 3 Comparison of parameters, $V_{DD}=0.9$ V, PUN (7, 0) $N=1$ pitch = 5 nm, PDN (22, 0) pitch = 10 nm and $N=1$ at 10 MHz

Adiabatic design	Logic gates	AVG POWER (nW)	DELAY (ps)	PDP (aj)	EDP (E-30J)
2N2N2P	BUFFER/INVERTER	29.12	59.61	1.735	103.4
	NAND/AND	28.25	24.01	0.678	16.27
	NOR/OR	28.20	49.72	1.402	69.70
	XOR/XNOR	31.53	40.55	1.278	51.82
PFAL	BUFFER/INVERTER	22.20	4.904	0.108	0.529
	NAND/AND	21.08	4.646	0.097	0.450
	NOR/OR	21.13	9.622	0.203	1.953
	XOR/XNOR	26.41	11.21	0.296	3.318
DCPAL	BUFFER/INVERTER	4.341	13.35	0.057	0.760
	NAND/AND	4.823	23.14	0.111	2.568
	NOR/OR	4.823	25.14	0.121	3.041
	XOR/XNOR	6.755	23.88	0.161	3.844
ON–OFF-DCDB	BUFFER/INVERTER	1.649	8.578	0.014	0.120
	NAND/AND	1.938	8.784	0.017	0.149
	NOR/OR	1.932	12.39	0.023	0.284
	XOR/XNOR	2.596	14.37	0.037	0.531

(7,0), (22,0) is a chirality vector

Table 4 Comparison of parameters, $V_{DD}=0.9$ V, PUN (7, 0) $N=1$ Pitch = 5 nm, PDN (22, 0) Pitch = 10 nm and $N=1$ at 500 MHz

Adiabatic design	Logic gates	AVG POWER (nW)	DELAY (ps)	PDP (aj)	EDP (E-30J)
2N2N2P	BUFFER/INVERTER	105.7	6.338	0.066	0.418
	NAND/AND	109.5	7.364	0.806	5.935
	NOR/OR	108.2	7.953	0.860	6.839
	XOR/XNOR	142.5	7.763	1.106	8.585
PFAL	BUFFER/INVERTER	91.53	2.863	0.262	0.750
	NAND/AND	99.42	3.465	0.344	1.191
	NOR/OR	103.4	5.979	0.618	3.695
	XOR/XNOR	112.3	9.445	1.060	10.01
DCPAL	BUFFER/INVERTER	32.75	12.23	0.400	4.892
	NAND/AND	35.32	10.37	0.388	4.023
	NOR/OR	34.42	13.23	0.495	6.548
	XOR/XNOR	57.32	11.97	0.686	8.211
ON–OFF-DCDB	BUFFER/INVERTER	20.38	5.373	0.109	0.585
	NAND/AND	14.38	6.384	0.091	0.580
	NOR/OR	15.38	6.578	0.101	0.664
	XOR/XNOR	26.48	6.496	0.172	1.117

(7,0), (22,0) is a chirality vector

AND, 84.12% in NOR/OR, 76.42% in XOR/XNOR when compared with PFAL circuit. When compared with DCPAL proposed circuit saves average power of 37.77% in Buffer/NOT, 59.28% in NAND/AND, 55.31% in NOR/OR, 53.80% in XOR/XNOR when operating frequency of the circuit is 500 MHz.

Similarly from Table 5 it is observed that proposed ON–OFF-DCDB-PFAL adiabatic logic saves average power of 73.00% in Buffer/NOT, 76.82% in NAND/AND, 74.75% in NOR/OR, 72.02% in XOR/XNOR when compared with 2N2N2P circuit. Similarly proposed circuit saves average power of 64.49% in Buffer/NOT, 57.33% in NAND/AND, 58.12% in NOR/OR, 57.469% in XOR/XNOR when compared with PFAL circuit. When compared with DCPAL proposed circuit saves average power of 32.06% in Buffer/NOT, 32.83% in NAND/AND, 33.97% in NOR/OR, 31.42% in XOR/XNOR when operating frequency of the circuit is 1 GHz.

5.2 Delay

From Table 3 it is observed that proposed ON–OFF-DCDB-PFAL adiabatic logic saves delay of 85.60% in Buffer/NOT, 63.41% in NAND/AND, 75.08% in NOR/OR, 74.76% in XOR/XNOR when compared with 2N2N2P circuit. When compared with DCPAL proposed circuit saves delay of 35.74% in Buffer/NOT, 62.02% in NAND/AND, 50.71% in NOR/OR, 39.82% in XOR/XNOR when operating frequency of

Table 5 Comparison of parameters, $V_{DD} = 0.9$ V, PUN (7, 0) $N = 1$ Pitch = 5 nm, PDN (22, 0) Pitch = 10 nm and $N = 1$ at 1 GHz

Adiabatic design	Logic gates	AVG POWER (nW)	DELAY (ps)	PDP (aj)	EDP (E-30J)
2N2N2P	BUFFER/INVERTER	253.2	4.732	1.198	5.668
	NAND/AND	256.3	5.107	1.308	6.679
	NOR/OR	231.2	5.486	1.268	6.956
	XOR/XNOR	325.7	5.584	1.818	10.15
PFAL	BUFFER/INVERTER	192.5	1.902	0.366	0.696
	NAND/AND	139.2	2.102	0.292	0.613
	NOR/OR	139.4	2.541	0.354	0.899
	XOR/XNOR	215.4	5.262	1.133	5.961
DCPAL	BUFFER/INVERTER	100.6	4.073	0.409	1.665
	NAND/AND	88.42	6.730	0.595	4.004
	NOR/OR	88.40	5.684	0.502	2.853
	XOR/XNOR	132.9	5.147	0.684	3.520
ON–OFF-DCDB	BUFFER/INVERTER	68.34	8.294	0.566	4.694
	NAND/AND	59.39	5.584	0.331	1.848
	NOR/OR	58.37	4.484	0.261	1.170
	XOR/XNOR	91.13	4.313	0.393	1.695

the circuit is 10 MHz. Proposed circuit has larger delay than PFAL, but overall PDP of the proposed circuit is less.

5.3 Power Delay Product (PDP) and Energy Delay Product (EDP)

Proposed ON–OFF-DCDB-PFAL shows significant saving of PDP 99.19% in Buffer/NOT, 97.49% in NAND/AND, 98.35% in NOR/OR, 97.10% in XOR/XNOR when compared with 2N2N2P. Similarly proposed circuit saves EDP 99.88% in Buffer/NOT, 99.08% in NAND/AND, 99.59% in NOR/OR, 98.97% in XOR/XNOR when compared with 2N2N2P at 10 MHz frequency and similarly saves PDP 87.03% in Buffer/NOT, 82.47% in NAND/AND, 88.66% in NOR/OR, 87.50% in XOR/XNOR when compared with PFAL. Proposed circuit saves EDP 77.31% in Buffer/NOT, 66.83% in NAND/AND, 85.45% in NOR/OR, 83.99% in XOR/XNOR when compared with PFAL at 10 MHz frequency and similarly saves PDP 95.27% in Buffer/NOT, 70.17% in NAND/AND, 79.27% in NOR/OR, 77.01% in XOR/XNOR when compared with DCPAL. Similarly proposed circuit saves EDP 84.21% in Buffer/NOT, 94.19% in NAND/AND, 90.66% in NOR/OR, 86.18% in XOR/XNOR when compared with DCPAL at 10 MHz frequency.

5.4 Limiting Frequency

As we move toward the low-power design with the scaling of technology, there is expense of performance of the circuit. By using CNTFET technology there is tremendous reduction of power consumption in adiabatic circuit design; therefore, it is necessary to calculate overall performance of the adiabatic logic design by using CNTFET technology. In this paper, we have calculated the limiting frequency of different adiabatic circuit by using different technology (CMOS, FinFET (SG & LP mode) and CNTFET) for the measurement of performance of the circuit. Limiting frequency of the circuit can be defined by continuously increasing the frequency of the circuit until output logic of the circuit degrades, and that stopping point is known as limiting frequency.

Figure 9 shows the comparison chart of limiting frequency for four adiabatic circuits based on different technologies. From Fig. 6 it is observed that CNTFET has lower I_{OFF} current and faster switching speed than CMOS and FinFET technology; from the simulation results, it is observed that limiting frequency of CNTFET-based adiabatic logic is higher than bulk CMOS and FinFET technology. Adiabatic circuit based on CMOS has limiting frequency of 2N2N2P, PFAL, DCPAL and proposed ON–OFF-DCDB-PFAL that is 16 GHz, 25 GHz, 21 GHz and 25 GHz, respectively. Based on CNTFET, limiting frequency of the 2N2N2P, PFAL, DCPAL and proposed ON–OFF-DCDB-PFAL is 25 GHz, 58 GHz, 52 GHz and 64 GHz, respectively. In Proposed Circuit ON-OFF DCDB PFAL frequency reaches upto 64 GHz, which is highest among of ON–OFF-DCDB-PFAL reaches up to 64 GHz, which is highest among the four clock chain and other three also tremendous increase in the limiting frequency, i.e., 25 GHz for 2N2N2P, 58 GHZ for PFAL and 52 GHz for DCPAL. Similarly SG mode FinFET also has high limiting frequency which is

highest among LP mode and CMOS technology; it has 18 GHz in 2N2N2P, 42 GHz in PFAL, 40 GHz in DCPAL and 45 GHz in ON–OFF-DCDB.

From the above discussion limiting frequency of various adiabatic logic designs for low-power CNTFET device does not sacrifice the performance. It can be predicted that the improvement of leakage suppression and performance is also applicable to other CNTFET-based adiabatic circuit.

Figure 10 shows the average leakage current measurement from 1 to 100 MHz, and as we increase the frequency, the leakage current also increases. In the graph, more leakage current will flow in 2N2N2P circuit, but the proposed ON–OFF-DCDB-PFAL circuit has lower leakage current than 2N2N2P, PFAL and DCPAL in both lower and higher frequency ranges.

6 Conclusion

In this paper a novel adiabatic circuit design is presented for logic circuits based on CNTFET. Here four adiabatic circuit designs are rebuilt by using CNTFET technology, and comparison among them for average power consumption, delay, PDP and EDP with variation of frequency from 10 MHz to 1 GHz range is made. From the simulation results it is observed that CNTFET shows significant power saving on replacing CMOS and FinFET (SG and LP mode) technologies. Proposed ON–OFF-DCDB-PFAL shows significant saving of PDP 99.19% in Buffer/NOT, 97.49% in NAND/AND, 98.35% in NOR/OR, 97.10% in XOR/XNOR when compared with 2N2N2P. Similarly proposed circuit saves EDP 99.88% in Buffer/NOT, 99.08% in NAND/AND, 99.59% in NOR/OR, 98.97% in XOR/XNOR when compared with 2N2N2P at 10 MHz frequency. Besides considerable power reduction, there is performance improvement by proposed ON–OFF-DCDB-PFAL adiabatic circuit.

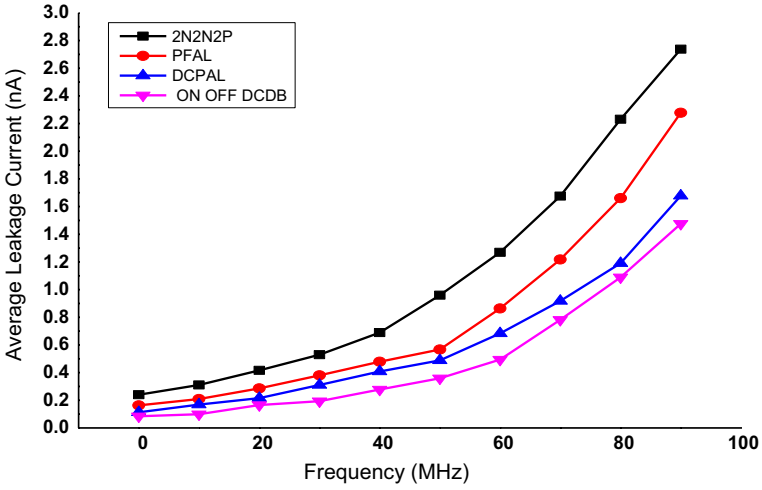

Fig. 10 Measurement of average leakage current

Hence, low-power, high-performance CNTFET-based adiabatic logic is compatible structure for the future IC design.

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