



A Novel Multiplexer-Based Quaternary Full Adder in Nanoelectronics

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Abstract

Using multi-valued logic (MVL) can reduce the chip area and connections which have direct effect on power consumption. Recently, according to the high ability of nanotechnology in designing MVL, some researchers have focused on this advanced approach. In this paper, primarily, a new design of quaternary multiplexer 4:1 with carbon nanotube field-effect transistors (CNFETs) is proposed. Afterward, quaternary successor, quaternary predecessor, and quaternary second level successor (quaternary second level predecessor) cells are, for the first time, introduced based on CNTFETs. All of the above-mentioned designs are applied to quaternary half adder and quaternary full adder circuits. To approve the designs, the performance is simulated by HSPICE simulator for 32-nm technology with the Stanford compact SPICE model for CNFETs. The results of simulation represent the improved PDP by 67.14% compared to the best current techniques in the literature. All of the proposed designs are evaluated under various operation conditions such as drive ability, fabrication tolerance, and different supply voltages, confirming the performance of proposed circuits.

Keywords Multiple valued logic · Quaternary logic · CNTFET · Quaternary adder · Quaternary multiplexer · Quaternary successor · Quaternary predecessor

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1 Introduction

Today, one common problem of binary circuits is the high number of connections in the integrated circuits (ICs) design which in turn increases the volume of chips and as well as the energy consumption of connections [3]. A common reason to consider the implementation of MVL circuits with more than two discrete signal levels is less wiring congestion compared to the binary-valued circuits. Using MVL brings the benefit of more information transmission with fewer numbers of connections which means reduction in chip area and power consumption [11]. The semiconductor industry has been faced with numerous challenges by the size reduction in semiconductor components and ICs in nanometer range. Short-channel effects and power dissipation limits are the major barriers to more size reduction. Therefore, alternative technologies for silicon transistors are being explored. One of the suitable candidates for replacing CMOS technology is the CNTFET [12]. Advantages such as ballistic transmissions, high mobility, and low power consumption for CNTFET are the main reasons of much research to apply to electronic circuits [5]. The most important advantage of CNTFET transistors is the strong relationship between the threshold voltage and the nanotube diameter [7]. This allows the multi-level circuits to be designed in a simpler and less complex manner. The CNTFETs have been applied in MVL circuits design in a lot of research during recent years.

By application of CNTFETs in MVL circuits design, ternary circuits domain such as ternary logics [1, 17], multi-digit binary-to-ternary converter [14], ternary multiplexer [18], ternary successor and predecessor [10], ternary memory cell [9], and ternary multiplier [15] have been introduced. Moreover, other designs in quaternary circuits domain naming gates and arithmetic circuits [4, 13] full adder cell [2, 17] have been presented.

In this paper, primarily, a new design of quaternary multiplexer 4:1 with CNFETs is proposed. Then, for the first time, the quaternary successor, predecessor, and second level successor (second level predecessor) cells are introduced based on CNTFETs. All above-mentioned designs are applied to QHA and QFA circuits.

The second part refers to CNTFETs and quaternary logic. The third part presents the proposed circuits and discussion about the related operation. The fourth part depicts the results of the simulation and makes a comparison with the previous works, and the fifth part concludes the paper.

2 Carbon Nanotube Field-Effect Transistor (CNFETs)

CNTs are thin tubes of graphene with one atom thickness, which have become a pipe. Among the emerging devices that use nanotechnology, CNFET has attracted more attention for its unique features such as high electric conductivity, high thermal conductivity, mechanical strength, thermal resistivity/stability, actuation properties at low voltages, and field emission [8].

Due to the reduction in the scale of semiconductor components and integrated circuits to a range of nanometers, the semiconductor industry faces a lot of challenges.

Reducing the scale causes short-channel effects and decreases gate controllability, increased leakage currents, and large parameter variations [6].

The decline in CMOS technology has been high over the past three decades, but may soon be over, due to increased short-channel effects and power dissipation constraints. Therefore, alternative technologies for silicon transistors are being explored. An option to overcome many problems in CMOS is using the carbon nanotube field-effect transistor (CNFET).

An extraordinary feature of CNFETs is that their threshold voltage is easily controlled by changing the diameter of the nanotubes under the gate. This unique feature makes them quite suitable for designing logical circuits [4]. Diameter of the CNT is calculated according to the following equation [12]:

$$V_{th} \cong \frac{E_{bg}}{2e} = \frac{\sqrt{3}aV_{\pi}}{3eD_{CNT}} \cong \frac{0.436}{D_{CNT}(\text{nm})} \quad (1)$$

where $a = 2.49 \text{ \AA}$ is the carbon to carbon atom distance, $V_{\pi} = 3.033 \text{ eV}$ is the carbon π - π bond energy in the tight bonding model, e is the unit electron charge, and D_{CNT} is the CNT diameter [7].

3 Quaternary Logic

A quaternary logic function includes four values that are indicated with '0,' '1,' '2,' and '3' and are nominally equivalent to 0, 1/3 VDD, 2/3 VDD, and VDD voltage levels, respectively. The main quaternary logic functions are QNOT, QNAND, and QNOR. Each of these functions is given in as:

$$\text{QNOT}(a) = 3 - a \quad (2)$$

$$\text{QNAND}(a.b) = \overline{\text{Min}(a.b)} = \begin{cases} 3 - a & \text{if } a \leq b \\ 3 - b & \text{otherwise} \end{cases} \quad (3)$$

$$\text{QNOR}(a.b) = \overline{\text{Max}(a.b)} = \begin{cases} 3 - a & \text{if } a \geq b \\ 3 - b & \text{otherwise} \end{cases} \quad (4)$$

Quaternary successor and predecessor are special cases of the cycle operators. The general equation for these cases is Eq. 5. Where p is the logic system (radix). Quaternary successor represents next level of input logic level ($k = 1$ in cycle operator Eq. 5), and the quaternary predecessor represents the previous level of input logic level ($k = 3$ in cycle operator Eq. 5). The second level quaternary successor or second level quaternary predecessor is in fact the quaternary predecessor and quaternary successor, which performs two-level increase or decrease in logical levels ($k = 2$ in cycle operator Eq. 5) [11]. Table 1 shows truth table of successor function, predecessor function, and second level successor function. Another unary function used in this paper is Eq. 6.

Quaternary inverters (QI) used in this paper are: negative (NQI), intermediate (IQI), standard (SQI), and positive quaternary inverter (PQI). The equation of characteristic

Table 1 The truth table for successor function, predecessor function, and second level successor function

Input X	Output				
	Successor X 1	Second level successor X 2	Predecessor X 3	X0	X1
0	1	2	3	3	0
1	2	3	0	0	3
2	3	0	1	0	0
3	0	1	2	0	0

Table 2 [5] The truth table of quaternary inverters

IN	OUT		
	NQI	IQI	PQI
0	3	3	3
1	0	3	3
2	0	0	3
3	0	0	0

of each four-level inverter is given in Eq. (16). The truth table for each one of the inverters is also given in Table 2 [4].

$$X^k = (x + k) \bmod p \tag{5}$$

$$X_k = \begin{cases} 3 & X = K \\ 0 & X \neq K \end{cases} \tag{6}$$

$$\begin{aligned} \text{NQI} &= \begin{cases} 3 & \text{if IN} = 0 \\ 0 & \text{if IN} \neq 0 \end{cases} & \text{IQI} &= \begin{cases} 3 & \text{if IN} = 0 \text{ or } 1 \\ 0 & \text{if IN} = 2 \text{ or } 3 \end{cases} \\ \text{PQI} &= \begin{cases} 3 & \text{if IN} \neq 3 \\ 0 & \text{if IN} = 3 \end{cases} & \text{SQI} &= 3 - \text{in} \end{aligned} \tag{7}$$

4 Proposed Design

In this section, the design of circuits used in the H.A and F.A circuit is discussed. The performance of each circuit is investigated. The proposed circuits include quaternary positive multiplexer 2:1, quaternary multiplexer 4:1, quaternary successor, quaternary predecessor, and quaternary second level successor. Quaternary inverters used in this paper are shown in Fig. 1.

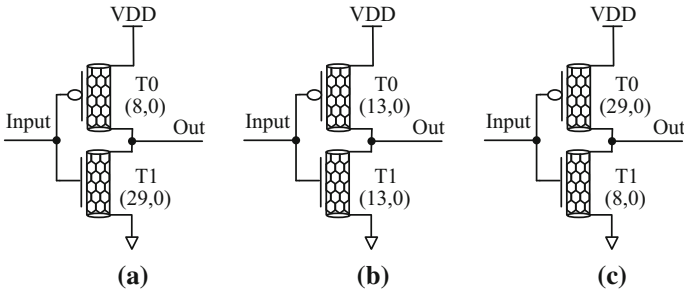


Fig. 1 Schematic design of the quaternary inverter [4]. **a** NQI, **b** IQI, and **c** PQI

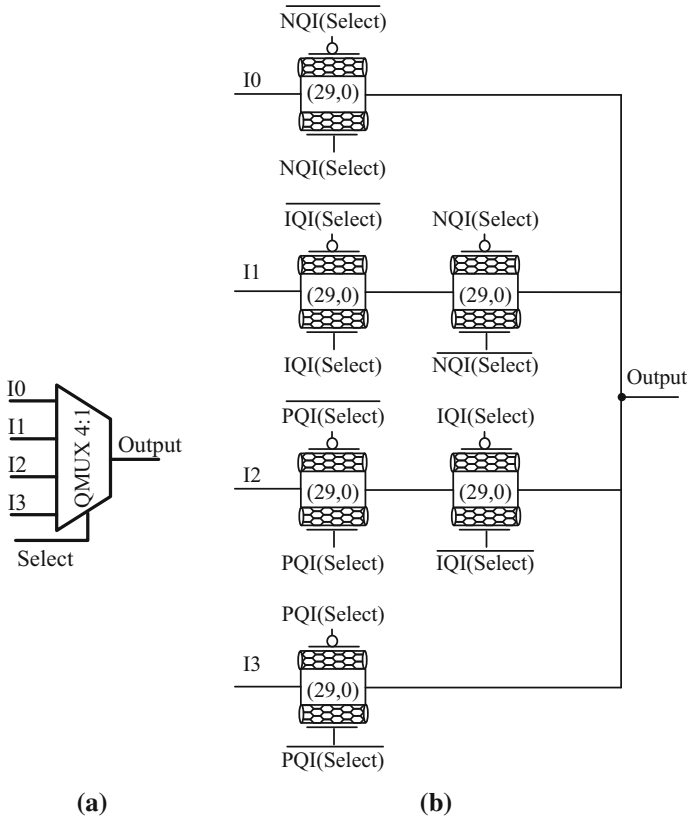


Fig. 2 **a** Symbol of the proposed quaternary multiplexer 4:1 and its **b** schematic design

4.1 Proposed Quaternary Multiplexer 4:1

Figure 2a, b shows the symbol and the proposed circuit design of quaternary multiplexer, respectively. The number of transistors used for QMUX 4:1 is 24. The designed circuit works as follows:

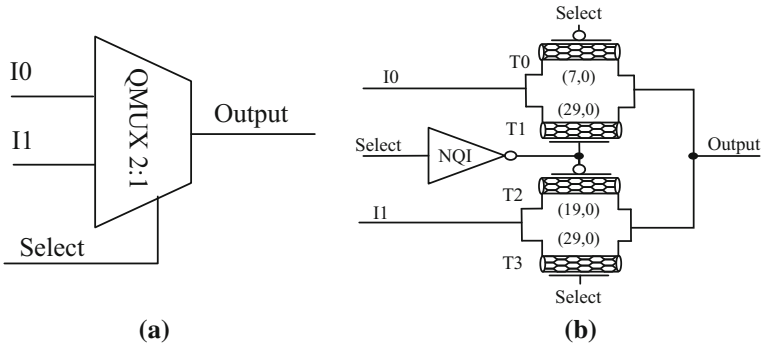


Fig. 3 a Symbol of proposed quaternary positive multiplexer 2:1 and its **b** schematic design

When select = ‘0,’ depending on the threshold voltage and transistor type, the transistors T0, T1, T2, T3, T6, and T7 are ON, and T4, T5, T8, T9, T10, and T11 are OFF, and this causes the I0 to be transferred to output.

When select = ‘1,’ depending on the threshold voltage and transistor type, the transistors T2, T3, T4, T5, T6, and T7 are ON, and T0, T1, T8, T9, T10, and T11 are OFF, and this causes the I1 to be transferred to output.

When select = ‘2,’ depending on the threshold voltage and transistor type of the transistors T4, T5, T6, T7, T8, and T9 are ON, and T0, T1, T2, T3, T10, and T11 are OFF, and this causes the I2 to be transferred to output.

When select = ‘3,’ depending on the threshold voltage and transistor type of the transistors T4, T5, T8, T9, T10, and T11 are ON, and T0, T1, T2, T3, T6, and T7 are OFF, and this causes the I3 to be transferred to output.

4.2 Proposed Quaternary Positive Multiplexer 2:1

According to Fig. 3 a, a positive quaternary multiplexer is defined as a quaternary multiplexer in which, when select = ‘0,’ I0 will transfer to output, otherwise I1 will transfer to output. Figure 3b shows the symbol and the circuit design of quaternary multiplexer, respectively. A quaternary positive multiplexer 2:1 circuit works as follows:

In the first section (select = ‘0’), the NQI output is 3 when its input is 0. Therefore, depending on the threshold voltage and the type of transistor, when select = ‘0,’ the transistors T0, T1 are ON and T2, T3 OFF and the input of the I0 is transmitted to the output. In the second section (select = ‘1’), the NQI inverted output is 0, which causes the transistors T3, T2 to be ON and T1, T0 OFF, and the input of I1 is passed to the output. The number of transistors used for a QMUX 2:1 is 6.

4.3 Proposed Quaternary Successor and Predecessor and Second Level Successor Cells

In this paper, quaternary successor, quaternary predecessor, and quaternary second level successor circuits are designed in both single-supply voltage and in three-supply

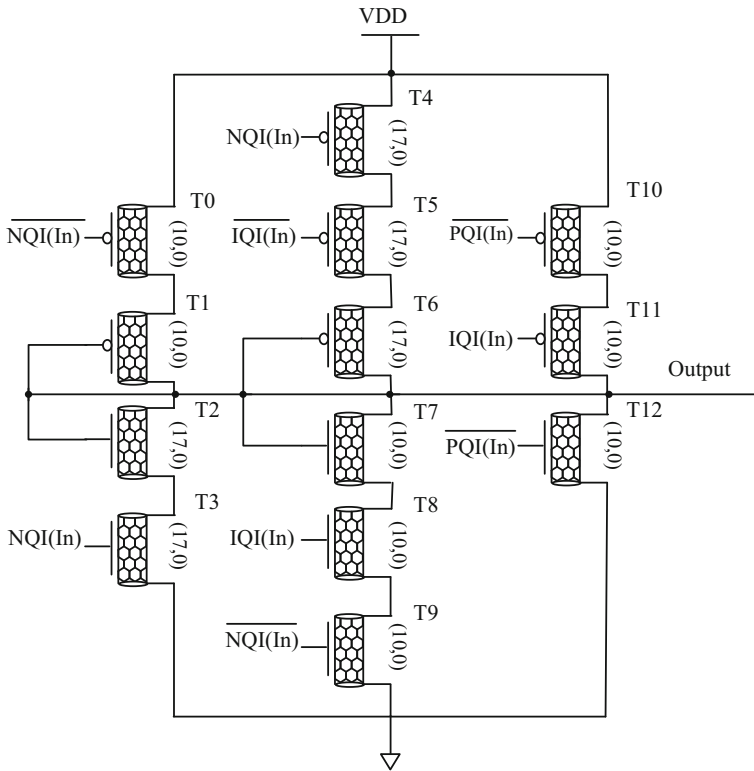


Fig. 4 The proposed single-supply voltage quaternary successor cell

voltage. Using a single voltage source reduces the number of chip connections; on the other hand, the voltage division used to generate $VDD/3$ and $2VDD/3$ increases the static power. Here, a diode connection is used to reduce the direct currents [9].

Using three voltage sources increases the metal connection; on the other hand, direct currents from the source to ground are eliminated, so the static power decreases sharply. Here, with the help of several sources, the logic 1 and 2 are directly transferred to the output.

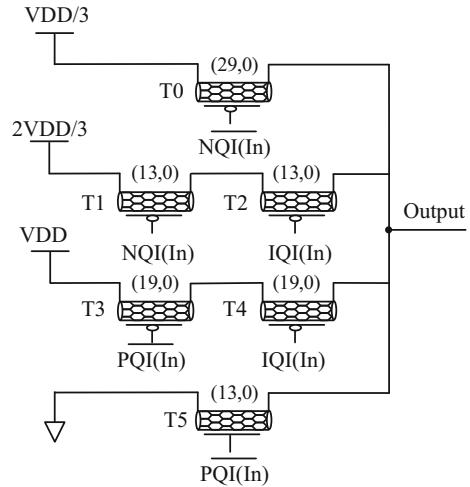
4.3.1 Proposed Single-Supply Voltage Quaternary Successor

The design of quaternary successor circuit in the single-supply voltage mode is shown in Fig. 4 which acts as seen in Table 1. The number of transistors used for single-supply voltage quaternary successor is 25. The designed circuit works as follows:

When $In = '0'$, depending on the threshold voltage and transistor type of the transistors, T5, T8, T10, T4, T6, T7, T9, T11, and T12 are OFF; the voltage division on VDD source by T0, T1, T2, and T3 transistors generates $VDD/3$. The voltage division is adjusted by CNT diameter to obtain $VDD/3$ (logic '1').

When $In = '1'$, the transistors T0, T1, T2, T3, T10, T11, and T12 are OFF; a voltage division on VDD source by T4, T5, T6, T7, T8, and T9 transistors generates

Fig. 5 The proposed quaternary three-supply voltages-based successor cell



$2VDD/3$. The voltage division is adjusted by CNT diameters of these transistors to obtain $2VDD/3$ (logic '2').

When $In = '2'$, the transistors T2, T4, T9, T10, and T11 are ON and T0, T1, T5, T6, T7, T8, and T12 are OFF, and this causes the VDD source to be transmitted to the output and generate logic '3'.

When $In = '3'$, the transistors T0, T4, T9, T11, and T12 are ON and T1, T2, T3, T5, T6, T7, T8, and T10 are OFF, and this causes the output to be connected to ground (logic '0').

4.3.2 Proposed Three-Supply Voltage Quaternary Successor

In the previous section, the proposed design is presented based on single-supply voltage. Here, however, using three-supply voltages, logic '0,' '1,' '2,' and '3' are directly transferred to output. Figure 5 shows the proposed three-supply voltage-based successor. The number of transistors used for three-supply voltage quaternary successor is 16.

When $In = '0'$, the transistors T0, T2, and T3 are ON and T1, T4, and T5 are OFF; this causes the output to be connected to the source of $VDD/3$, and in fact the logic '1' is generated at the output.

When $In = '1'$, the transistors T1, T2, and T3 are ON and T0, T4, and T5 are OFF; this causes the output to be connected to the source of $2VDD/3$ to generate logic '2'.

When $In = '2'$, the T1, T3, and T4 transistors are ON and T0, T2, and T5 are OFF; this causes the output to be connected to the source of VDD, (logic '3').

When $In = '3'$, the T1, T4, and T5 transistors are ON and T0, T2, and T3 are OFF; this causes the output to be connected to the ground (logic '0').

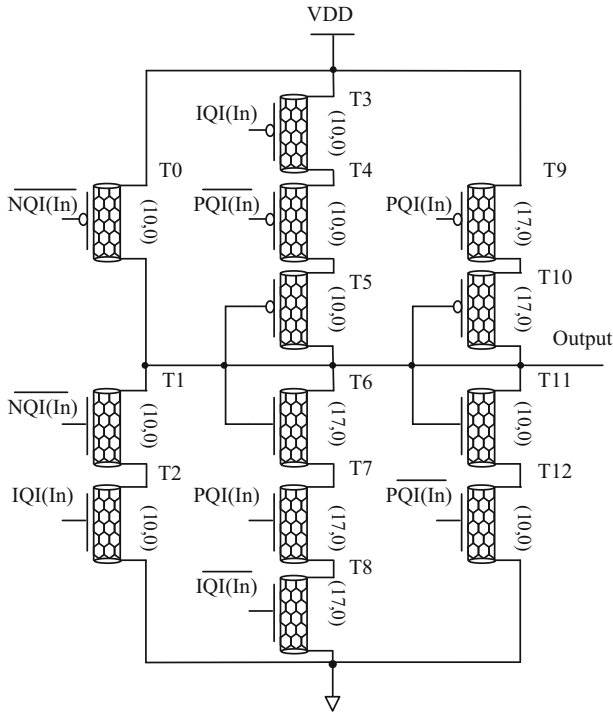


Fig. 6 The proposed single-supply voltage quaternary predecessor cell

4.3.3 Proposed Single-Supply Voltage Quaternary Predecessor

The design of the single-supply voltage quaternary predecessor is shown in Fig. 6. The number of transistors used for single-supply voltage quaternary predecessor is 25. This design works as follows, according to Table 1, the logic ‘0,’ ‘1,’ ‘2,’ and ‘3’ must be converted to logic ‘3,’ ‘0,’ ‘1,’ and ‘2,’ respectively.

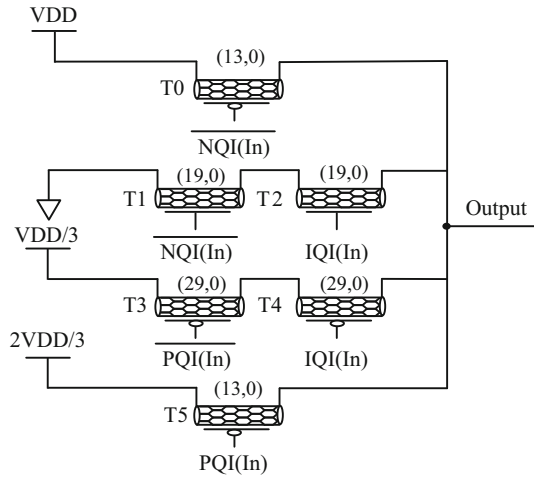
When $In = '0'$, depending on the threshold voltage and transistor type, the transistors T0, T2, T3, and T7 are ON and T1, T4, T5, T6, T8, T9, T10, T11, and T12 are OFF; this transfers the VDD source to the output and creates logic ‘3’ on the output.

When $In = '1'$, the T1, T2, T4, and T7 transistors are ON and T3, T5, T6, T8, T9, T10, T11, and T12 are OFF, and this causes the output to be connected to ground (logic ‘0’).

When $In = '2'$, the T0, T2, T9, T10, T11, and T12 transistors are OFF; the voltage division on VDD source is created by T3, T4, T5, T6, T7, and T8 transistors. The voltage division is adjusted by CNTs diameter to $VDD/3$.

When $In = '3'$, the T1, T3, T5, T6, T8, T9, T10, T11, and T12 transistors are ON and the transistors T0, T2, T4, and T7 are OFF; the voltage division from the VDD source on the T9, T10, T11, and T12 transistors generate a logic ‘2’ ($2VDD/3$) at the output.

Fig. 7 The proposed three-supply voltage quaternary predecessor cell



4.3.4 Proposed Three-Supply Voltage Quaternary Predecessor

In the previous section, the proposed design was presented based on single-supply voltage. Here, however, using three-supply voltages, logic ‘0,’ ‘1,’ ‘2,’ and ‘3’ are directly transferred to output. Figure 7 shows the proposed three-supply voltage-based predecessor. The number of transistors used for three-supply voltage quaternary predecessor is 16.

When $In = '0,'$ depending on the threshold voltage and the type of transistor, the transistors T0, T2, and T3 are ON and T1, T4, and T5 are OFF; this causes the output to be connected to the source of VDD, and in fact the logic ‘3’ is generated at the output.

When $In = '1,'$ the transistors T1, T2, and T3 are ON and T0, T4, and T5 are OFF; this causes the output to be connected to GND (logic ‘0’).

When $In = '2,'$ the T1, T3, and T4 transistors are ON and T0, T2, and T5 are OFF; this causes the output to be connected to the VDD/3 (logic ‘1’).

When $In = '3,'$ the T1, T4, and T5 transistors are ON and T0, T2, and T3 are OFF; this causes the output to be connected to the source of 2VDD/3 (logic ‘2’).

4.3.5 Proposed Single-Supply Voltage Second Level Predecessor or Second Level Successor

The design of the single-supply voltage quaternary second level successor (quaternary second level predecessor), as shown in Fig. 8, works as follows: according to Table 1, the logic ‘0,’ ‘1,’ ‘2,’ and ‘3’ must be converted to logic ‘2,’ ‘3,’ ‘0,’ and ‘1,’ respectively. The number of transistors used for single-supply voltage quaternary second level successor is 24.

When $In = '0,'$ depending on the threshold voltage and transistor type, the transistors T0, T1, T2, T3, T5, and T7 are ON and T4, T6, T8, T9, T10, and T11 are OFF; the

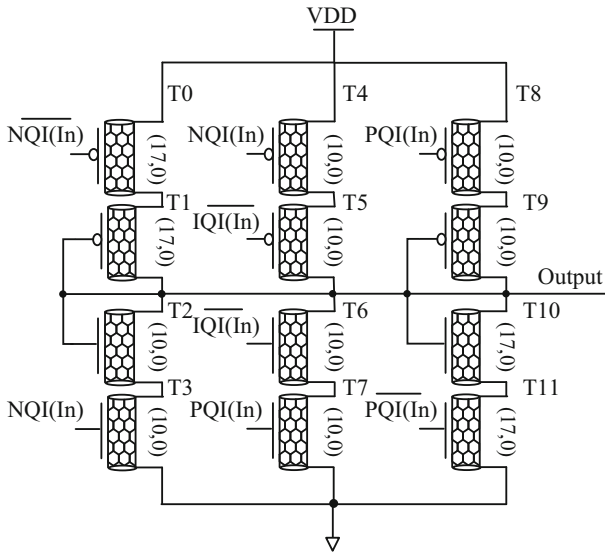


Fig. 8 The proposed three-supply voltage quaternary second level successor cell

voltage division on VDD by T0, T1, T2, and T3 transistors is adjusted by CNT diameter to generate $2VDD/3$ logical '2'.

When $In = '1'$, the transistors T4, T5, and T7 are ON and T0, T1, T2, T3, T6, T8, T9, T10, and T11 are OFF; this transfers the VDD source to the output and creates a logical '3' on the output.

When $In = '2'$, the transistors T4, T6, and T7 are ON and T0, T1, T2, T3, T5, T8, T9, T10, and T11 are OFF, and this causes the output to be connected to ground and logic '0'.

When $In = '3'$, the transistors T4, T6, T8, T9, T10, and T11 are ON and the transistors T0, T1, T2, T3, T5, and T7 are OFF; the voltage division on VDD source by T8, T9, T10, and T11 transistors generates $VDD/3$. The voltage division is adjusted by CNT diameter to $VDD/3$ (logic '1').

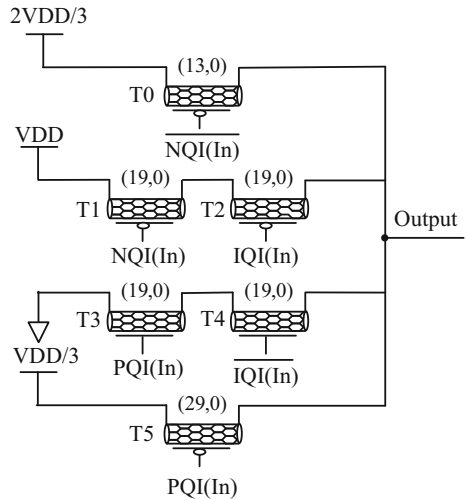
4.3.6 Proposed Three-Supply Voltage Quaternary Second Level Successor

In the previous section, the proposed design was presented based on one supply voltage. Here, using three-supply voltages, logic '0,' '1,' '2,' and '3' are directly connected to output. Figure 9 shows the proposed three-supply voltage-based second level successor. The number of transistors used for three-supply voltage quaternary second level successor is 16.

When $In = '0'$, the transistors T0, T2, and T3 are ON and T1, T4, and T5 are OFF; this causes the output to be connected to the source of $2VDD/3$ (logic '2').

When $In = '1'$, the transistors T1, T2, and T3 are ON and T0, T4, and T5 are OFF; this causes the output to be connected to the source of VDD, and in fact the logical '3' is generated at the output.

Fig. 9 The proposed three-supply voltage quaternary second level successor cell



When $In = '2,'$ the T1, T3, and T4 transistors are ON and T0, T2, and T5 are OFF; this causes the output to be connected to GND, and in fact the logic '0' is generated at the output.

When $In = '3,'$ the T1, T4, and T5 transistors are ON and T0, T2, and T3 are OFF; this causes the output to be connected to the source of $VDD/3,$ and in fact the logic '1' is generated at the output.

4.4 Proposed Quaternary Half Adder Design Based on Multiplexer

According to the truth table of quaternary half adder (QHA) presented in Table 4, it can be seen that, when $A = '0,'$ then the output is equal to B exactly, when $A = '1,'$ then the output is equal to the next logic level of B (successor (B)), when $A = '2,'$ then the output is equal to the previous logic level of B (second level successor (B)), and when $A = '3,'$ then the output is equal to the previous level of B (predecessor (B)). It could be represented by unary function Table 1 as:

$$\text{sum}_{\text{QHA}} = A_0 B^0 + A_1 B^1 + A_2 B^2 + A_3 B^3 \tag{8}$$

Also, it is worth noting that according to Table 3, when $A = '0,'$ then carry is exactly '0'. When $A = '1,'$ then carry is equal to $\overline{\text{PQI}}(B),$ when $A = '2,'$ then carry is equal to $\overline{\text{IQI}}(B),$ and when $A = '3,'$ then carry is equal to $\overline{\text{NQI}}(B),$ it could be represent by unary function as:

$$\text{carry}_{\text{QHA}} = 1 \cdot \overline{(A_0 + A_1 \overline{B^3} + A_2 (B^0 + B^1) + A_3 B^0)} \tag{9}$$

Figure 10 shows the block diagram for implementing the proposed quaternary half adder according to the above discussion.

Table 3 The truth table of QHA

SUM <i>B</i>						Carry <i>B</i>				
	<i>A</i>	0	1	2	3	<i>A</i>	0	1	2	3
0	0	1	2	3	0	0	0	0	0	0
1	1	2	3	0	1	0	0	0	0	1
2	2	3	0	1	2	0	0	1	1	1
3	3	0	1	2	3	0	1	1	1	1

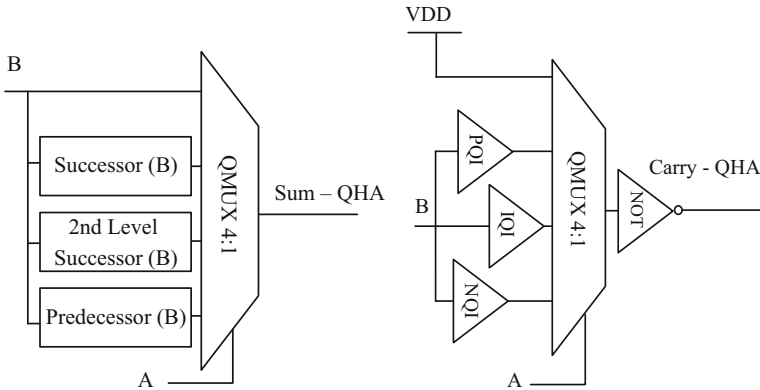


Fig. 10 Symbol of the proposed quaternary half adder

Table 4 The truth table of QFA

Cin = 0					Cin = 1						
SUM					SUM	Carry					
<i>B</i>	<i>A</i>	0	1	2	3	<i>B</i>	<i>A</i>	0	1	2	3
0	0	1	2	3	0	0	0	0	0	0	1
1	1	2	3	0	1	0	0	0	1	1	0
2	2	3	0	1	2	0	0	1	1	2	0
3	3	0	1	2	3	0	1	1	1	3	0

4.5 Proposed Quaternary Full Adder Design Based on Multiplexer

In this section, the proposed full adder is presented according to the truth table of quaternary full adder (QFA) presented in Table 4; it can be seen that if $C_{in} = '0,'$ then sum is as same as the result of the half adder sum, and if $C_{in} = '1,'$ then sum is the next logic level of Sum - QHA (successor (Sum - QHA)).

For carry output, if $C_{in} = '0,'$ the carry output in the QFA circuit is the same as the QHA circuit. If $C_{in} = '1,'$ then according to the input value *A*, one of the four PQI (*B*), IQI (*B*), NQI (*B*), and GND are transmitted to the output. The block diagram of

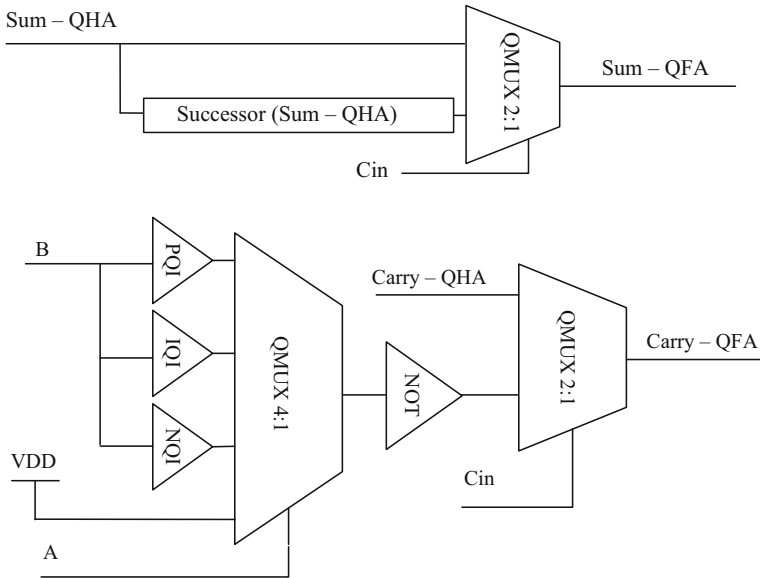


Fig. 11 Block diagram of the proposed quaternary full adder

quaternary proposed full adder is presented in Fig. 11. These could be represented by unary function as:

$$\text{sum}_{\text{QFA}} = \text{Cin}_0 \text{sum}_{\text{QHA}}^0 + \text{Cin}_1 \text{sum}_{\text{QHA}}^1 \tag{10}$$

$$\text{carry}_{\text{QFA}} = \text{Cin}_0 \text{carry}_{\text{QHA}}^0 + \text{Cin}_1 \left(\overline{A_0 B^3 + A_1 (B^0 + B^1) + A_2 B^0 + A_3} \right) \tag{11}$$

5 Simulation Results

The simulation is performed using the HSPICE for 32-nm technology with the Stanford Compact SPICE model for CNFET. All of the proposed designs are evaluated under different loads, process variation, and different supply voltage. Monte Carlo analyses have been conducted with ± 5 to $\pm 15\%$ Gaussian distribution and variation at $\pm 3\sigma$ level process variation. The temperature effect, driving ability in load, process variation, as well as power supply voltage variations for the proposed quaternary positive multiplexer 2:1, multiplexer 4:1, successor, predecessor, and second level successor are shown in Figs. 12, 13, 14, and 15, respectively. As can be seen, all proposed designs have good stability in temperature changes and fabrication tolerance and also proper driving ability.

The voltage transfer characteristics (VTC) of single-supply and three-supply voltages of the proposed quaternary successor, predecessor, and second Level successor are shown in Fig. 16. As can be seen, according to the sharp transient in voltages 0.15–0.45–0.75 V, these designs have a high noise margin. The reader may be won-

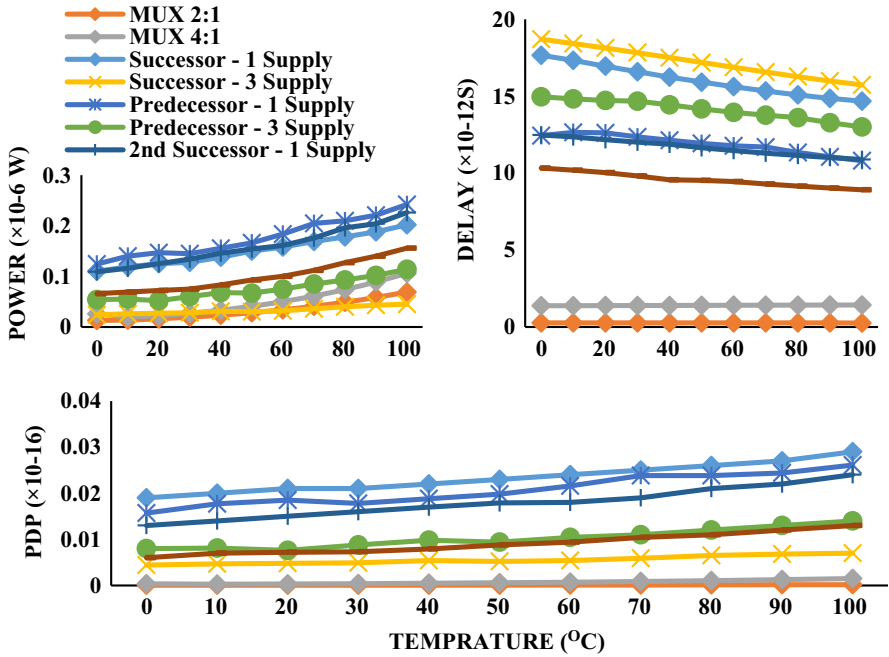


Fig. 12 Evaluation of the proposed designs for different temperatures

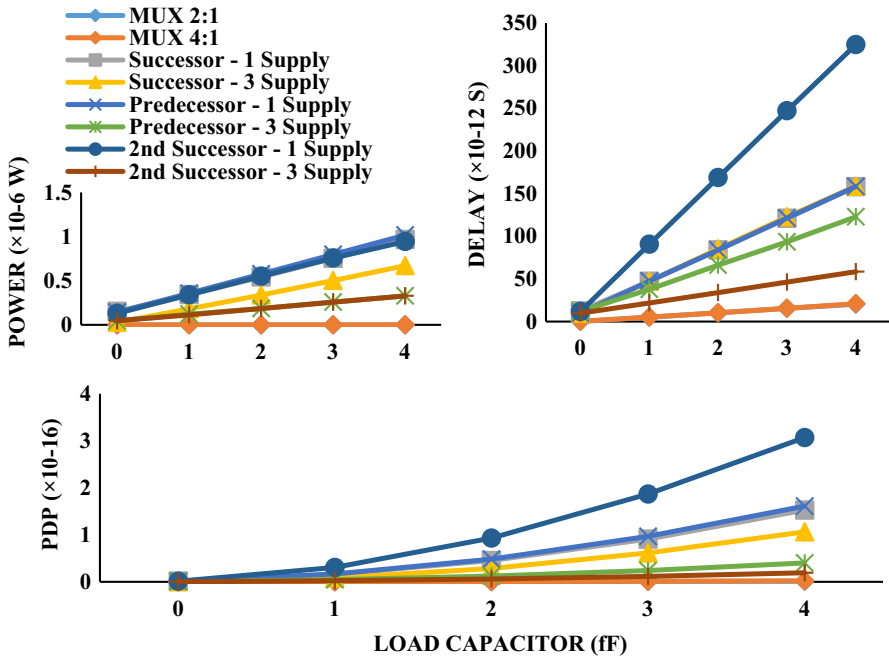


Fig. 13 Evaluation of the proposed designs for different loads

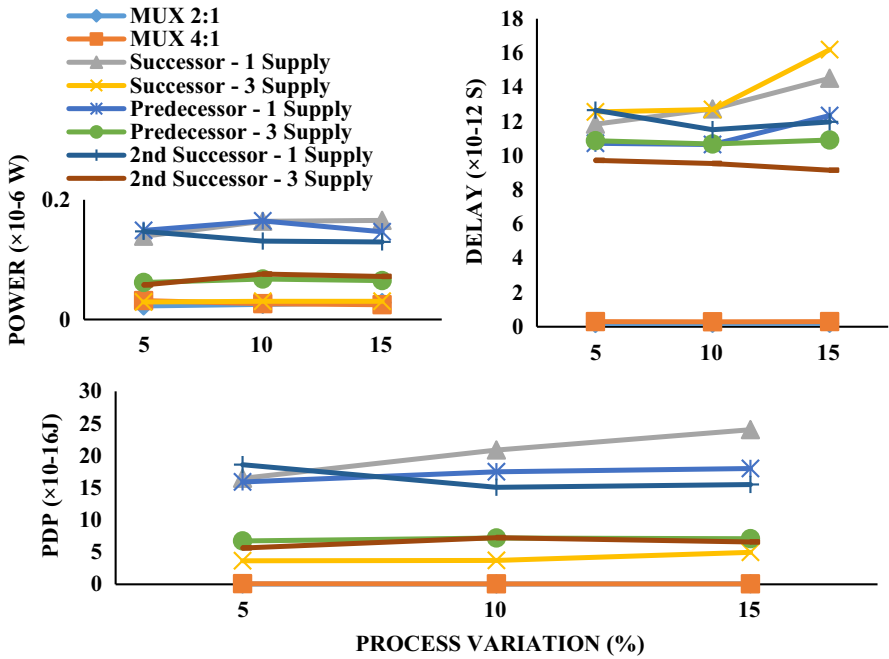


Fig. 14 Evaluation of the proposed designs versus process variation

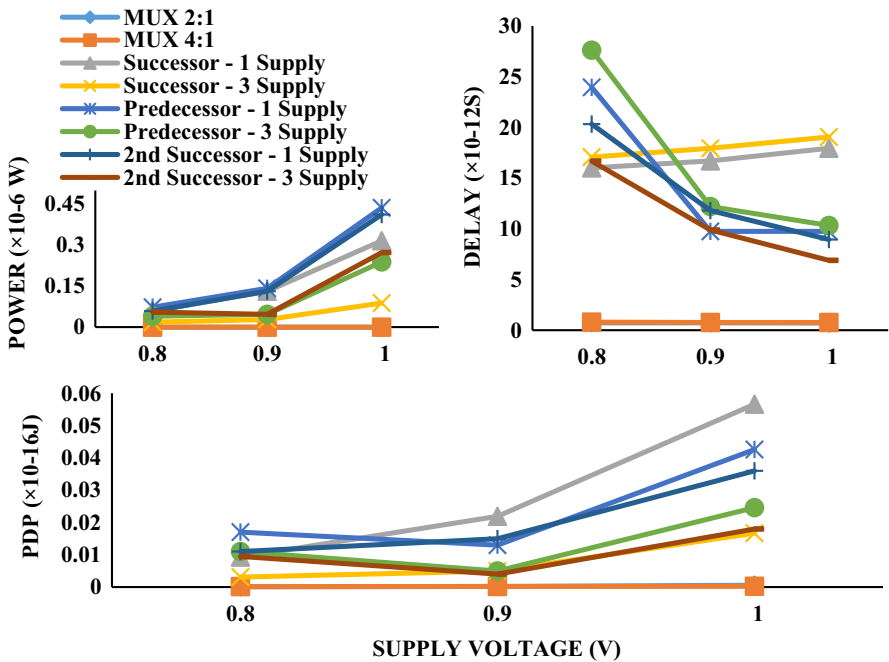


Fig. 15 Evaluation of the proposed designs for different supply voltages

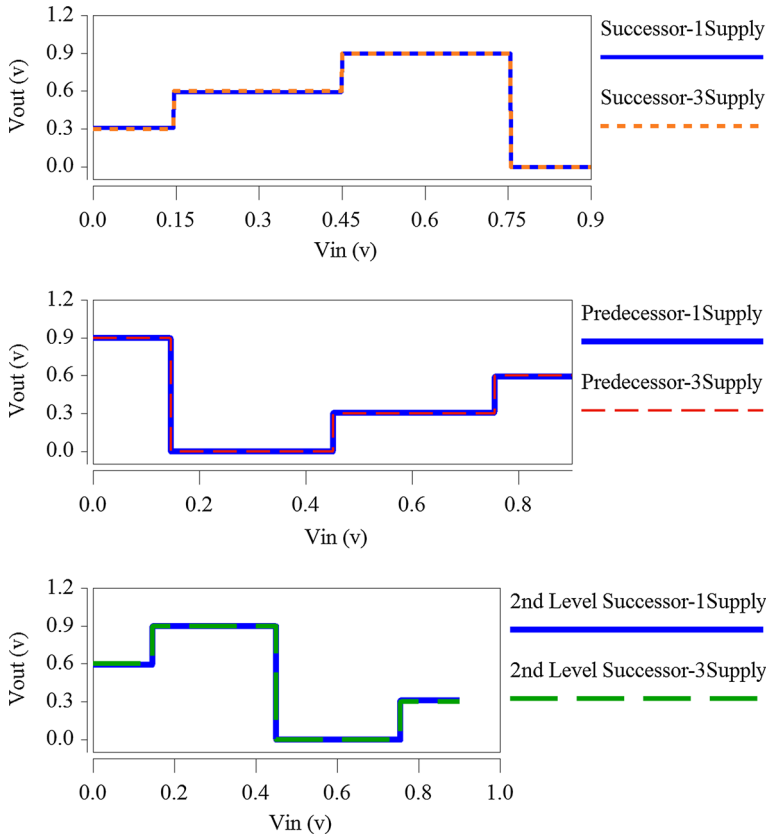


Fig. 16 VTC diagram for proposed quaternary successor, predecessor, and second Level successor

Table 5 Simulation results of the proposed quaternary multiplexer 4:1 (QMUX 4:1)

C-load	Parameter	Proposed design	[13]
0e–15f	Power (uW)	0.026	1.947
	Delay (ps)	0.309	0.595
	PDP (e-19J)	0.080	11.59
2e–15f	Power (uW)	0.066	1.986
	Delay (ps)	10.29	19.60
	PDP (e-19J)	6.791	389.4
Transistor count		24	32

dering the VTC is near to ideal VTC for maximum noise margin. But it is really possible in CNTFETs circuit design by proper adjustment of threshold voltage of each CNTFET.

For the QMUX 4:1 circuit, according to Table 5, the power is reduced in comparison with the ref [13] about 99.66%, the delay is decreased by 48.06%, and the PDP is improved by 99.30%. In this case, the number of transistors has fallen from 32 to 24.

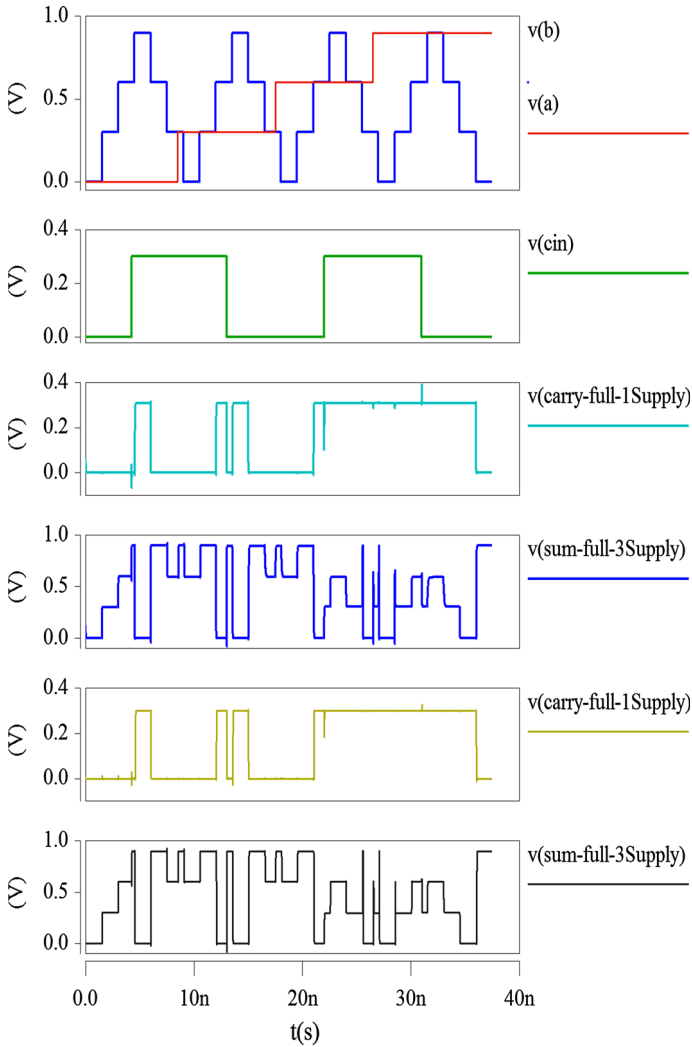


Fig. 17 Transient response of proposed QFA

Figure 17 shows the output waveforms of the proposed QFA. Table 6 shows the power, delay, and PDP of different QHA designs as can be seen for the designed QHA based on three-supply voltages, the average power is reduced by 92.03% and the delay by 46.92%. As a result, the PDP is improved by 98.95% compared to ref [13]. Note that ref [13] uses three-supply voltages. In this case, the number of transistors has decreased from 106 to 50. For single-supply voltage case, compared with the best result of ref [4], the power is reduced by 65.72%, and the delay is increased by 100.7%. As a result, the PDP is improved 31.15%. In this case, the number of transistors has dropped from 87 to 70.

Table 6 Simulation results of the proposed quaternary half adder (QHA)

C-load	Parameter	Proposed design 1	Proposed design 2	First QHA [4]	Second QHA [4]	[13]
0e–15f	Power (uW)	0.116	0.499	1.755	1.456	5.882
	Delay (ps)	10.92	38.08	49.89	18.97	20.57
	PDP (e-16J)	0.012	0.190	0.876	0.276	1.210
2e–15f	Power (uW)	0.333	0.729	1.908	1.619	5.961
	Delay (ps)	277.6	99.54	251.3	74.94	42.45
	PDP (e-16J)	0.924	0.752	4.795	1.213	2.531
Transistor count		50	70	89	87	106
Power supply count		3	1	1	1	3

Table 7 Simulation results of the proposed quaternary full adder (QFA)

C-load	Parameter	Proposed design 1	Proposed design 2	[4]	[17]	First QFA [16]	Second QFA [16]
0e–15f	Power (uW)	0.212	0.884	2.476	75.34	137.5	57.73
	Delay (ps)	46.71	43.88	71.72	112.7	114.7	17.45
	PDP (e-16J)	0.099	0.387	1.178	84.95	157.5	41.25
2e–15f	Power (uW)	0.453	1.161	2.657	102.4		
	Delay (ps)	407.2	665.0	107.9	122.3		
	PDP (e-16J)	1.844	7.721	2.871	125.3		
Transistor count		137	157	195	163	788	154
Power supply count		3	1	1	1	3	1

For the QFA circuit, according to Table 7, in three-supply voltage cases, the power is reduced in comparison with the first ref [16] about 99.84%, the delay is decreased by 59.27%, and the PDP is improved by 99.93%. In this case, the number of transistors has fallen to 137. In single-source case, compared to the best result of ref [4], the power is reduced by 64.29%, the delay is reduced by 38.82%, and the PDP also improved by 67.14%. In this case, the number of transistors has fallen from 195 to 157. For better comparison, the results are shown in Fig. 18 as bargraph.

The temperature effect, driving ability at different loads, process variation, as well as power supply voltage variations are shown in Figs. 19, 20, 21, and 22 for the proposed QHA and QFA, respectively. As can be seen, designed adders have good stability in temperature changes and fabrication tolerance and they also have proper

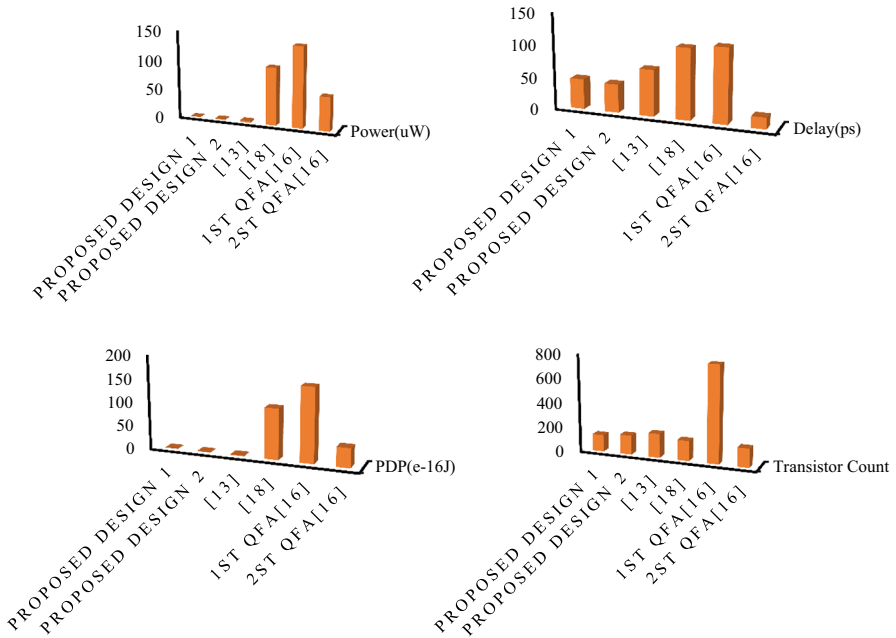


Fig. 18 a The average power in different designs of QFA. b The delay in different designs of QFA. c The PDP in different designs of QFA. d The number of transistors in different designs of QFA

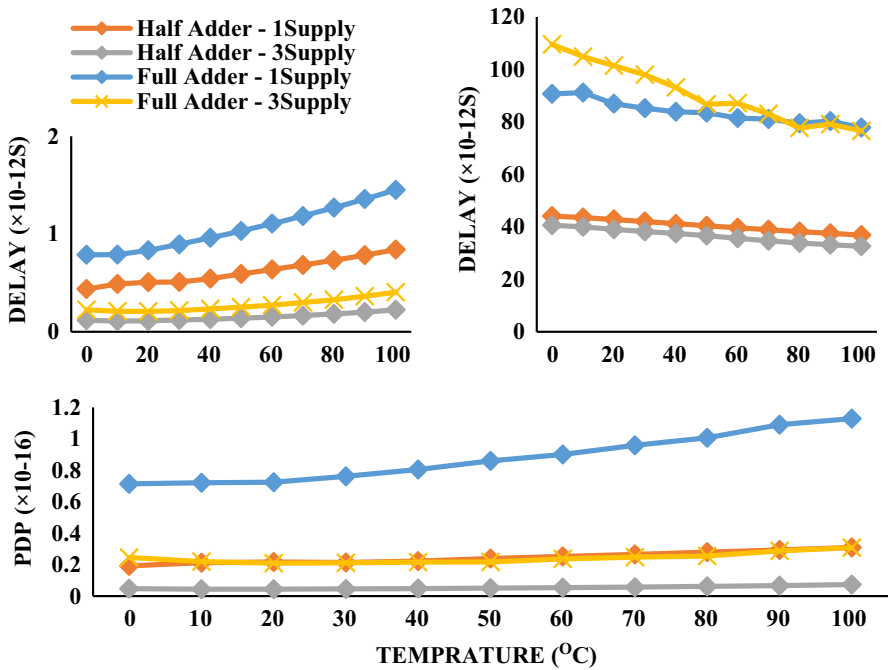


Fig. 19 Evaluation of the proposed QHA and QFA cell for different temperatures

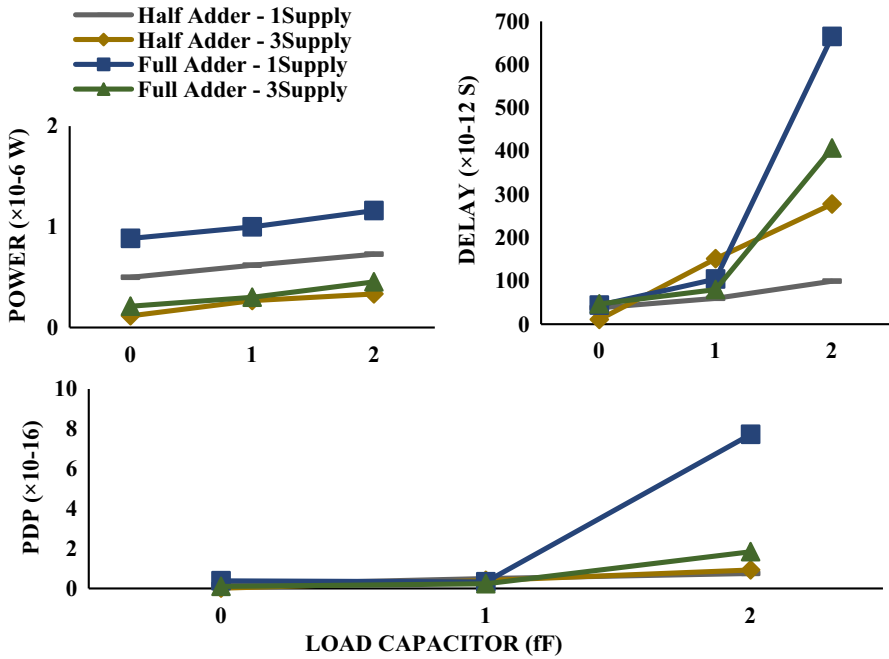


Fig. 20 Evaluation of the proposed QHA and QFA cell for different load

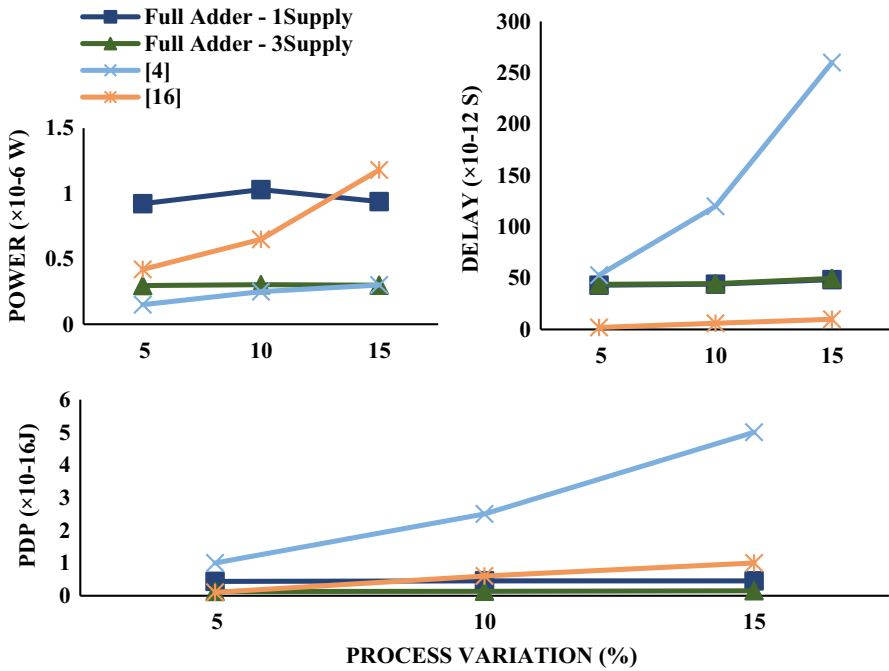


Fig. 21 Evaluation of the proposed QFA cell versus process variation

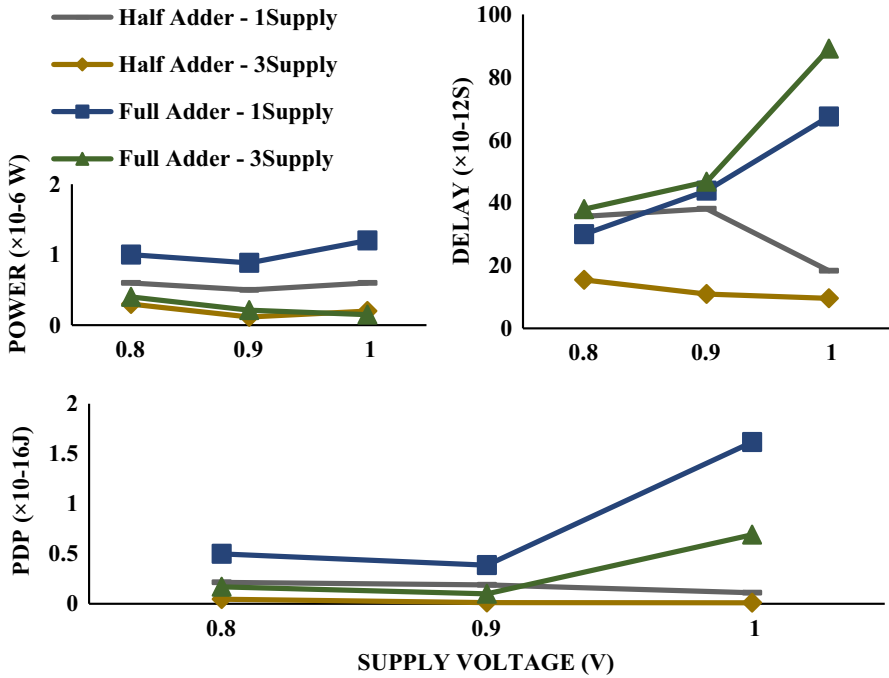


Fig. 22 Evaluation of the proposed QHA and QFA cell for different supply voltages

driving ability. According to Fig. 21, the proposed design is more stable in process variation compared to other designs.

6 Conclusion

High ability of nanotechnology has encouraged many researchers to utilize it in designing MVL circuits in the last decade.

In this paper, primarily, a novel design of quaternary multiplexer 4:1 with CNFETs is proposed. Then, quaternary successor, predecessor, and second level successor cells are, with single and three-supply voltage, introduced based on CNTFETs. All above-mentioned designs are applied to quaternary half adder and full adder circuits.

The simulation results indicate that proposed quaternary full adder in three-supply voltage case has lower PDP, about 1590 times, than the best-reported result, and also in single-supply voltage case, the PDP is reduced about 3.04 times in comparison with the best-reported single-supply voltage-based design. Moreover, the number of transistor count is reduced from 788 to 137 and 163 to 157 for three-supply voltage and single-supply voltage design, respectively.

Evaluating all of the proposed designs under different operating conditions confirms the correct performance which would lead to apply nanotechnology extensively for such designs in future. It is suggested to design quaternary multiplier based on multiplexer for future works.

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