Circuits, Systems, and Signal Processing (2019) 38:2588–2606
https://doi.org/10.1007/s00034-018-0981-7

A New Method for Design of CNFET-Based Quaternary Circuits

Akbar Doostaregan[1] · **Adib Abrishamifar**[1]

Received: 14 August 2017 / Revised: 30 October 2018 / Accepted: 30 October 2018 /
Published online: 20 November 2018

Abstract

In this paper, a new method for designing quaternary circuits in carbon nanotube field-effect transistor (CNFET) technology is proposed. Beyond many advantages of multi-valued logics (MVLs), the conversion of bits of a byte between quaternary and binary logic is easy and can be done independently. Therefore, this logic can be used effectively for wholly quaternary circuit design or beside binary logic as part of a great digital system. Thanks to particular capabilities of CNFET technology, proposed designs are implemented in this technology. These complementary symmetric gates are merely made by transistors and require only one supply voltage in addition to ground level. The proposed design for implementing standard quaternary inverter (SQI) generates three inherently binary inverters in quaternary logic as well: positive quaternary inverter (PQI), negative quaternary inverter (NQI) and symmetric quaternary inverter (SyQI). Based on the proposed design, new quaternary NAND (QNAND) and quaternary NOR (QNOR) gates are presented as well. These gates could be used as fundamental blocks for implementing complex digital circuits. QNAND and QNOR may be designed to adopt up to four inputs; however, in general applications, designs with two inputs are used. Proposed gates are simulated by means of Synopsys HSPICE tool with the standard 32 nm CNFET Stanford model, and performance parameters including maximum delay time, average power and energy consumption are extracted and compared with the simulation results of the state-of-the-art designs. The results indicate priority of proposed designs such that the delay time and energy consumption are roughly equal or less than half and one-third of other presented designs, respectively. Moreover, the voltage transfer curve (VTC) of proposed gates demonstrates the proper noise margin values from 90 mV up to 113 mV for different gates. For evaluating stability and robustness of these gates, more simulations are carried out by considering process deviations in which the proposed designs demonstrate proper performance among all in the most simulations.

✉ Akbar Doostaregan
a.doustaregan@iust.ac.ir

Extended author information available on the last page of the article

Keywords Carbon nanotube field-effect transistor (CNFET) · Multi-valued logic (MVL) · Quaternary logic · Inverter · Energy consumption

1 Introduction

Multi-valued logic (MVL) has rich and extensive history. Notwithstanding this logic was introduced in 1920, due to the domination of binary logic, development and practical applications of MVLs delayed until the late 70s [11]. In these years, pinout and interconnections density problems as well as subsequent difficulties in energy consumption increment and speed reduction became serious in binary circuits [8, 10]. In addition to considerable occupied space in integrated circuits (ICs) and complexity of cost-effective routing, the delay time along the interconnection lines was another problem. Interconnect lines in ICs could cause considerable problems for signal integrity (SI) such as disturbing noise and clock jitter in printed circuit board (PCB) layouts as still they are one of the significant resources of challenges in ICs [7, 8, 23]. These problems can be more serious when data transmission rate increases. To overcome these problems, MVL was introduced as a good candidate for substituting binary logics [11]. Furthermore, MVL circuits could reduce data traffic by transmitting more information compared with binary logic.

MVL met more success in some technologies such as integrated injected logic (I2L), emitter-coupled logic (ECL) and charge-coupled devices (CCD) [10]. However, complementary metal oxide semiconductor (CMOS) was prominent technology and MVL experienced many problems for competition with binary logic in this technology.

In the recent years, scaling down problems in CMOS technology pushed the scientists to think about the alternative technologies. Carbon nanotube field-effect transistor (CNFET) is one of the most prominent candidates for substituting CMOS technology. CNFET technology benefits from ballistic transport attributes and low power consumption under low supply voltages and very small dimensions [27]. Thanks to great advantage of CNFET technology in adjusting threshold voltage, many problems of MVL are removable in this technology. This can be done by adjusting the diameter of carbon nanotube (CNT) that is easily and accurately possible. Hence, these superiorities of CNFET to CMOS technology, as well as many advantages of MVL to binary logic encourage scientists to apply MVL in CNFET technology. Furthermore, the similarity of MOSFET to CNFET makes it possible to easily transfer previous works in CMOS to CNFET technology that met many successful results in the literature [2, 3, 28].

In spite of meeting some challenges toward substituting CNFET technology with CMOS technology, development of advanced techniques for the fabrication of devices and materials makes it possible to produce CNFETs with high quality and high yield to be used in digital ICs and designing fundamental blocks such as oscillators, flip-flops, full adders and decoders [27].

Higher radices of MVL have many similarities with digital fuzzy logic, so the achievements of MVL are used widely in this logic [2, 9]. Multi-valued circuits can be used either independently for realizing digital systems or as part of binary systems [6, 22]. In particular, powers-of-2 radices such as 4, 8, 16 and 32 are suitable for imple-

menting MVL beside binary systems and that is because each arbitrary bit of a byte in these radices can be independently converted to binary bits. For instance, a quaternary bit can be converted to two binary bits, and an eight-valued bit can be converted to three binary bits completely. This property makes these radices very suitable for use in memories which many memory cells were proposed in the literature [1, 15, 26]. However, due to the reduction of noise margin and higher circuit complexity, radices higher than 4 are used rarely in arithmetic circuits. So, quaternary logic experienced good welcome during the recent years, and many circuit design methods were introduced such that some methods for applying balanced mode numbers in this logic were presented [17, 19].

By considering these advantages of CNFET technology and quaternary logic, a new method for designing CNFET-based standard quaternary inverter (SQI) is proposed. The presented SQI is structural and complementary symmetric which includes four pass transistors and three binary inverters whose transition points are set easily by adjusting the diameter of CNTs. The SQI design can be used for designing other building blocks that can lead to a total digital circuit design. Hence, based on the proposed SQI, new quaternary NAND (QNAND) and quaternary NOR (QNOR) gates are presented. It is sufficient to replace the binary inverters by the binary NANDs and NORs, respectively.

One of the notable applications of SQIs is for implementing SRAM cells [1]. Hence, a new modified design for SQI can lead to modified SRAM memory cells which are widely used even in binary logic systems.

It is worth mentioning that the total undesired effects of interconnection lines can be reduced in quaternary logic; however, by the reason of noise margin decrement, these effects should be taken into account. This can be done by using proper PCB layout techniques in addition to accurate and simple design rules introduced in the literature [7, 8, 23].

The rest of this paper is organized as follows: First, CNFET technology is introduced briefly in Sect. 2. In Sect. 3, quaternary logic is reviewed. The proposed inverter and quaternary fundamental gates are presented in Sect. 4. In Sect. 5, designs are simulated, and finally, the last section concludes the paper.

2 A Brief Introduction to Carbon Nanotube Field-Effect Transistors

Carbon nanotubes are made by rolling graphene sheets into cylindrical structures. The rolling angle is so important, which makes the essential properties of CNT. The tube can be semiconductor or metallic depending on this angle. The angle is indicated in terms of chiral number (n_1, n_2) of chirality vector by the following equation [15]:

$$C_{\mathrm{h}} = n_1 a_1 + n_2 a_2, \tag{1}$$

where a_1 and a_2 are the unit vectors of the graphene with the magnitude equal to the carbon-to-carbon atom distance, $a \approx 2.49$ Å.

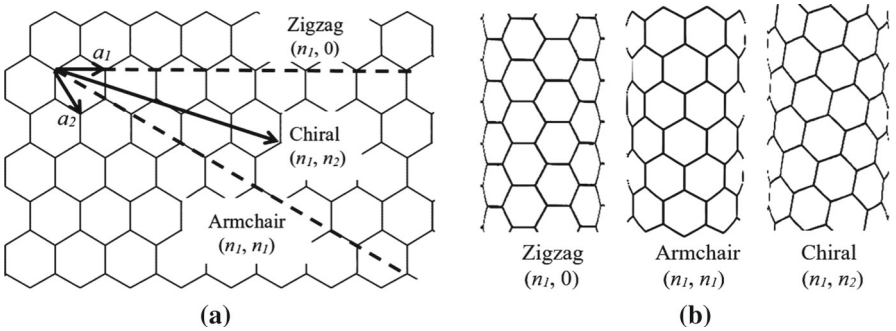

Fig. 1 **a** Graphene sheet and different types of chirality vector: zigzag ($n_1 \times n_2 = 0$), armchair ($n_1 = n_2$) and chiral (n_1, n_2). **b** Rolled graphene sheets to make different types of CNTs according to their chiral number

If $n_1 \times n_2 = 0$, the nanotube is called zigzag. If $n_1 = n_2$, the nanotube is armchair. Otherwise, it is chiral. Armchair nanotubes are metallic. Figure 1 depicts a graphene sheet with three conceivable types of chiral vector as well as corresponding CNTs.

For chiral nanotubes, if difference between n_1 and n_2 is the integer multiple of 3 ($n_1 - n_2 = 3$ k, $n_1 \times n_2 \neq 0$; $k \in \mathbb{Z}$), the tube is quasi-metallic; otherwise, it is semiconductor [12]. However, there are some exceptions because curvature effects in small diameter tubes can strongly influence electrical properties. Hence, very small diameter zigzag nanotubes, for instance (5, 0), are metallic [16]. However, the semiconducting CNTs can be used in the FETs instead of silicon as the channel.

CNTs can be single-walled carbon nanotube (SWCNT), which includes only one layer of tube, or multi-walled carbon nanotube (MWCNT) which includes multiple tubes with unit center. In electronic applications, the focus is typically on SWCNTs, and this type of CNTs is used in CNFETs.

Further to rolling angle, the diameter of sheet is important for determining the property of CNFET. Precise rolling the sheet makes it possible to define the threshold voltage of CNFET by the following equation [14]:

$$V_{\text{th}} \simeq \frac{E_{\text{g}}}{2e} \simeq \frac{0.436}{D_{\text{CNT}}}, \tag{2}$$

where E_{g} is the bandgap, e is the unit electron charge, and D_{CNT} is the diameter of the CNT which is indicated in nanometer. The diameter could be defined by following equation as well:

$$D_{\text{CNT}} = \frac{a\sqrt{n_1^2 + n_1 n_2 + n_2^2}}{\pi} \simeq 0.0783\sqrt{n_1^2 + n_1 n_2 + n_2^2} \tag{3}$$

Based on Eqs. (2) and (3), the threshold voltage of a CNFET can be obtained easily. It is obvious that for achieving smaller values for threshold voltage, the diameter and chiral numbers shall increase. In the same way, by decreasing the diameter, the threshold voltage will increase.

3 Review of Quaternary Logic

In MVL with radix r, inverter function of arbitrary variable x can be defined in multiple ways; however, a more popular definition could be found in the literature as follows [12]:

$$\bar{x} = r - 1 - x \tag{4}$$

This function can be written in quaternary logic in the form of below:

$$\mathrm{SQI}(x) = 3 - x, \tag{5}$$

where SQI is the abbreviation of Standard Quaternary Inverse function and respective circuit level gate is standard quaternary inverter. Henceforth, x is assumed to be the input signal of quaternary gate. Some other gates for inverse function have been proposed in the literature [13, 14, 18]. These gates are positive quaternary inverter (PQI), negative quaternary inverter (NQI) and symmetric quaternary inverter (SyQI). The functions of these gates could be defined by following equations [13]:

$$\mathrm{PQI}(x) = \begin{cases} 3 & \text{if } x \neq 3 \\ 0 & \text{if } x = 3 \end{cases} \tag{6}$$

$$\mathrm{NQI}(x) = \begin{cases} 0 & \text{if } x \neq 0 \\ 3 & \text{if } x = 0 \end{cases} \tag{7}$$

$$\mathrm{SyQI}(x) = \begin{cases} 3 & \text{if } x = 0, 1 \\ 0 & \text{if } x = 2, 3 \end{cases} \tag{8}$$

As can be seen, these three inverters are binary type, and their output value is just 0 and 3, so they are used for some special purposes such as producing binary signals in quaternary logic systems.

Based on the SQI definition, QNAND and QNOR operations could be defined as follows:

$$\mathrm{QNAND}(x_1, x_2, \ldots, x_n) = 3 - \min(x_1, x_2, \ldots, x_n) \tag{9}$$

$$\mathrm{QNOR}(x_1, x_2, \ldots, x_n) = 3 - \max(x_1, x_2, \ldots, x_n) \tag{10}$$

where x_1, x_2, …, and x_n are input signals of gates.

In Eqs. (9) and (10), it is assumed that QNAND and QNOR may adopt more than two input signals; however, generally they are made for two inputs.

In the same manner as for inverters, it is possible to define binary NAND and binary NOR operators in quaternary logic; however, they are less considered in the literature.

The truth table of these six functions is shown in Table 1. For SQI, there are only four conceivable states, while 16 states could be found for two input quaternary gates: QNAND and QNOR. There are only two states for output of other inverters.

Table 1 Truth table of fundamental gates in quaternary logic

x_1	x_2	SQI (x_1)	SyQI (x_1)	PQI (x_1)	NQI (x_1)	QNAND	QNOR
0	0	3	3	3	3	3	3
0	1	3	3	3	3	3	2
0	2	3	3	3	3	3	1
0	3	3	3	3	3	3	0
1	0	2	3	3	0	3	2
1	1	2	3	3	0	2	2
1	2	2	3	3	0	2	1
1	3	2	3	3	0	2	0
2	0	1	0	3	0	3	1
2	1	1	0	3	0	2	1
2	2	1	0	3	0	1	1
2	3	1	0	3	0	1	0
3	0	0	0	0	0	3	0
3	1	0	0	0	0	2	0
3	2	0	0	0	0	1	0
3	3	0	0	0	0	0	0

4 Proposed Design of Standard Quaternary Inverter (SQI)

In this section, the new design for implementing quaternary gates in voltage mode is presented. Figure 2a shows the proposed SQI. This complementary symmetric design is made by 10 CNFETs. Three pair of CNFETs constitutes three binary NOTs. These binary NOTs are in fact PQI, SyQI and NQI gates. The proposed SQI is fully made by CNFETs and requires only one supply voltage; Vdd and ground voltage level; 0 V. Hence, the output voltages of binary NOTs could be 0 V or Vdd that are equivalent to 0 and 3 quaternary logic levels, respectively. In this design, Tn2 and Tp2 have only one tube, while other CNFETs have three tubes. The transition region of NOT1, NOT2 and NOT3 are adjusted such that they make NQI, SyQI and PQI gates, respectively. Therefore, the transition point of NOT1 is adjusted on approximately mean voltage of 0 and 1/3Vdd which is 1/6Vdd. This could be achieved by choosing proper values for chiral numbers of CNFETs. In the same manner, the transition points of NOT2 and NOT3 are adjusted close to 1/2Vdd and 5/6Vdd, respectively. So, when the input is 0, the outputs of all NOTs become 3. Therefore, Tp1 and Tp2 become "on," and the output of SQI will be 3. In the same manner, if the input is 3, the output of all NOTs changes to 0; hence, Tn1 and Tn2 become "on" and the output of SQI will be 0. When the input becomes 1, the output of NOT1 and NOT2 will be 3 and the output of NOT3 will be 0. In this condition, Tn1 and Tn2 become parallel, and the output of SQI will be achieved from voltage division among them and Tp2. Therefore, output will be 2. In the same manner, when the input becomes 2, output of NOT1 will be 3 and output of NOT2 and NOT3 will be 0. Hence, Tp1 and Tp2 become parallel, and output of SQI

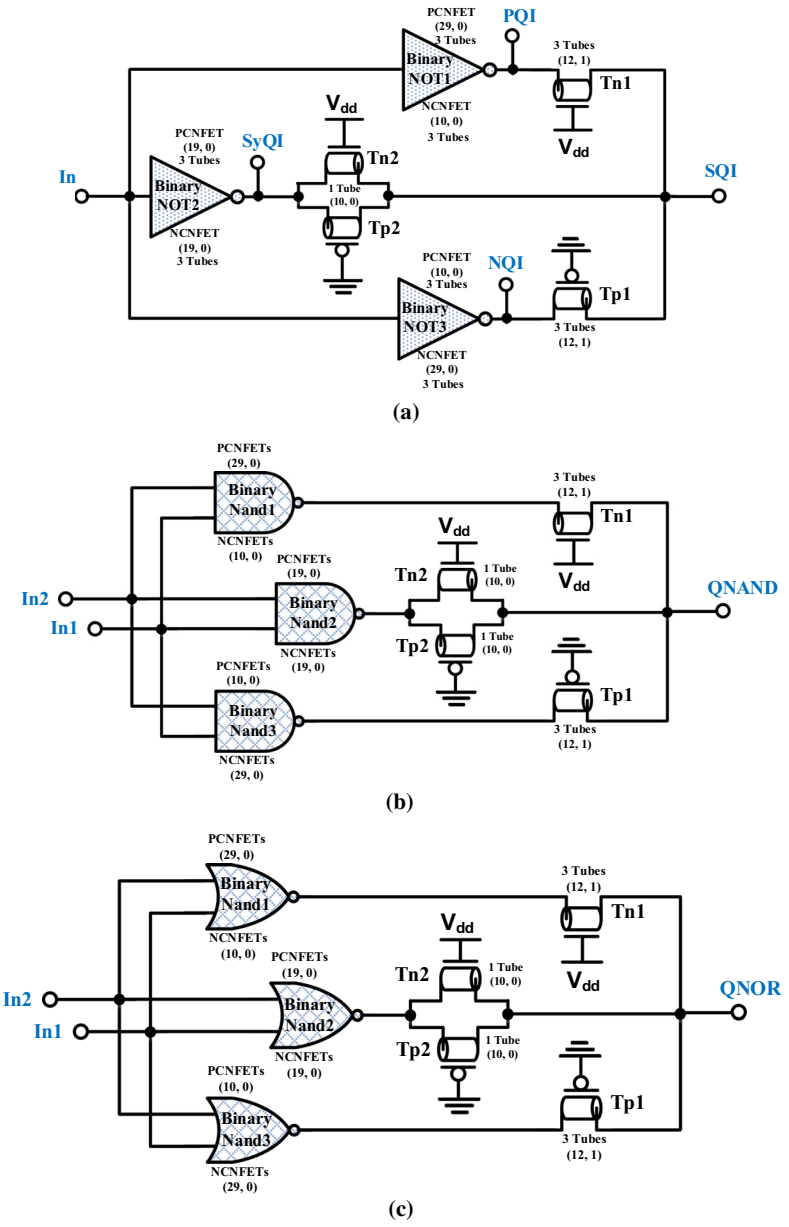

Fig. 2 Proposed quaternary designs **a** SQI, **b** QNAND, **c** QNOR

will be the achieved from voltage dividing among them and Tn2. Therefore, output will be 1.

One of the great advantages of this design is generating all four quaternary inverse function outputs at the same time as shown in Fig. 2a. Figure 3a demonstrates the

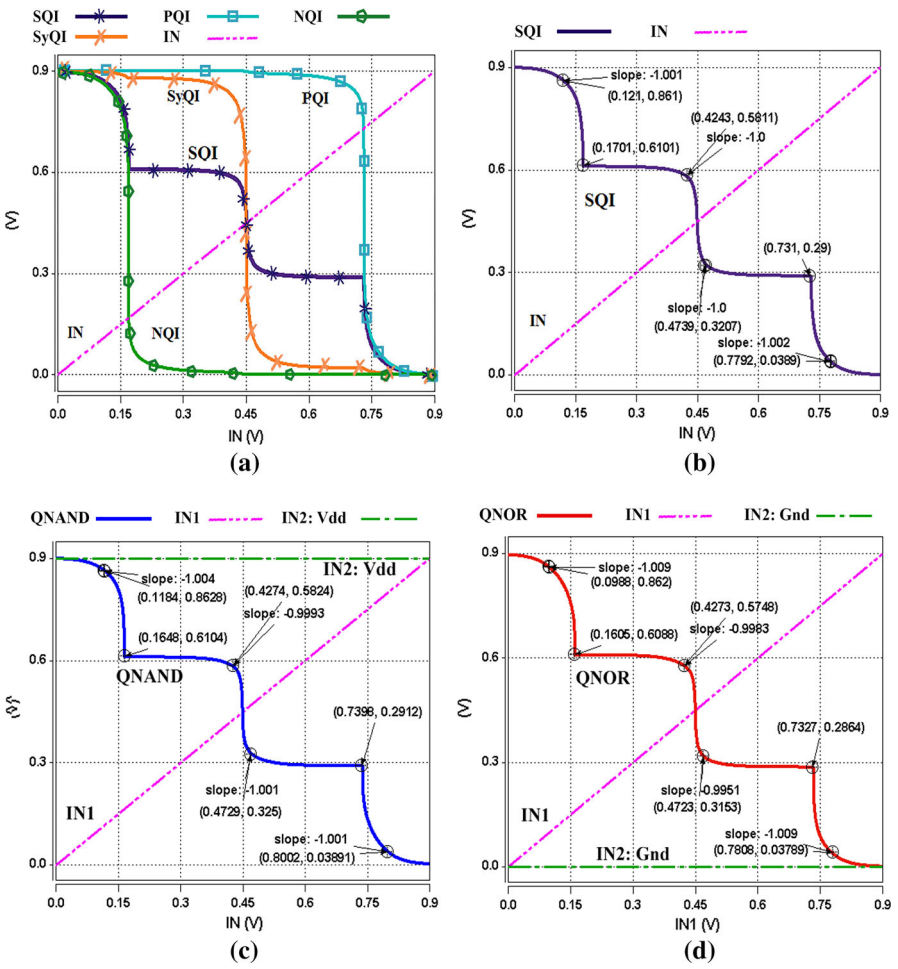

Fig. 3 VTC of proposed design **a** SQI, SyQI, PQI, NQI and VTC with noise margin measurements for **b** SQI, **c** QNAND (IN1, Vdd), **d** QNOR (IN1, Gnd)

voltage transfer characteristics (VTC) of proposed design for inverter definitions of (5) to (8). The VTCs have proper steep in transition regions as well as desirable voltage levels specifically for SQI. Therefore, the correct functionality of proposed design is proven.

Based on the proposed SQI, it is possible to make QNAND and QNOR gates. To achieve this aim, it is enough to replace binary NOTs with suitable binary NAND and NOR gates, respectively. The chiral number of *P*-type CNFETs in NAND and NOR gates shall be the same as *P*-type CNFET of respective NOT, and the chiral number of *N*-type CNFETs in binary NAND and NOR gates shall be the same as *N*-type CNFET of respective binary NOT. The proposed design for QNAND and QNOR is shown in Fig. 2b and c, respectively. The operational principle of these gates is simple and

Table 2 Output values of binary gates in QNOR and QNAND gates

x_1	x_2	BNand1	BNand2	BNand3	QNAND	BNor1	BNor2	BNor3	QNOR
0	0	3	3	3	**3**	3	3	3	**3**
0	1	3	3	3	**3**	3	3	0	**2**
0	2	3	3	3	**3**	3	0	0	**1**
0	3	3	3	3	**3**	0	0	0	**0**
1	0	3	3	3	**3**	3	3	0	**2**
1	1	3	3	0	**2**	3	3	0	**2**
1	2	3	3	0	**2**	3	0	0	**1**
1	3	3	3	0	**2**	0	0	0	**0**
2	0	3	3	3	**3**	3	0	0	**1**
2	1	3	3	0	**2**	3	0	0	**1**
2	2	3	0	0	**1**	3	0	0	**1**
2	3	3	0	0	**1**	0	0	0	**0**
3	0	3	3	3	**3**	0	0	0	**0**
3	1	3	3	0	**2**	0	0	0	**0**
3	2	3	0	0	**1**	0	0	0	**0**
3	3	0	0	0	**0**	0	0	0	**0**

based on the SQI gate. Output values of binary gates in QNAND and QNOR gates for different values of inputs are demonstrated in Table 2.

As shown in Table 2, binary gates may adopt logic values 0 or 3 in quaternary logic. The output values of these NOTs are adjusted such that the desired outputs of two-input quaternary gates are produced.

In comparison with SQI, these gates have six more CNFETs. As mentioned in Sect. 3, it is possible to make QNAND and QNOR gates with more than two inputs. Hence, for increasing input signals by one to make three-input gate, six more CNFETs are required for replacing two-input binary gates with three-input ones in Fig. 2b and c.

For evaluating the functionality of proposed QNAND and QNOR, 'In1' of QNAND is connected to Vdd and 'In1' of QNOR is grounded. Therefore, the VTC of these gates can be extracted as plotted in Fig. 3b and c.

Similar to VTC of SQI, the transfer characteristics of QNAND and QNOR have good steeps and voltage levels that prove the fine functionality of proposed designs.

In order to verify the proper functionality of designs, the values of noise margin for proposed designs are measured. Table 3 shows the noise margin of designed gates according to Fig. 3b–d. As shown, the average values are close to 100 mV for all three gates; however, the values for SQI are fairly better than QNOR and QNAND. Noise margin values in Table 3 are apt and proper for confidently generating desired output signals of quaternary logic.

Table 3 Noise margin values of proposed gates

Proposed gates	NML $0 \leftrightarrow 1$ (mV)	NMH $0 \leftrightarrow 1$ (mV)	NML $1 \leftrightarrow 2$ (mV)	NMH $1 \leftrightarrow 2$ (mV)	NML $2 \leftrightarrow 3$ (mV)	NMH $2 \leftrightarrow 3$ (mV)	Average (mV)
SQI	92	111	104	107	111	91	103
QNAND	101	91	102	110	108	98	101
QNOR	95	106	112	103	90	102	101

5 Simulation, Evaluation and Comparison

Although the VTC of proposed designs demonstrated appropriate functionality of these gates; however, for deep evaluation, it is necessary to extract their performance parameters. This purpose is obtained in this section by simulating designs of Fig. 2a and c. Moreover, the simulation is done for two state-of-the-art designs in [18, 13], and then, the results will be compared with each other. These two designs, which outperform other former designs, were proposed based on the designs of [6, 24], respectively.

The design of [6] was introduced in CMOS technology by means of transistors and capacitors; however, in [18], the CMOS transistors were substituted by CNFETs. Moreover, capacitors were implemented by source–drain–substrate-connected CNFETs to eliminate non-CNFET elements.

Pseudo-NCNFET design as presented in [13] substituted the resistors in design of [24] by gate-grounded *P*-type CNFETs to make a fully transistor-based design. For producing desired outputs of SQI, the threshold voltages are adjusted by proper choosing of the chirality and the number of substituted CNTs [13]. Pseudo-NCNFET SQI consists of three NCNFETs and three PCNFETs. As reported in [13], the design shows competitive results and in some cases better performances compared with other state of the arts. Although, the design has low count of elements, the design is not symmetric which causes the VTC to be asymmetric and decrement of the noise margin.

In simulations, three evaluating parameters are extracted: *maximum delay time, average power consumption* and *energy consumption* which is indicated in term of *power–delay product (pdp)*. Maximum delay time is an essential parameter to determine the speed of circuits. This parameter is the time interval between 50% of change at the input signal and 50% of the change at the corresponding output voltage. This time is measured for all possible transitions, and maximum value is recorded. Power and energy consumption are two important parameters particularly in recent years, after rapid development of portable digital devices [20]. It worth noting that the power and energy consumption are dependent on the input pattern; however, the patterns are chosen to establish justified conditions for all designs according to transitions.

Simulations are carried out by means of Synopsys HSPICE tool. The timestep in transient analysis is chosen such small that its effect on output response parameters becomes less than 0.1%.

Table 4 Characteristics of the used CNFET model

Parameter	Brief description	Value
L_{ch}	Physical channel length	32 nm
L_{dd}	The length of doped CNT drain-side extension region	32 nm
L_{ss}	The length of doped CNT source-side extension region	32 nm
L_{geff}	The Scattering mean free path in the intrinsic CNT channel and S/D regions	100 nm
K_{ox}	The dielectric constant of high-k top gate dielectric material (HfO_2)	16
K_{sub}	The dielectric constant of substrate (SiO_2)	4
T_{ox}	The thickness of high-k top gate dielectric material	4 nm
C_{sub}	The coupling capacitance between the channel region and the substrate (SiO_2)	40 aF/μm
Efi	The Fermi level of the doped S/D tube	6 eV

Applied CNFET model is Stanford University CNFET circuit model for the channel length Lch = 32 nm. Parameters of this model are tabulated in Table 4 [4, 5].

This model is a SPICE-compatible compact model, which describes enhancement-mode, unipolar MOSFETs with SWCNTs as channels [4]. Each device may have one or more CNTs with arbitrary chirality.

The model is based on a quasi-ballistic transport picture and includes an accurate description of the capacitor network in a CNFET. In addition, the effects of channel length scaling can be modeled down to 20 nm.

The model non-idealities are the quantum confinement effects on both circumferential and axial directions, the acoustical/optical phonon scattering in the channel region and the screening effect by the parallel CNTs for CNFET with multiple CNTs. These effects are mainly indicated in terms of the gate-to-gate and gate-to-contact-plug capacitances, the parasitic capacitance between the gate and the source/drain formed by multiple 1D nanotubes the charge screening among the adjacent nanotubes, the access resistance of the source/drain extension regions, the Schottky-barrier resistance at the metal–nanotube contact interfaces and the band-to-band leakage current.

The complete dynamic gate-capacitance network makes the model suitable for both analog and digital applications with better predictions of the dynamic performance and transient response [4].

Operating temperature is 25 °C and supply voltage is 0.9 V. So, logic levels 0, 1, 2 and 3 are equivalent to 0 V, 0.3 V, 0.6 V and 0.9 V, respectively.

To evaluate driving ability of designs, a 1 fF load capacitor is used in the output of circuits in all simulations.

The simulating condition is similar for all three designs except that in respective references other specific conditions have been mentioned.

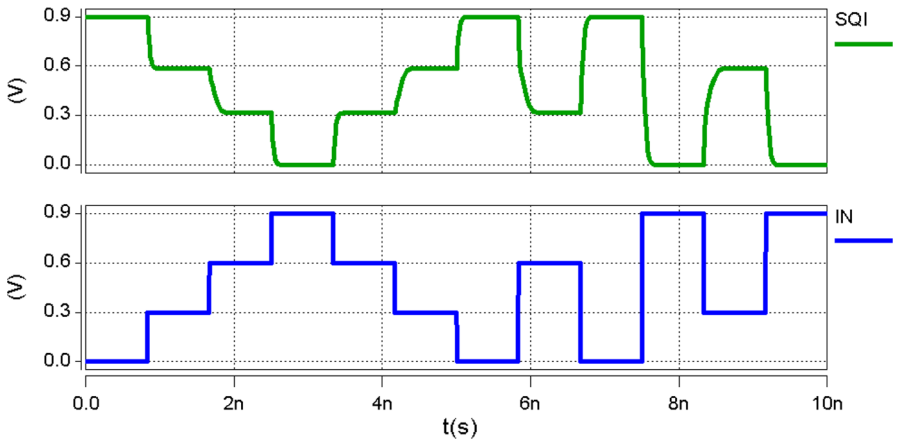

Fig. 4 Input voltage pattern and output response of the proposed SQI

Table 5 Simulation results of SQIs with 1 fF capacitance load

Simulated design	Maximum delay time (in ps)	Average power consumption (in μW)	Energy consumption (PDP) (in aJ)
[13]	487.37	**1.247**	601.53
[18]	212.08	2.457	521.14
Proposed	**102.68**	1.69	**173.45**

5.1 Standard Quaternary Inverter

Figure 4 shows input voltage pattern and output response of proposed SQI. All possible 12 transitions including $0\rightarrow 1$, $0\rightarrow 2$, $0\rightarrow 3$, $1\rightarrow 0$, $1\rightarrow 2$, $1\rightarrow 3$, $2\rightarrow 0$, $2\rightarrow 1$, $2\rightarrow 3$, $3\rightarrow 0$, $3\rightarrow 1$ and $3\rightarrow 2$ are used in input pattern. Moreover, the period of staying in each logic levels 0, 1, 2 and 3 is the same and equal to 1/4 of total time period of input pattern. The frequency of pattern is 100 MHz.

The output response in Fig. 4 demonstrates the accurate functionality of proposed SQI in transient analysis. Beyond the proposed design, this pattern is fed to presented designs in [13, 18]; then, performance parameters are measured and recorded in Table 5. The best results are defined in bold font.

According to Table 5, the proposed SQI has minimum delay time that is roughly half of [16] and 1/3 of [18] and consumes minimum energy that is approximately 1/3 of other designs. However, proposed SQI consumes 40% more power than [18], while [13] consumes 45% more power than proposed SQI.

An important point in digital circuits is that the operating frequency and output load capacitor values are not constant and may vary depending on the application. However, because of the significant role of these parameters in performance of circuits, a group of simulations are done for all designs while sweeping the frequency and load capacitor independently. First, the frequency is swept from 50 MHz to 1 GHz in four steps. The results are shown in Fig. 5a and c. In these figures, variation of frequency has not

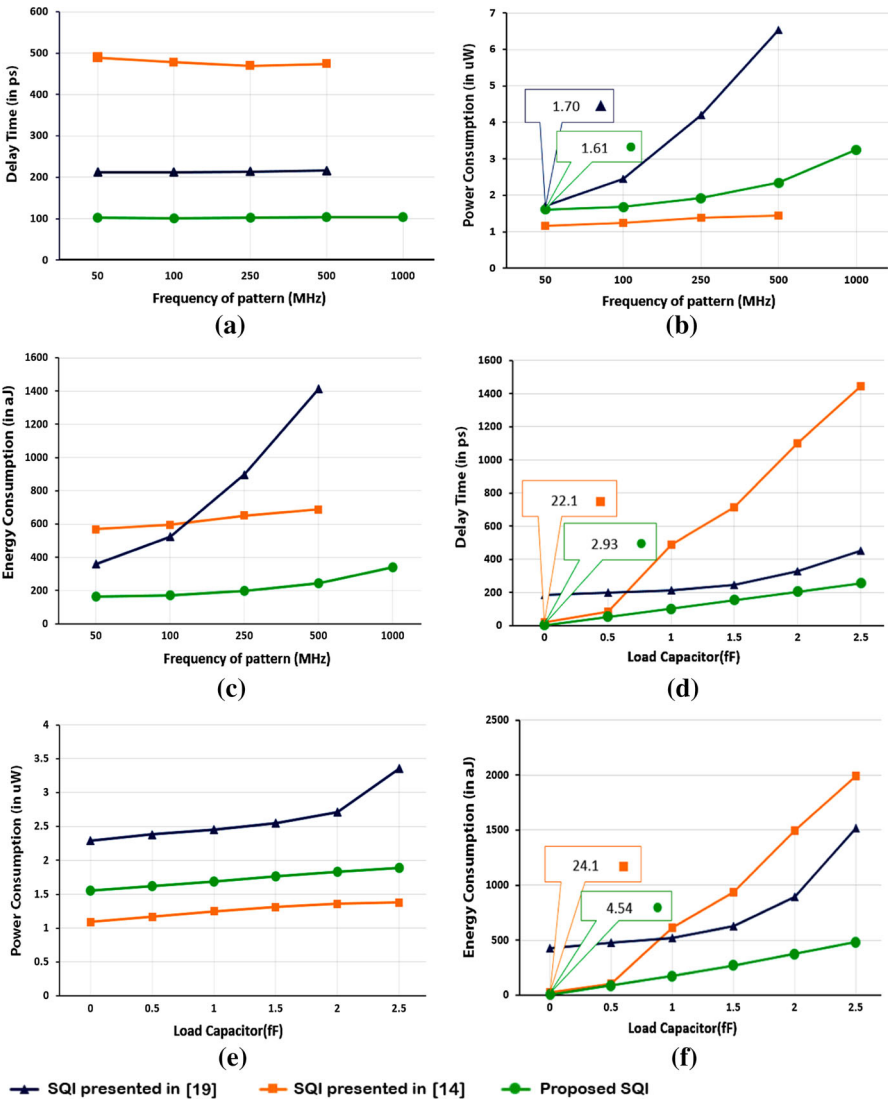

Fig. 5 Output responses including delay time, power consumption and energy consumption for SQI designs versus variation of **a**–**c** frequency, and **d**–**f** load capacitor

significant effect on delay time as it was predictable. However, increment of frequency increases the power consumption in [16]. The reason is that the weighting capacitors in this design are charged and discharged alternatively in direct relation with frequency. It is noteworthy that in high frequencies, designs of [13, 18] malfunction; hence, the results are absent in Fig. 5a and c.

In the same way, simulations are done by sweeping the value of capacitive load from 0 to 2.5 fF in 5 steps, and results are demonstrated in Fig. 5d–f.

Design of [13] has least variation response in these simulations, since the output capacitor is significantly smaller than the capacitors of the design itself. Therefore, its effect on performance of this circuit is less than that of two other designs.

The behavior of proposed design and [18] is similar, and the curves of measured parameters are ascending. However, the slope of curves in [18] is greater. Moreover, in no-load conditions, the performance parameters of proposed design improve significantly in comparison with other designs particularly compared with [13].

To fulfill the study, the robustness of designs is simulated in the presence of some process deviations in the following. The process deviations are feasible in CNFET technology as described in the literature [13, 14, 18, 25]. Therefore, a batch of simulations are carried out, while the values of the following process parameters changes independently: CNT diameter, channel/source/drain length and oxide layer thickness. Since operating temperature in actual circuits is not fixed, the simulation is also done for measuring the effect this parameter.

The result of simulations is demonstrated in Fig. 6a–l. The vertical axis is the deviation of simulated designs compared to the values of Table 5.

Increasing the diameter of CNT causes decrement in the delay time of all designs. Therefore, in spite of the little changes in power consumption, the energy consumption decreases as well, particularly up to 20% for proposed design as demonstrated in Fig. 6c. It should be noted that the energy consumption is measured in terms of power–delay product. Therefore, despite decrement of delay time and increment of power consumption, the difference of energy consumption along with the deviations of parameters moves up and down as can be seen for design of [18].

The variation of channel/source/drain length results in little decrement of delay time and energy consumption for design of [13]. However, the variation of this parameter has negligible effect on proposed design.

Deviation of oxide layer affects more than two before-mentioned parameters such that the delay times increase up to 50%, while the power consumption decreases up to 30% for proposed design. However, the energy consumption increases up to 30% for proposed design. The working temperature variation decreases delay times while increases the power consumption, but energy consumption alters very slightly.

5.2 QNAND and QNOR

QNAND and QNOR can be used as fundamental blocks for designing quaternary logic circuits. These gates have been shown in Fig. 2b and c, respectively. These gates are simulated, and their performance parameters are extracted. The input voltage patterns and output responses are depicted in Fig. 7. The input patterns include many simultaneous transitions for two inputs. The upper curves in Fig. 7 are outputs of QNAND and QNOR gates that demonstrate proper functionality of proposed designs in transient analysis.

Simulation results are tabulated in Table 6. The results are similar to values of Table 5 such that the best values of delay time and energy consumption belong to proposed gates.

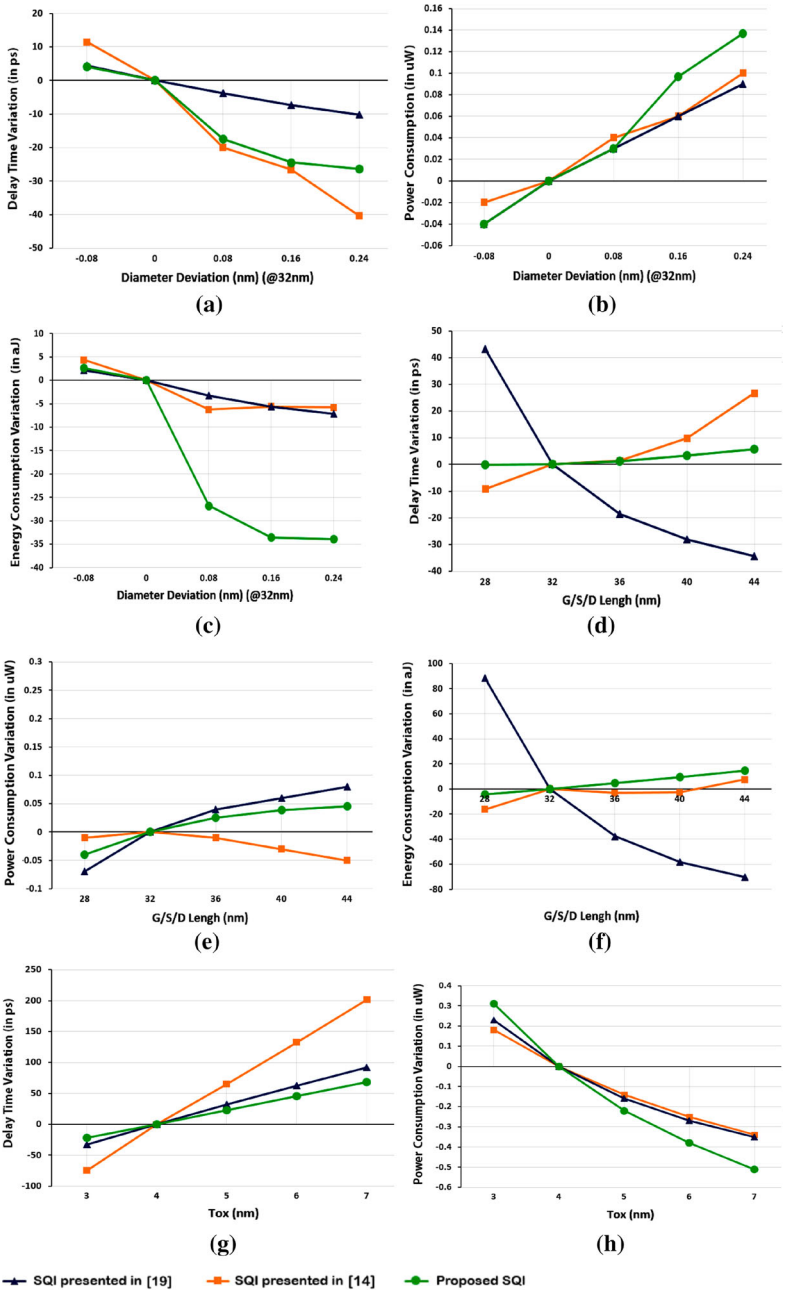

Fig. 6 Simulation results including delay time, power consumption and energy consumption for SQI designs versus variation of **a**–**c** diameter of carbon nanotube, **d**–**f** channel length, **g**–**i** oxide layer thickness and **j**–**l** operating temperature

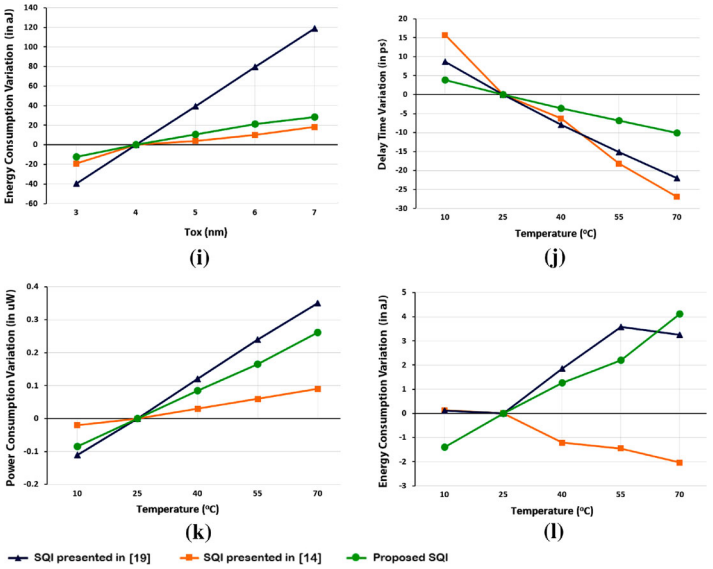

Fig. 6 continued

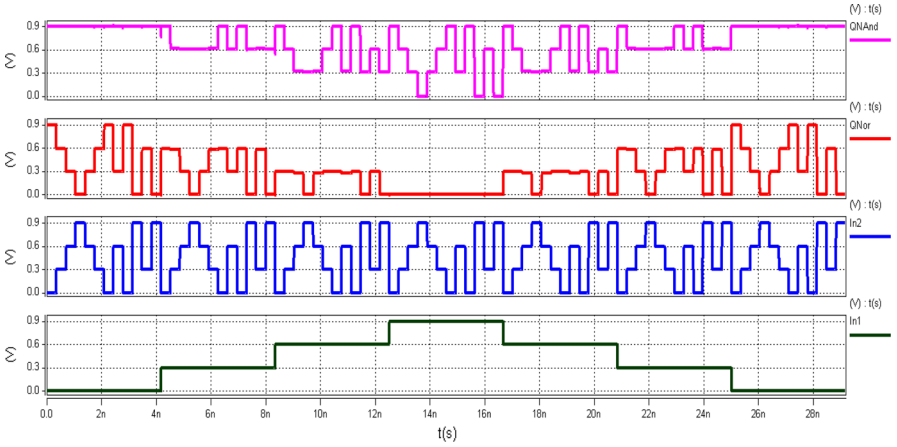

Fig. 7 Voltage pattern of inputs and outputs of the proposed QNOR and QNAND

6 Conclusion

In this paper, a new design for implementing voltage-mode standard quaternary inverter in CNFET technology was proposed. The proposed SQI furthermore includes three binary-type inverters in quaternary logic: SyQI, PQI and NQI. The design is complementary symmetric and requires only one supply voltage in addition to ground level voltage. Based on the proposed SQI, two quaternary gates, QNAND and QNOR, were presented. The VTC of these designs with suitable voltage levels and noise margin proves their proper functionality. Simulation results demonstrate better per-

Table 6 Simulation results of proposed QNOR and QNAND

Simulated design	Maximum delay time (in ps)	Average power consumption (in μW)	Energy consumption (PDP) (in aJ)
QNAND			
[13]	457.66	**1.02**	466.81
[18]	357.41	2.87	1025.76
Proposed	**105.76**	1.66	**175.56**
QNOR			
[13]	426.35	**1.46**	622.471
[18]	310.09	2.89	930.59
Proposed	**123.09**	1.67	**205.56**

formance of the proposed gates compared with two state-of-the-art designs in terms of maximum delay time and energy consumption. The proposed SQI demonstrates much better performance in no-load condition compared with other designs in terms of maximum delay and energy consumption. Particularly, in high frequencies, other designs malfunction, while the proposed SQI works properly.

Since process deviations may affect the performance of designs, some exhaustive simulations were done to study these effects. Despite deviations that alter performance parameters more or less, the proposed SQI demonstrates acceptable responses.

The SQI is fundamental gate in quaternary circuit design. In addition to QNOR and QNAND, this circuit can be used for implementing other building blocks such as quaternary XOR, binary-to-quaternary decoder and encoder, quaternary multiplexer and arithmetic circuits such as adder and multiplier. In addition, the presented designs may be used for incorporating in other digital circuits [21].

An important application of SQI is for designing SRAM cells that are widely used in digital circuits and devices. The main part of a typical SRAM cell consists of two cross-coupled SQIs. Therefore, the proposed SQI can be used to design new SRAM cells.

Due to the proper simulation results of the proposed design, it is anticipated that the performance parameters of the new designed circuits and SRAM cell are desirable too.

References

1. E. Abiri, A. Darabi, A novel design of low power and high read stability Ternary SRAM (T-SRAM), memory based on the modified Gate diffusion input (m-GDI) method in nanotechnology. Microelectron. J. **58**, 44–59 (2016)
2. A. Bozorgmehr, M.H. Moayeri, K. Navi, N. Bagherzadeh, Ultra-efficient fuzzy min/max circuits based on carbon nanotube FETs. IEEE Trans. Fuzzy Syst. **26**, 1073–1078 (2017)
3. D. Brito, T.G. Rabuske, J.R. Fernandes, P. Flores, J. Monteiro, Quaternary logic lookup table in standard CMOS. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **23**(2), 306–316 (2015)
4. J. Deng, H.-S. Wong, A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—part I: model of the intrinsic channel region. IEEE Trans. Electron Devices **54**, 3186–3194 (2007)

5. J. Deng, H.-S. Wong, A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—part II: full device model and circuit performance benchmarking. IEEE Trans. Electron Devices **54**, 3195–3205 (2007)
6. A. Doostaregan, M.H. Moaiyeri, K. Navi, O. Hashemipour, On the design of new low-power CMOS standard ternary logic gates, in *Proceedings of the 15th CSI International Symposium on Computer Architecture and Digital Systems* (2010), pp. 115–120
7. T. Eudes, B. Ravelo, A. Louis, Experimental validations of a simple PCB interconnect model for high-rate signal integrity. IEEE Trans. EMC **54**(2), 397–404 (2012)
8. T. Eudes, B. Ravelo, Analysis of multi-gigabits signal integrity through clock H-tree. Int. J. Circuit Theory Appl. **41**(5), 535–549 (2013)
9. A. Gabrielli, E. Gandolfi, A fast digital fuzzy processor. IEEE Micro **19**(1), 61–79 (1999)
10. V. Gaudet, A survey and tutorial on contemporary aspects of multiple-valued logic and its application to microelectronic circuits. IEEE J. Emerg. Sel. Top. Circuits Syst. **6**(1), 5–122 (2016)
11. S.L. Hurst, Multiple-valued logic-its status and its future. IEEE Trans. Comput. **33**(12), 1160–1179 (1984)
12. E.A. Laird, F. Kuemmeth, G.A. Steele, K. Grove-Rasmussen, J. Nygard, K. Flensberg, L.P. Kouwenhoven, Quantum transport in carbon nanotubes. Rev. Mod. Phys. **87**(3), 703 (2015)
13. J. Liang, L. Chen, J. Han, F. Lombardi, Design and evaluation of multiple valued logic gates using pseudo N-type carbon nanotube FETs. IEEE Trans. Nanotechnol. **13**(4), 695–708 (2014)
14. S. Lin, Y.-B. Kim, F. Lombardi, A Novel ternary logic design based on CNFET, in *Proceedings of IEEE International Midwest Symposium on Circuits and Systems, Cancun, Mexico* (2009)
15. S. Lin, Y.-B. Kim, F. Lombardi, Design and analysis of a 32 nm PVT tolerant CMOS SRAM cell for low leakage and high stability. Integr. VLSI J. **43**(2), 176–187 (2010)
16. X. Lu, Z. Chen, Curved pi-conjugation, aromaticity, and the related chemistry of small fullerenes. Chem. Rev. **105**(10), 3643–3696 (2005)
17. J.K. Meena, S.C. Jain, H. Gupta, S. Gupta, Synthesis of balanced quaternary reversible logic circuit, in *Circuit, Power and Computing Technologies (ICCPCT), International Conference on* (IEEE, 2015)
18. M.H. Moaiyeri, R.F. Mirzaee, A. Doostaregan, K. Navi, O. Hashemipour, A universal method for designing low-power carbon nanotube FET-based multiple-valued logic circuits. IET Comput. Digit. Tech. **7**(4), 167–181 (2013)
19. M.H. Moaiyeri, K. Navi, N. Bagherzadeh, Ultra-low-power carbon nanotube FET-based quaternary logic gates. Int. J. Electron. **103**(9), 1524–1537 (2016)
20. A. Morgenshtein, A. Fish, I.A. Wagner, Gate-diffusion input (GDI): a power efficient method for digital combinatorial circuits. IEEE Trans. VLSI Syst. **10**(5), 566–581 (2002)
21. K. Navi, A. Doostaregan, M.H. Moaiyeri, O. Hashemipour, A hardware-friendly arithmetic method and efficient implementations for designing digital fuzzy adders. Fuzzy Sets Syst. **185**(1), 111–124 (2011)
22. A. Nekooei, Z. Navabi, Multi-valued logic test access mechanism for test time and power reduction, in *Design and Technology of Integrated Systems in Nanoscale Era (DTIS), 10th International Conference on* (IEEE, 2015)
23. B. Ravelo, Delay modelling of high-speed distributed interconnect for the signal integrity prediction. Eur. Phys. J. Appl. Phys. (EPJAP) **57**(31002), 1–8 (2012)
24. A. Raychowdhury, K. Roy, Carbon-nanotube-based voltage-mode multiple-valued logic design. IEEE Trans. Nanotechnol. **4**, 168–179 (2005)
25. A. Raychowdhury, K. Roy, Carbon nanotube electronics: design of high-performance and low-power digital circuits. IEEE Trans. Circuits Syst. **54**, 2391–2401 (2007)
26. Z. Tang, Q. Cao, O. Ishizuka, A learning multiple-valued logic network: algebra, algorithm and applications. IEEE Trans. Comput. **47**(2), 247–250 (1998)
27. Y. Yang, L. Ding, J. Han, Z. Zhang, L.M. Peng, High-performance complementary transistors and medium-scale integrated circuits based on carbon nanotube thin films. ACS Nano **11**(4), 4124–4132 (2017)
28. Z. Yu, Y. Chen, H. Nan, W. Wang, K. Choi, Design of a novel low power 6-T CNFET SRAM cell working in sub-threshold region, in *Proceedings of IEEE International Conference on Electro/Information Technology (EIT)* (2011), pp. 1–5

Affiliations

Akbar Doostaregan[1] · Adib Abrishamifar[1]

Adib Abrishamifar
abrishamifar@iust.ac.ir

[1] School of Electrical Engineering, Iran University of Science and Technology (IUST), Tehran, Iran