

# Dual-Output Operational Transconductance Amplifier-Based Electronically Controllable Memristance Simulator Circuit

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Received: 16 March 2017 / Revised: 17 May 2018 / Accepted: 19 May 2018 /  
Published online: 25 May 2018  
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**Abstract** In this paper, a new floating analog memristance simulator circuit based on dual-output operational transconductance amplifiers (DO-OTA) and passive elements is proposed. Theoretical derivations are presented which describe the circuit characteristics. DO-OTA active elements in the proposed circuit are realized with CMOS transistors, and PSPICE simulations are performed. Also workability of the circuit is tested experimentally by using commercially available integrated circuits. Theoretical derivations are validated with PSPICE simulation and experimental results. All results show that proposed simulator circuit provides frequency-dependent pinched hysteresis loop and nonvolatility feature. Exciting frequency, minimum and maximum memristance values and memristance range can be adjustable electronically with bias currents by changing the transconductances of DO-OTAs. Simulator circuit has a frequency range of 1 Hz–180 kHz.

**Keywords** Memristor · Simulator · Operational transconductance amplifier · Electronically controllable

## 1 Introduction

After the announcement of Chua's memristor element in 1971 [7] and the announcement in 2008 of a group of HP Laboratories that a memristor could be realized with

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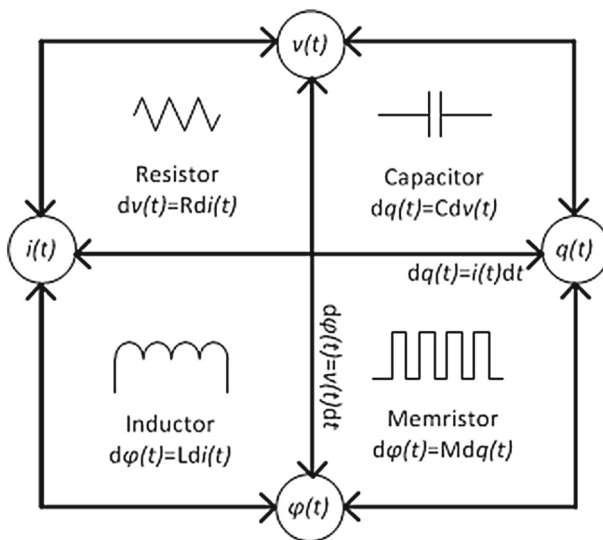
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TiO<sub>2</sub> film [14], the interest on this element has been increasing day by day. The memristor which has led to a great number of applications in various designs of analog electronics like chaotic oscillators, sensors, cellular neural networks, memory devices and other analog circuitries is the element that provides the relation between flux and charge, which is mathematically missing in circuit theory. The relations between electrical variables and elements can be seen from Fig. 1. It is not possible to find a commercial memristor product yet due to the difficulties encountered in the production of the memristor. For this reason, emulator circuit studies that mimic the mathematical model of the memristor proposed by HP are frequently found in the literature. In this study, a memristance simulator circuit which creates the magnitude in Eq. (1) proposed by Chua in 1971 is realized, not the emulator of the TiO<sub>2</sub> memristor presented by HP. In this equation, memristance ( $M$ ) is obtained when flux ( $\varphi$ )–charge ( $q$ ) curve is nonlinear, though the resistance changes with operation point. If external voltage or current is not applied, the resistance will remain constant as the operating point will not change. This is held in memory as the value of the resistance of the memristor and is called the memristance.

$$v(t) = \frac{d\varphi(t)}{dq(t)} i(t) = M(t)i(t) \quad (1)$$

There are lots of studies in the literature that the passive element values in the circuit must be changed to obtain the desired nonlinearity degree for a specific frequency [1, 4, 6, 10, 17–20]. These changes are difficult to implement, and therefore, methods are needed to make it easier to adapt. Also operation frequencies are limited to a narrow range [1, 10, 17, 18]. In [12], controllability of the circuit is provided with the help of three potentiometers. This is also a mechanical control method. Additionally, this



**Fig. 1** Basic electrical circuit elements

circuit contains many number of active and passive components. The other study in the literature that controls the memristance with the transconductance [13] exhibits memristance characteristic hysteresis curve up to 1 kHz. Another electronically controllable study has given the method of controlling with current [11], but only the conceptual structure has been proposed, and no experiment studies have been done with real elements. Also it is stated at the paper [11] that it does not support any long-term memory effect, only realizes the nonlinear memristor dynamics up to 100 Hz. Although [20] appears to be advantageous in terms of the number of active elements and [19] in terms of frequency, it can be seen that one of them contains 50 and the other contains more than 150 transistors. Some studies offer electronic controllability, but their grounded connection restriction brings disadvantage for designers [3, 5]. The other approach about the memristance circuit studies, when almost all studies in the literature are emulator circuits of HPs  $\text{TiO}_2$  memristor, a small number of circuits are from different memristance equations [6, 17]. The purpose of this study is to design a floating, nonvolatile, electronically controllable memristance simulator circuit that displays the dynamic behavior which is defined by Chua [7] in a wide frequency range.

In the proposed memristance simulator circuit, a wide range of operation frequency from 5 Hz to 180 kHz is obtained when relatively few numbers of active and passive elements are used. Electrical controllability is provided by only changing the bias currents of the dual-output transconductance amplifier (DO-OTA) circuits. Proposed circuit topology and relative equations are explained in Sect. 2. Mathematical analysis and results of simulations are given in Sect. 3. The method and results of the experimental study are given in Sect. 4. Section 6 contains the results of the study and a comparison table.

## 2 Proposed Simulator Circuit

In this section, a flux-controlled memristance simulator circuit is derived and controllability of the characteristic  $i-v$  hysteresis loop is presented. Schematic of the proposed emulator circuit is given in Fig. 2.

The circuit consists of two DO-OTA circuits and one analog multiplier. The defining equations of DO-OTA are  $i_p = i_n = 0$ ,  $i_{z+} = g_m(v_p - v_n)$  and  $i_{z-} = -g_m(v_p - v_n)$ . Analog multiplier (AM) is defined with the equation  $v_m = kv_a v_b$ .  $k$  is a real constant measured in  $\text{V}^{-1}$ .

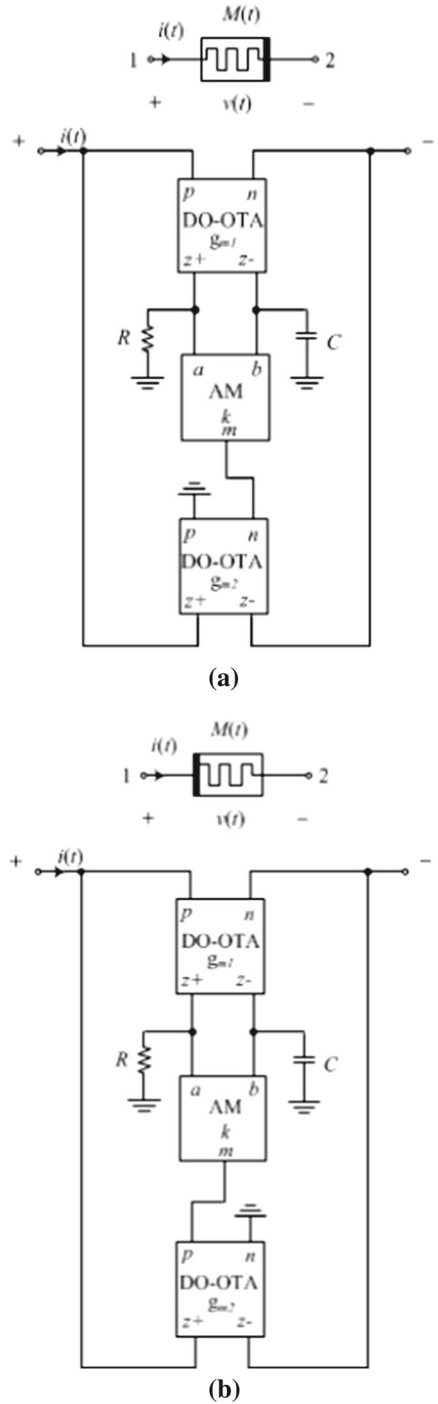
By using the defining equations of ideal devices and analyzing the circuit schematics given in Fig. 2, the voltages on the capacitor  $v_C$ , on the resistor  $v_R$ , and the output voltage of the multiplier  $v_M$  can be calculated as Eq. (2a), (2b), and (2c) respectively.

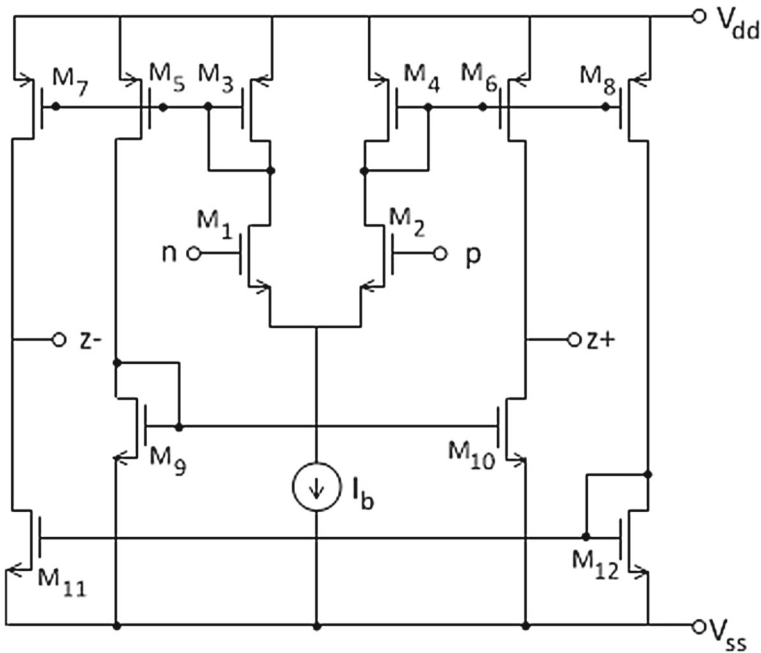
$$v_C(t) = \frac{-g_{m1}\varphi(t)}{C} \quad (2a)$$

$$v_R(t) = Rg_{m1}v(t) \quad (2b)$$

$$v_M(t) = \pm \frac{kRg_{m1}^2\varphi(t)v(t)}{C} \quad (2c)$$

**Fig. 2** Proposed memristance simulator circuits. **a** Positive memristance simulator. **b** Negative memristance simulator





**Fig. 3** Designed DO-OTA circuit

Hence, the memristance equation of simulator circuit is obtained as Eq. (3).

$$M(t) = \frac{v(t)}{i(t)} = \pm \frac{C}{kRg_{m1}^2g_{m2}\varphi(t)} \quad (3)$$

If a sinusoidal exciting source  $v_{in} = V_m \sin(\omega t)$  is applied to this device, Eq. (3) turns into Eq. (4).

$$M(t) = \pm \frac{C\omega}{kRg_{m1}^2g_{m2}V_m(1 - \cos(\omega t))} \quad (4)$$

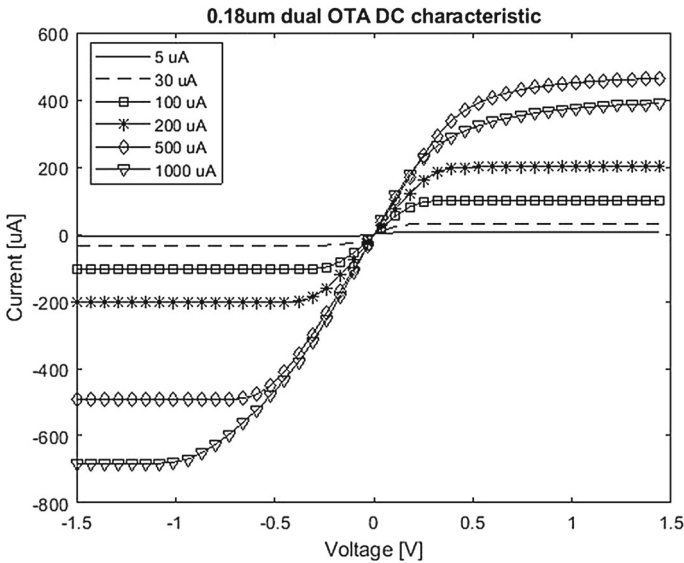
Equations (3) and (4) are used with sign '+' for positive memristance circuit in Fig. 2a. With a small connection change as in Fig. 2b, the circuit changes its sign and simulation of negative memristance values can be possible. The defining equation of negative memristance simulator circuit has sign '-.'

### 3 Theoretical and Simulation Results

In this work, a DO-OTA circuit is designed by using  $0.18 \mu\text{m}$  CMOS transistors as seen in Fig. 3 [9]. The dimensions of the MOS transistors used in the DO-OTA implementation are given in Table 1. Supply voltages are chosen as  $\pm 1.5 \text{ V}$ .  $I_b$  is the bias current to control the transconductance ( $g_m$ ) of the circuit. Designed DO-OTA circuit could have transconductance between the range  $[50\text{--}1200 \mu\text{A/V}]$  by applying

**Table 1** Dimensions of CMOS transistors

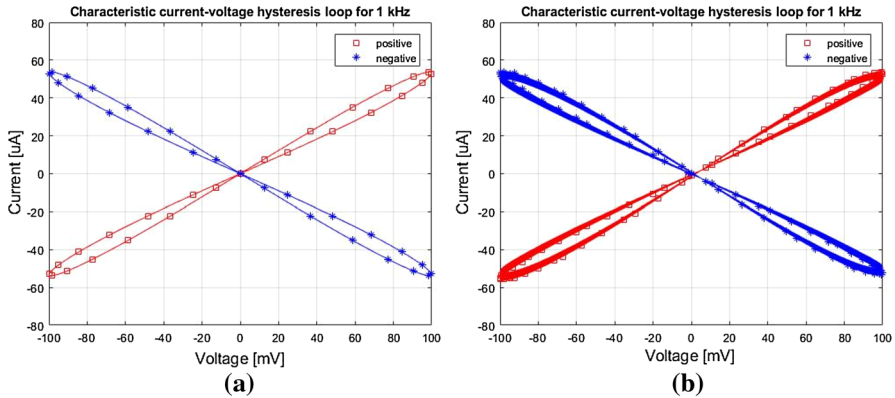
	$W(\mu\text{m})/L(\mu\text{m})$
PMOS transistors	
$M_3-M_8$	11.52/1.44
NMOS transistors	
$M_1-M_2$	4.5/0.36
$M_9-M_{12}$	5.76/1.44



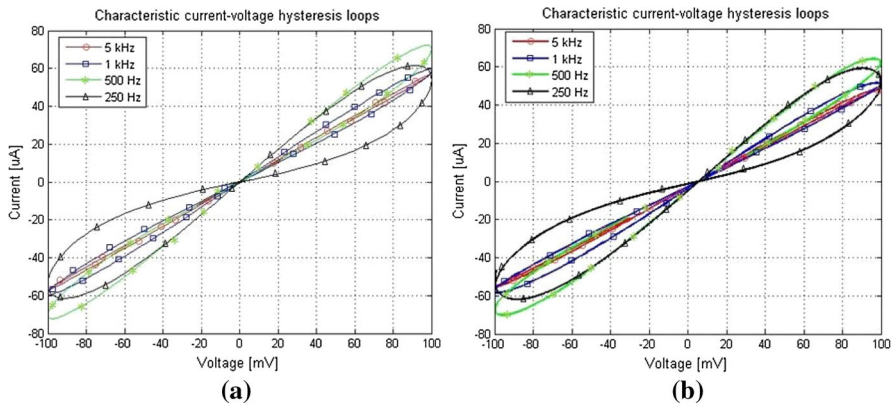
**Fig. 4** DC characteristic of DO-OTA for different bias currents

a bias current from 5 to 1000 μA. When choosing  $I_b = 200 \mu\text{A}$ , the DC characteristic of designed DO-OTA has 700 μA/V transconductance. Different transconductance curves are given in Fig. 4. Maximum symmetric differential input voltage range for this transconductance level is determined as ± 200 mV. Maximum output current is also determined as ± 200 μA. The simulations are performed using 0.18 μm level-7 TSMC CMOS technology parameters with PSPICE. AD633JN is used as AM [16].

In order to be called a circuit as a memristance simulator, the circuit should exhibit a pinched hysteresis loop in the voltage–current plane when driven by a bipolar periodic signal, the hysteresis lobe area should decrease monotonically as the excitation frequency increases and the pinched hysteresis loop should shrink to a single-valued function when the frequency tends to infinity [2]. In this study, both positive and negative memristance simulator circuit equations exhibited the characteristic current–voltage hysteresis loops which pass through the origin of the coordinate system and pinch when the frequency increases. If there is an offset shift problem due to non-ideality of analog multiplier element, it can be ensured that the hysteresis curve passes through the origin by applying an appropriate DC voltage from the ‘Summing Input’



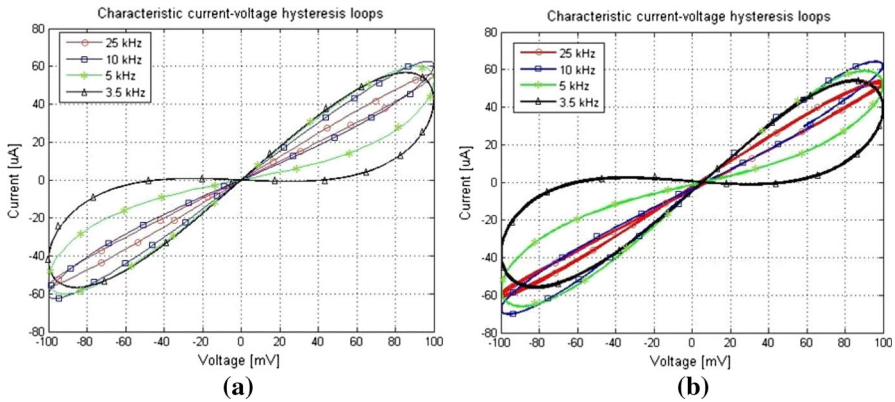
**Fig. 5** Characteristic  $i-v$  hysteresis loops for both positive and negative memristance simulators. **a** Mathematical calculations. **b** PSPICE analysis



**Fig. 6** Characteristic pinched  $i-v$  hysteresis loops for positive memristance simulator for 100 nF. **a** Mathematical calculations. **b** PSPICE analysis

terminal [16]. Figure 5a, b shows the positive and negative memristance simulator hysteresis loops for  $R = 15 \text{ k}\Omega$ ,  $C = 100 \text{ nF}$  and 1 kHz sinusoidal exciting source. To show frequency dependency of the simulator circuit, different sinusoidal exciting sources of 250, 500 Hz, 1 and 5 kHz are applied to the circuit when the other parameters stay constant. Obtained pinched hysteresis loops from mathematical calculations and PSPICE simulations are given in Fig. 6a, b respectively. According to these results, the circuit shows memristance in range [1.9–2 k $\Omega$ ] for 5 kHz, [1.75–2.2 k $\Omega$ ] for 1 kHz, [1.2–2.45 k $\Omega$ ] for 500 Hz and [1.1–5 k $\Omega$ ] for 250 Hz.

If capacitor value is decreased, frequency range in which memristor simulator shows nonlinearity speciality is increased. Figure 7 shows pinched hysteresis loops for circuit using 4.7 nF capacitor when other parameters stay constant. According to these results, the circuit shows memristance in range [1.6–2 k $\Omega$ ] for 25 kHz, [1.3–2.25 k $\Omega$ ] for 10 kHz, [1.2–5 k $\Omega$ ] for 5 kHz and [1–11 k $\Omega$ ] for 3.5 kHz. It can be seen that memristance characteristics can be exhibited over 25 kHz frequency. Congruently



**Fig. 7** Characteristic pinched  $i-v$  hysteresis loops for positive memristance simulator for 4.7 nF. **a** Mathematical calculations. **b** PSPICE analysis

**Table 2** Frequency ranges according to capacitor values

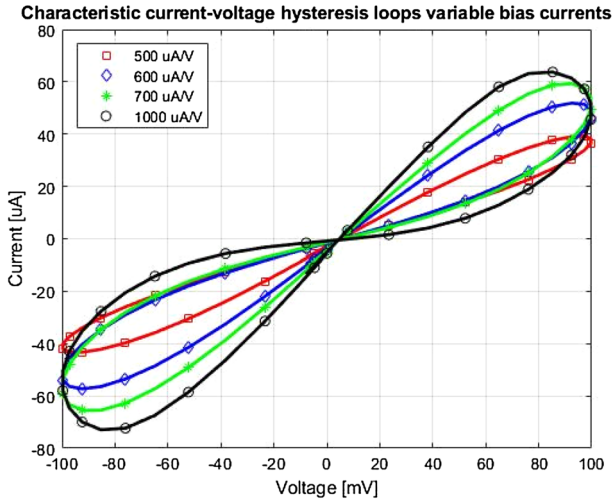
Capacitor value	Frequency range
100 pF	140–180 kHz
150 pF	110–145 kHz
220 pF	80–115 kHz
330 pF	50–85 kHz
1 nF	22–60 kHz
4.7 nF	3.2–27 kHz
100 nF	230 Hz–7 kHz
1 µF	5 Hz–300 kHz
22 µF	1–6 Hz

increasing capacitor values show memristance characteristic at lower frequencies. Frequency ranges according to capacitor values are given in Table 2.

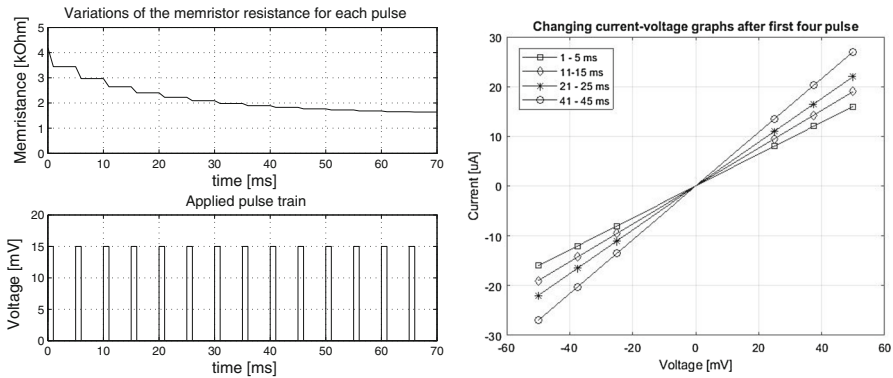
In order to obtain memristance values at different nonlinearity levels for a specific frequency, bias control current of DO-OTA elements can be adjusted. Lower bias currents create lower output currents and lower nonlinearities for memristance devices. Thus, it is possible to form a memristance simulation in a specific frequency, with a specific nonlinearity degree without changing the circuit elements. As an example, for 5 kHz input signal, Fig. 8 shows the PSPICE results of different memristance characteristics with different current sources in a simulator circuit with 4.7 nF capacitor.

In order to demonstrate the workability of the proposed simulator circuit, it is necessary to provide the nonvolatility test as well as provide the frequency-dependent pinched hysteresis loop. When 15 mV positive pulses with 5 ms period and 1 ms duration are applied continuously, the variations of the memristance are as in Fig. 9a. The circuit parameters during the pulse train are  $R = 30\text{ k}\Omega$ ,  $C = 330\text{ nF}$ , and in addition, 10 kHz, 50 mV sinusoidal exciting source, which the simulator circuit exhibits linear resistor behavior at that frequency, is connected serially to examine the impedance value of the circuit. The proposed memristor has nonvolatile characteristic





**Fig. 8** Characteristic pinched  $i-v$  hysteresis loops for 4.7 nF capacitor and variable bias currents



**Fig. 9** Variations of the memristance when positive pulses are applied continuously. **a** Variations of the memristor resistance for each pulse along the time and applied input signal. **b** Changing current–voltage graphs after first four pulses

because of the fact that memristance has no change during the pulse interval time. The shifting at the current–voltage graphs of the memristance simulator circuit, which has displayed the memristance change after each pulse, can be seen in Fig. 9b.

### 4 Experimental Results

In this section, it is intended to conduct experiments with any DO-OTA circuit, to validate the correctness of the proposed circuit topology. Because there is not a commercially available DO-OTA circuit, DO-OTA is implemented using LM13700 integrated circuit in order to obtain experimental results as Fig. 10 [15]. Since there are two OTAs in each integrated LM13700, one integrated circuit is used for one DO-

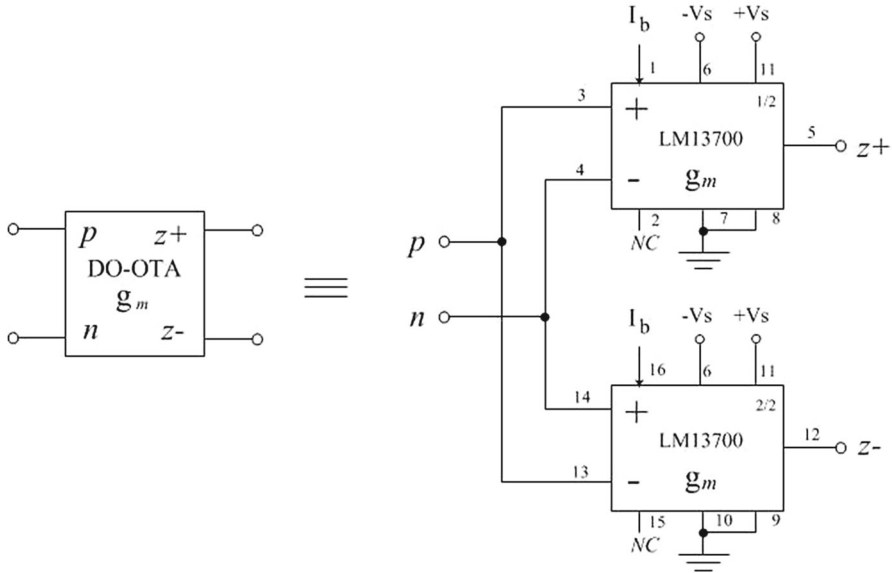


Fig. 10 Implementation of DO-OTA with LM13700 integrated circuits

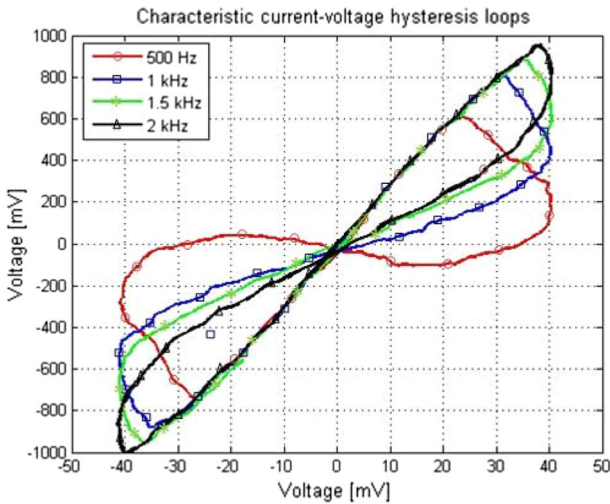
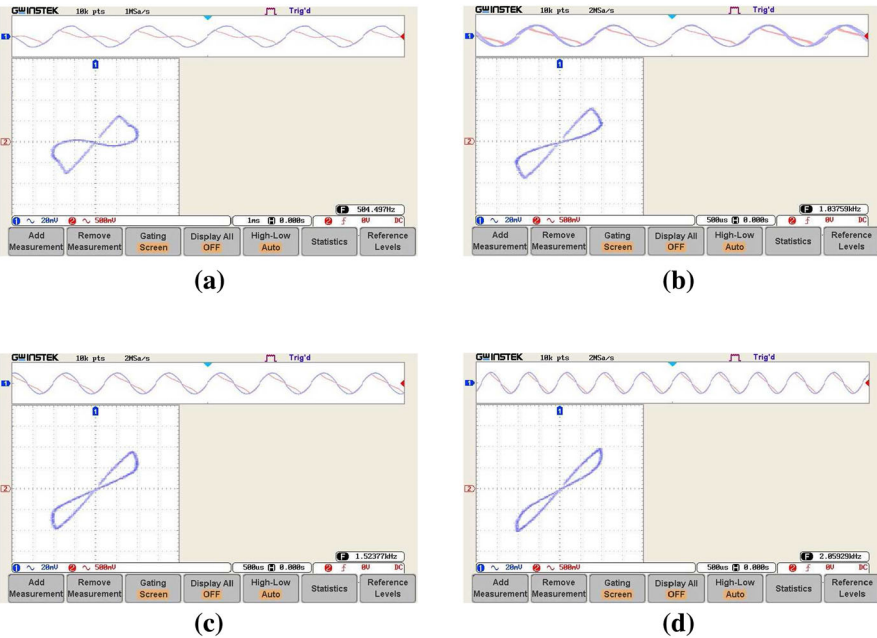


Fig. 11 Pinched hysteresis loops according to  $1700 \mu\text{A/V}$  transconductance

OTA element. Firstly, for testing the frequency-dependent pinched hysteresis loops, transconductances of OTA elements are set to  $1700 \mu\text{A/V}$ . R and C are chosen as  $15 \text{ k}\Omega$  and  $2.2 \text{ nF}$ , respectively. By applying exciting sinusoidal sources with the frequencies of 500 Hz, 1, 1.5 and 2 kHz, characteristic frequency-dependent hysteresis loops can be seen from Fig. 11. Oscilloscope outputs for this measurement are given in Fig. 12.



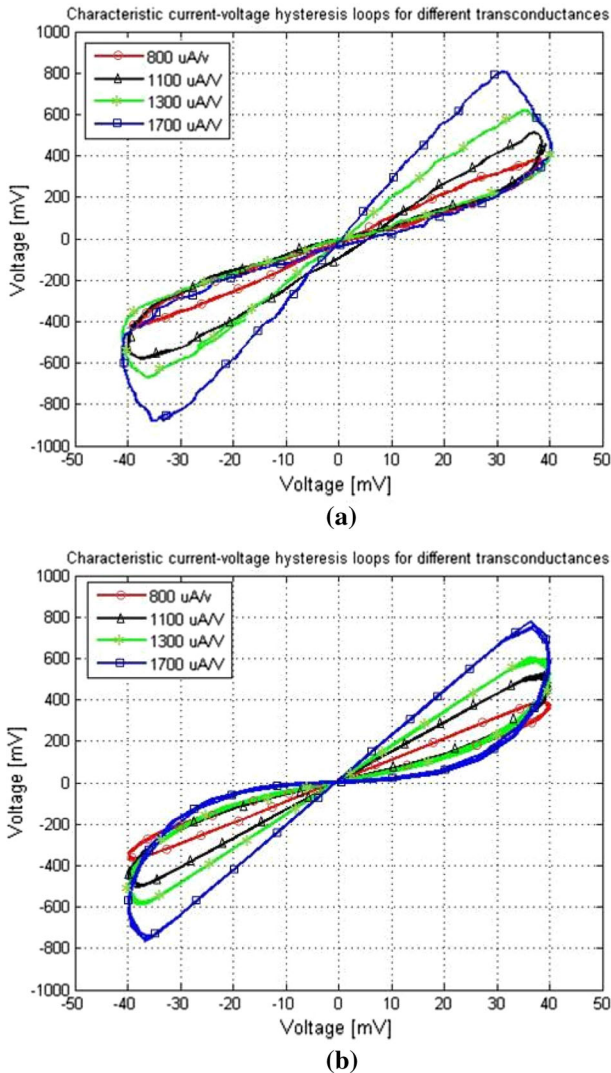
**Fig. 12** Oscilloscope output samples for transconductance of  $1700 \mu\text{A/V}$ . **a** 500 Hz. **b** 1 kHz. **c** 1.5 kHz. **d** 2 kHz

Secondly, the electronic controllability can be tested with the same circuit by applying 1 kHz sinusoidal input signal to the circuit with transconductances being 800, 1100, 1300 and  $1700 \mu\text{A/V}$ . Different nonlinearity degrees are obtained as can be seen in Fig. 13, by using ideal DO-OTA circuit which was formed with ideal dependent sources in PSPICE and by using LM13700 onboard circuit.

## 5 An Application Example: Serial MC Circuit

In order to show applicability of the proposed memristance simulator circuit, serial MC and RC connections are simulated as in Fig. 14a. If decremental memristor is used in MC circuit, discharge time must be lower; for incremental memristor, discharge time must be higher than serial RC circuit. Used passive element values are  $C = 1 \text{ nF}$ ,  $R = 1.2 \text{ k}\Omega$  and  $M_{\text{initial}} = 1.2 \text{ k}\Omega$ .

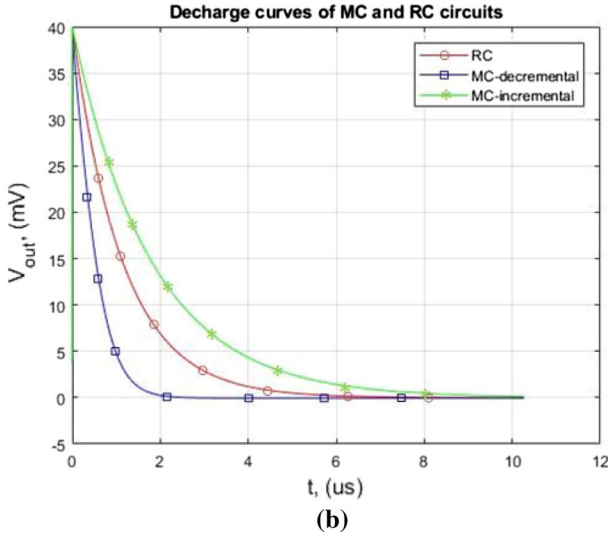
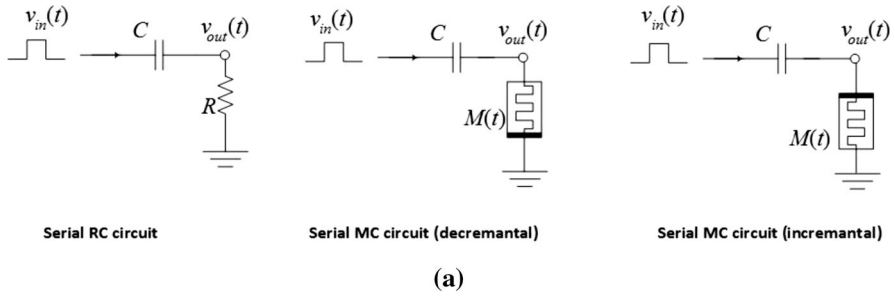
According to resistance variations, decay time varies and if memristance becomes lower than initial memristance value, time constant becomes lower. In case of usage of incremental memristor, memristance value is higher than initial memristance value and time constant will be higher as shown in Fig. 14b. As a result, the applicability is verified because simulation results are very similar to Joglekar's theoretical MC circuit [8].



**Fig. 13** Controllability of memristance value by changing transconductance for 1 kHz input. **a** Onboard circuit with LM13700. **b** PSPICE with ideal DO-OTA circuit

## 6 Conclusion

In this work, an analog circuit which shows memristance characteristics is proposed by using two DO-OTAs, one analog multiplier, one grounded resistor and one grounded capacitor. Proposed topology has wide enough frequency ranging from 5 Hz up to 180 kHz to satisfy frequency-dependent pinched hysteresis  $i-v$  loop. It is possible to obtain different nonlinearity degrees with a specific input frequency by adjusting  $g_m$  values of DO-OTAs with  $I_b$  current. That is, the memristance value of the proposed



**Fig. 14** Serial RC and MC circuit application examples. **a** RC and MC circuits. **b** Discharge curves of RC and MC circuits

memristance simulator circuit can be electronically controlled by using bias current. The nonvolatility is displayed by applying a pulse train to the circuit. Theoretical calculations and PSPICE simulations are in good agreement. Also, the proposed circuit is floating and suitable for use as grounded. No matching condition is required for any circuit element or circuit parameter. Decreasing- and increasing-type-memristance simulation can be realized with a simple connection shifting.

Table 3 shows a comparison between existing studies. Electronic controllability feature is the most distinctive advantage of memristor emulator and simulator circuits. The proposed structure has a certain advantage in frequency between the simulator circuits. Also it has an advantage in terms of number of elements between emulator circuits. Given the floating structure, the preference of the topology is increasing. With the production of MOS DO-OTA circuit, it is clear that using this simulator circuit in memristive applications will be appropriate. The workability of the proposed floating memristance simulator circuit has been demonstrated by theoretical calculations, PSPICE simulations and experimental results.

**Table 3** Comparison between existing studies

Refs.	Number of active comp.	Number of passive comp.	Circuit type	Electr. contr.	Max. freq.	Floating
[6]	5	4	Simulator	No	40 kHz	Yes
[10]	6	10	Emulator	No	800 Hz	No
[17]	16	27	Simulator	No	300 Hz	Yes
[18]	8	12	Emulator	No	1 kHz	Yes
[20]	2	3	Emulator	No	1 MHz	Yes
[19]	16	7	Emulator	No	MHz level	No
[1]	4	10	Emulator	No	6 kHz	Yes
[4]	4	4	Emulator	No	8 kHz	Yes
[12]	12	9	Emulator	No	MHz level	No
[13]	7	7	Emulator	Yes	10 kHz	Yes
[11]	2	1	Emulator	Yes	100 Hz	Yes
[5]	7	6	Emulator	Yes	7 kHz	No
[3]	3	4	Emulator	Yes	7 kHz	No
Proposed circuit	3	2	Simulator	Yes	180 kHz	Yes

## References

1. M.T. Abuelmaatti, Z.J. Khalifa, A new floating memristor emulator and its application in frequency-to-voltage conversion. *Analog Integr. Circuits Signal Process.* **86**(1), 141–147 (2016)
2. S.P. Adhikari, MPd Sah, H. Kim, Three fingerprints of memristor. *IEEE Trans. Circuits Syst. I Regul. Pap.* **60**(11), 3008–3021 (2013)
3. A.G. Alharbi, M.E. Fouda, Z.J. Khalifa, M.H. Cowdhury, in *2016 IEEE 59th International Midwest Symposium on Simple Generic Memristor Emulator for Voltage-Controlled Models, Circuits and Systems (MWSCAS)* (2016), pp. 1558–3899
4. A.G. Alharbi, M.E. Fouda, M.H. Cowdhury, A novel flux-controlled memristive emulator for analog applications, advances in memristors, memristive devices and systems. *Stud. Comput. Intell.* **701**, 493–511 (2017)
5. A.G. Alharbi, M.E. Fouda, Z.J. Khalifa, M.H. Cowdhury, Electrical nonlinearity emulation technique for current-controlled memristive devices. *IEEE Access* **5**, 5399–5409 (2017)
6. Z.G. Cam, H. Sedef, A new floating memristance simulator circuit based on second generation current conveyor. *J. Circuits Syst. Comput.* **26**(2), 1750029 (2017)
7. L. Chua, Memristor—the missing circuit element. *IEEE Trans. Circuit Theory* **18**(5), 507–519 (1971)
8. Y.N. Joglekar, S.J. Wolf, The elusive memristor: properties of basic electrical circuits. *Eur. J. Phys.* **30**(4), 661–675 (2009)
9. K. Kaewdang, W. Surakamponorn, On the realization of electronically current-tunable CMOS OTA. *AEU Int. J. Electron. Commun.* **61**, 300–306 (2007)
10. H. Kim, MPd Sah, C. Yang, S. Cho, L.O. Chua, Memristor emulator for memristor circuit applications. *IEEE Trans. Circuits Syst. I Regul. Pap.* **59**(10), 2422–2431 (2012)
11. I. Koymen, E.M. Drakakis, in *14th International Workshop on CMOS-Based Nanopower Memristor Dynamics Emulator, Cellular Nanoscale Networks and Their Applications (CNNA)* (2014)
12. V.H. Nguyen, K.Y. Sohn, H. Song, On-printed circuit board emulator with controllability of pinched hysteresis loop for nanoscale TiO<sub>2</sub> thin-film memristor device. *J. Comput. Electron.* **15**(3), 993–1002 (2016)
13. H. Sozen, U. Cam, Electronically tunable memristor emulator circuit. *Analog Integr. Circuits Signal Process.* **89**(3), 655–663 (2016)

14. D.B. Strukov, G.S. Snider, D.R. Stewart, S.R. Williams, The missing memristor found. *Nature* **453**(7191), 80–83 (2008)
15. Texas Instruments, LM13700 dual operational transconductance amplifiers with linearizing diodes and buffers. LM13700 datasheet, Rev. F. (2015)
16. Texas Instruments, Low cost analog multiplier. AD633 datasheet, Rev. K. (2016)
17. L. Wei, W. Fa-Qiang, M. Xi-Kui, Exponential flux-controlled memristor model and its floating emulator. *Chin. Phys. B* **24**(11), 118401 (2015)
18. C. Yang, H. Choi, S. Park, M.P. Sah, H. Kim, L.O. Chua, A memristor emulator as a replacement of a real memristor. *Semicond. Sci. Technol.* **30**(1), 015007 (2015)
19. C. Yener, H.H. Kuntman, Fully CMOS memristor based chaotic circuit. *Radioengineering* **23**(4), 1140–1149 (2014)
20. A. Yesil, Y. Babacan, F. Kacar, A new DDCC based memristor emulator circuit and its applications. *Microelectron. J.* **45**(3), 282–287 (2014)