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A Novel Generalized Parallel Two-Box Structure for Behavior Modeling and Digital Predistortion of RF Power Amplifiers at LTE Applications

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Abstract This paper presents a generalized parallel two-box structure that is proposed for modeling and digital predistortion of power amplifiers and wireless transmitters exhibiting memory effects. The proposed predistortion scheme consists of two separable boxes; the first is utilized to model the static behavior of the power amplifier, while the second is proposed to consider the memory effect and nonlinear distortion of the power amplifier. The coefficients of the proposed model are identified by applying an indirect learning structure and a least square method. The validation of the proposed model is carried out using the simulation of the power amplifier and the digital predistortion excited by a 64QAM signal in the advanced design system software. According to the simulation results, the criterion of adjacent channel power ratio reduced by about 16 dB. The simulation results reveal an adjacent channel power ratio of almost -48 dB. Indeed, the proposed model leads to a better performance in terms of spectral regrowth in comparison with the memory polynomial model, and it also reduces the number of coefficients by approximately 22%. This proposed model enables a more accurate modeling of nonlinear distortion and memory effects compared to previous linearization methods.

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1 Introduction

The power amplifier (PA) is a fundamental component of wireless communication systems. Because a large amount of power is consumed by the radio frequency (RF) power amplifiers in transmitters, these circuits are known as power hungry blocks [27]. If the power amplifier circuits are driven at a saturation operating point, they generate the nonlinearities in an advanced communication system, causing not only out of band distortion, i.e., spectral regrowth, but also in-band distortions [29]. These distortions lead to severe interference of the adjacent channels and increase in the amount of error vector magnitude (EVM) [22]. Modern communication systems, such as worldwide interoperability for microwave access (WiMAX) and long-term evolution (LTE), exploit efficient modulation approaches in order to improve data transmission rate within a limited band [1].

The signals of the systems vary rapidly and have high peak to average power ratio [Orthogonal frequency-division multiplexing (OFDM) ∼ 10 dB]. Therefore, the power amplifier must be operated at a power level that is far from its saturation point. As a result, transmission of non-constant envelope signals employing power amplifiers at linear operation region has poor efficiency [6]. Thus, the efficiency of the power amplifier is dramatically reduced due to the large back-off from saturation operating point. Consequently, the trade-off between linearity and efficiency is emerging in RF power amplifier design. In order to improve linearity without losing efficiency, the use of power amplifier linearization methods is indispensable. For this reason, several linearization techniques, such as feedback, feedforward, and predistortion, have been proposed to improve the linearity of the transmitter and the power amplifier without sacrificing efficiency [26]. The predistortion method has suitable performance and low cost among the linearization techniques [2].

Figure 1 shows the conceptual diagram of the predistortion linearization process. In the predistortion linearization method, the input signal is predistorted before applying it to the input of a nonlinear power amplifier, so that the nonlinear response of the power amplifier can be compensated for, enabling the output of the amplifier to yield a linear response.

It is clear from Fig. 1 that the response of the power amplifier is compressive, while the input/output characteristic of the predistortion has an expanding behavior. Theoretically, the expanding characteristic of the predistortion can compensate for the compressing behavior of the power amplifier. As a result, the relationship between the input and output of the system will be linear. The predistortion can be classified into two types in accordance with the techniques used: (1) analog predistortion (APD) (2) digital predistortion (DPD).

The analog predistortion (ADP) directly operates with the analog signal and is placed near the power amplifier. When the analog predistortion operates at a high frequency, the analog predistortion implementation is so straightforward, but it shows
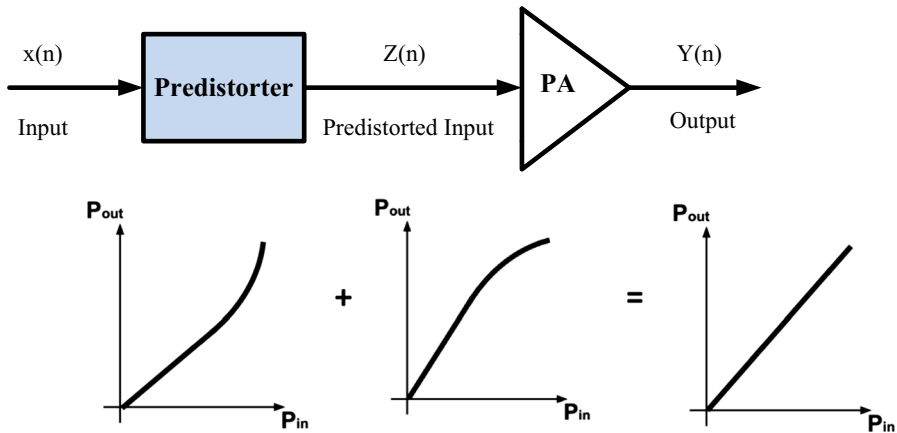
Fig. 1 Simplified concept of a predistortion linearization technique

limited capability and low performance [21]. Many analog predistortion circuits that have cost-effective and simple structures are described [4,14,18,24,32,34]. Although analog predistortion has several advantages compared to digital predistortion, such as simple structure and low cost, its capability to remove nonlinearity is less than that of digital predistortion. Indeed, while most analog predistortion circuits are employed in a narrow band application, the performance of analog predistortion is not comparable to digital predistortion. For example, Seo proposed an analog predistorter based on a Schottky diode, but the improvement in the adjacent channel power ratio is very small [30].

One of the linearization procedures commonly utilized in advanced communication systems is the digital predistortion method [2,9,12,15,26,35].

Because of digital hardware implementation, digital predistortion is one of the most useful approaches of linearization, with high flexibility and low cost. The accuracy of linearization is substantially augmented by digital implementation [20]. A memoryless model was commonly employed in the primary linearization procedures based on digital predistortion such that the model compensated for the static nonlinear behavior of the power amplifier [23]. The static nonlinear behavior is fully characterized in terms of amplitude modulation/amplitude modulation (AM/AM) and amplitude modulation/phase modulation (AM/PM) effects [5]. Cho proposed a lookup table (LUT) instead of the memoryless model, but the LUT may not usefully eliminate distortions in modern wireless transmitters. Furthermore, when the bandwidth of the power amplifier is increased in most modern transmitters, the memory effects of the power amplifier are not trivial. The memory effects of the power amplifier must be investigated to achieve the best performance of digital predistortion [16]. The Volterra series is the most appropriate model used to accurately model nonlinear dynamic systems [28]. When the order of memory depth and nonlinearity increases, the number of utilized coefficients increases very rapidly; hence, the computational complexity of the model is augmented. Guan [11] has recently proposed the Volterra series to model predistortion; however, the resource consumption, as well as the complexity
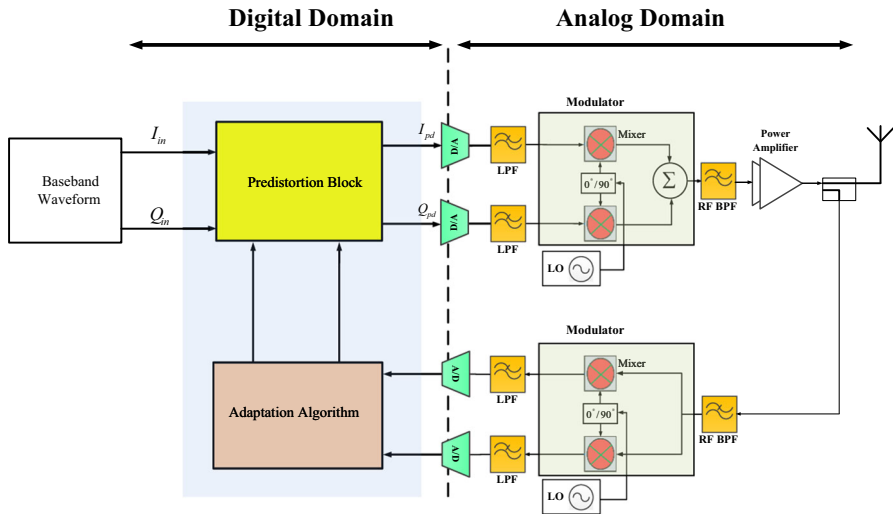
Fig. 2 The schematic of the digital predistortion block and the power amplifier

of the predistortion, has increased. Therefore, many structures that originate from the Volterra model, such as Wiener model [19], Hammaerstion model [20], and memory polynomial model [7], are proposed in order to overcome the complexity of the Volterra series. The models of Hammerstein and Wiener are commonly employed in low bandwidth applications. Moon [22] suggested an enhanced Hammerstein model, but the model and coefficients identification are very complex.

Nowadays, with the impressive growth in DSP techniques, most linearization methods based on digital predistortion are completely implemented in baseband domain. An overall system made of the power amplifier and digital predistortion-based linearization method has been depicted in Fig. 2. In this system, first, the generated baseband signal is distorted using the predistortion block, and then the distorted signal is passed through a digital to analog converter (DAC) in order to convert it to an analog signal. Similarly, the radio frequency signal is generated using a modulator composed of a mixer, local oscillator, and combiner, and then the RF signal is applied to the power amplifier in order to amplify the transmission signal.

In order to extract and update the coefficients of the digital predistortion model, as illustrated in Fig. 2, a small portion of the transmitted signal is taken by a coupler. The frequency of the return signal is down converted by the modulator, and the resultant signal is transformed to a digital signal using an analog to digital converter (ADC). The digital signal is then applied to the adaptation algorithm block, which takes a sample of input and output data and updates the coefficients of the predistortion block, in order to achieve an effective linearization method. The feedback path which is shown in Fig. 2 works only in the initial system setup or whenever the characteristics of the system have wide variations. Therefore, the design and implementation of a digital predistortion system include two parts: (1) The digital predistortion block: The input signals I and Q should be distorted by applying the digital predistortion block. (2) The

adaptation algorithm block is utilized for updating the coefficients of the predistortion block.

This paper proposes a generalized parallel two-box (GPTB) model to model and carries out digital predistortion (DPD) of power amplifiers. The proposed predistortion scheme includes two separable boxes; the first is utilized to model the static behavior of the power amplifier, while the second is proposed in order to consider the memory effect and nonlinear distortion of the power amplifier.

This paper is organized as follows: In Sect. 2, the proposed generalized parallel two-box model is described and the methods of coefficients identification are accurately introduced. Next, the performance assessment of the proposed model is completely expressed in Sect. 3. In this section, power amplifier model extraction and verification are carried out first, after which coefficients identification of the proposed model is done using the indirect learning method. Simulation of the overall transmitter with and without predistortion is carried out at the end of this section. Finally, the conclusion is presented in Sect. 4.

2 Generalized Parallel Two-Box (GPTB) Behavioral Model Based on Hybrid Memory Polynomial

2.1 Model Architecture

In this section, the generalized parallel two-box structure is proposed for the modeling of the digital predistorter. The proposed model consists of hybrid memory polynomial and memoryless nonlinear function, as depicted in Fig. 3. The first memoryless box emulates the static behavior of the power amplifier, while the second box considers the linear and nonlinear memory effects of the power amplifier. The detailed operation of the proposed generalized parallel two-box structure is explained as follows:

#### 2.1.1 Memoryless Nonlinear Function

The memoryless polynomial model is proposed in order to emulate the memoryless nonlinear function of the generalized parallel two-box predistorter. This function considers the static behavior of the power amplifier, which includes AM/AM and AM/PM characteristics.

The baseband complex output signal (y_{MLP}) of the memoryless polynomial function is defined as a function of its baseband complex input $x(n)$ signal according to:

$$Y_{MLP}(n) = \sum_{k=1}^{K_{MLP}} a_k \cdot x(n) \cdot |x(n)|^{k-1} \tag{1}$$

where a_k indicates the coefficients of the memoryless polynomial and K represents the memoryless polynomial function nonlinearity order.

Fig. 3 The proposed
generalized two-box predistorter
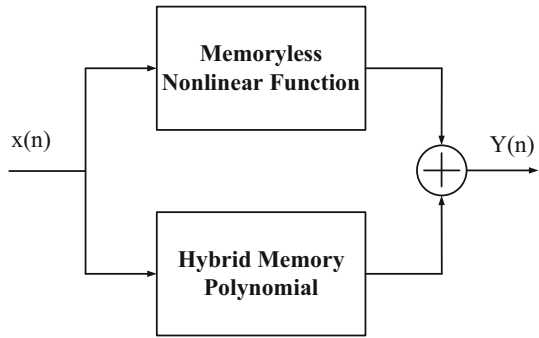
2.1.2 Hybrid Memory Polynomial

The hybrid memory polynomial has been suggested in order to consider the memory effect of the power amplifier in the proposed model. The hybrid memory polynomial model augments the memory polynomial model through the inclusion of cross-terms [13]. The parallel combination of the memory polynomial (MP) model and the envelope memory polynomial (EMP) model has been utilized to make the hybrid memory polynomial model, as illustrated in Fig. 4.

Therefore, the input/output signal of the hybrid memory polynomial model is defined as follows:

$$y_{\text{HMP}}(n) = \sum_{m=0}^{M} \sum_{k=1}^{K} a_{km} \cdot x(n-m) \cdot |x(n-m)|^{k-1}$$
$$+ \sum_{m=1}^{M_e} \sum_{K=1}^{K_e} b_{km} \cdot x(n) \cdot |x(n-m)|^{k-1} \tag{2}$$

where a_{mk} and b_{mk} are the coefficients of the memory polynomial and the envelope memory polynomial model, respectively. Also, K and M are the nonlinearity order and memory depth of the memory polynomial model, respectively. Similarly, K_e and M_e represent the nonlinearity order and memory depth of the envelope memory polynomial model, respectively. $x(n)$ and $y_{\text{HMP}}(n)$ refer to the input and output baseband complex waveforms of the model, respectively. The hybrid memory polynomial consists of two basic functions; therefore, Eq. (2) can be rewritten as:

$$y_{\text{HMP}}(n) = \phi_{\text{HMP}}(n) \cdot A \tag{3}$$

where the input data vector $\phi_{\text{HMP}}(n)$ and the coefficients vector A are described as

$$A = \begin{bmatrix} A_{\text{MP}} \\ A_{\text{EnvMP}} \end{bmatrix} \tag{4}$$

Memory Polynomial Model
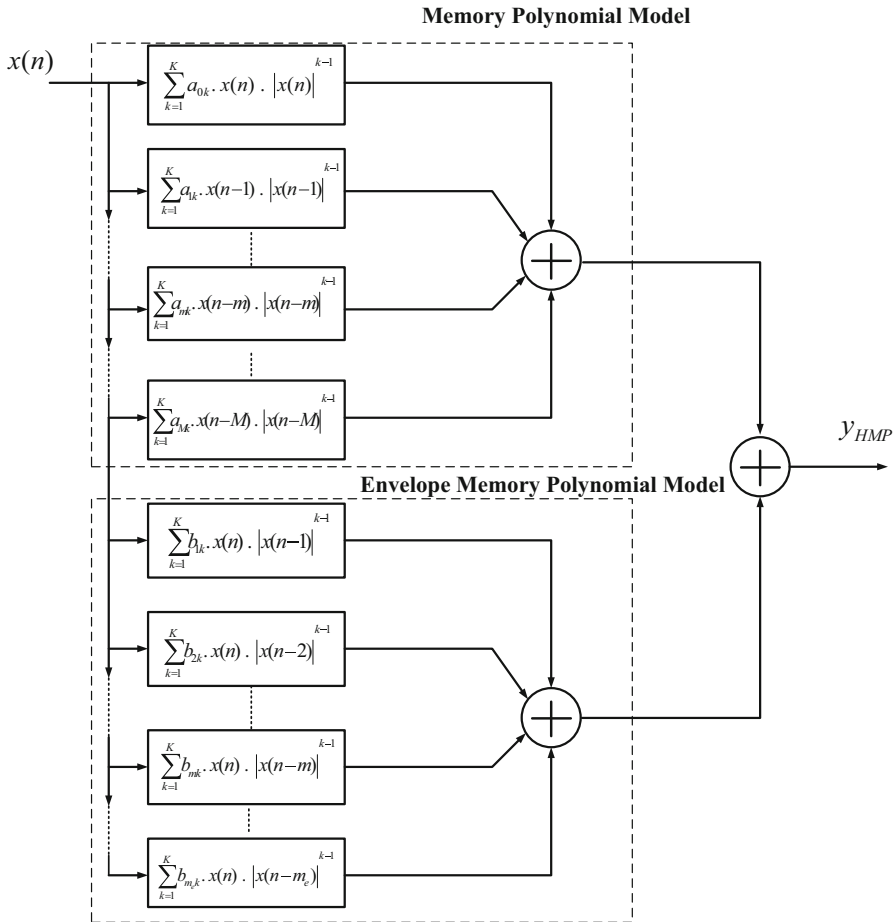
Fig. 4 Block diagram of the hybrid memory polynomial model

with

$$A_{\mathrm{MP}} = [a_{01} \cdots a_{0k} \; a_{11} \cdots a_{1K} \cdots a_{MK}]^{\mathrm{T}} \tag{5}$$

$$A_{\mathrm{EnvMP}} = \left[b_{12} \cdots b_{1k_{\mathrm{e}}} \; b_{22} \cdots b_{2K_{\mathrm{e}}} \cdots b_{M_{\mathrm{e}}K_e}\right]^{\mathrm{T}} \tag{6}$$

where $[.]^{\mathrm{T}}$ denotes the transpose operator and

$$\varphi_{\mathrm{HMP}}(n) = [\phi_{\mathrm{MP}}(n)\phi_{\mathrm{EnvMP}}(n)] \tag{7}$$

with

$$
\phi_{\text{MP}}(n) =
\begin{bmatrix}
x(n) \\
\vdots \\
x(n) \cdot |x(n)|^{k-1} \\
x(n-1) \\
\vdots \\
x(n-1) \cdot |x(n-1)|^{k-1} \\
\vdots \\
x(n-M) \cdot |x(n-M)|^{k-1}
\end{bmatrix}^{\text{T}}
\tag{8}
$$

$$
\phi_{\text{EnvMP}}(n) =
\begin{bmatrix}
x(n) \cdot |x(n-1)| \\
\vdots \\
x(n) \cdot |x(n-1)|^{K_e-1} \\
x(n) \cdot |x(n-2)| \\
\vdots \\
x(n) \cdot |x(n-2)|^{K_e-1} \\
\vdots \\
x(n) \cdot |x(n-M_e)|^{K_e-1}
\end{bmatrix}^{\text{T}}
\tag{9}
$$

The hybrid memory polynomial model incorporates the memory polynomial model and the envelope memory polynomial model in order to construct a very high-performance model. This model is placed in the bottom box of the proposed model with the aim of generating a distortion that is complementary of the distortion of the power amplifier and eliminating the memory effect of the power amplifier.

2.2 Model Identification

In this paper, the memory polynomial model has been employed in order to model the highly nonlinear power amplifier. Kim and Konstantinou [17] proposed the memory polynomial model several years ago. Due to the trade-off possible between complexity and accuracy, this model is one of the most popular models for behavior modeling of the power amplifier and predistortion. However, the coefficients of this model increase quickly when the highly nonlinear memory effect appears in the power amplifier.

When the coefficients of Volterra series [11] change to diagonal terms (i.e., removing all cross-terms), the memory polynomial model is generated. The model is a two summation formula with two parameters: nonlinear order and memory depth. The baseband complex output signal ($y_{\text{MP}}(n)$) of the memory polynomial model as a function of the baseband complex input signal ($x(n)$) can be described by the following equation:

$$y_{\mathrm{MP}}(n) = \sum_{m=0}^{M} \sum_{k=1}^{K} \alpha_{mk} \cdot x(n-m) \cdot |x(n-m)|^{k-1} \tag{10}$$

where α_{mk} indicates the coefficients of the model and K and M refer to the nonlinear order and memory depth, respectively. $y(n)$ is the complex output sample of the model at instant n, and $x(n-m)$ is the complex input sample at instant $n-m$.

If we rewrite Eq. (10) as a generic formulation, the equation is rewritten in vector format as:

$$y_{\mathrm{MP}}(n) = \varphi_{\mathrm{MP}}(n) \cdot A \tag{11}$$

where $\varphi_{\mathrm{MP}}(n)$ is a vector built using complex input signal samples $x(n-m)$ and A is a vector containing the model coefficients. These vectors are given by:

$$\phi_{\mathrm{MP}}(n) = \begin{bmatrix} x(n) \\ \vdots \\ x(n) \cdot |x(n)|^{k-1} \\ x(n-1) \\ \vdots \\ x(n-1) \cdot |x(n-1)|^{k-1} \\ \vdots \\ x(n-M) \cdot |x(n-M)|^{k-1} \end{bmatrix}^{\mathrm{T}} \tag{12}$$

$$A = [\alpha_{01} \cdots \alpha_{0k} \; \alpha_{11} \cdots \alpha_{1k} \cdots \alpha_{MK}]^{\mathrm{T}} \tag{13}$$

For a set of N samples, this vector representation can be rewritten in matrix format as follows:

$$y = X \cdot A \tag{14}$$

where y is the vector of N samples of the output signal and given by:

$$y = \begin{bmatrix} y(n) \\ y(n-1) \\ \cdots \\ \cdots \\ \cdots \\ y(n-N+1) \end{bmatrix}^{\mathrm{T}} \tag{15}$$

Also, X is a matrix whose rows are delayed versions of $\varphi_{\mathrm{MP}}(n)$. It is defined as follows:

$$X = [\varphi_{\mathrm{MP}}(n) \quad \varphi_{\mathrm{MP}}(n-1) \cdots \varphi_{\mathrm{MP}}(n-N+1)]^{\mathrm{T}} \tag{16}$$

$$X = \begin{bmatrix} x(n) & \cdots & x(n) \cdot |x(n)|^{K-1} & x(n-1) & \cdots & x(n-1) \cdot |x(n-1)|^{K-1} \\ x(n-1) & \cdots & x(n-1) \cdot |x(n-1)|^{K-1} & x(n-2) & \cdots & x(n-2) \cdot |x(n-2)|^{K-1} \\ \vdots & \cdots & \vdots & \vdots & \cdots & \vdots \\ x(n-N+1) & \cdots & x(n-N+1) \cdot |x(n-N+1)|^{K-1} & x(n-N) & \cdots & x(n-N) \cdot |x(n-N)|^{K-1} \end{bmatrix}$$

$$\begin{array}{ll} \cdots & x(n-M) \cdot |x(n-M)|^{K-1} \\ \cdots & x(n-M-1) \cdot |x(n-M-1)|^{K-1} \\ & \vdots \\ \cdots & x(n-M-N+1) \cdot |x(n-M-N+1)|^{K-1} \end{array} \Bigg]^{\mathrm{T}}$$

$$(17)$$

If the matrix X was invertible, the coefficients identification would be given by:

$$A = X^{-1} \cdot y \tag{18}$$

In order to perform coefficients extraction, an approximate solution can be achieved by minimizing the mean squared error, e, given by:

$$e = \|y - XA\|^2 \tag{19}$$

To solve this problem, one method which is usually utilized is the method of computing the pseudo-inverse of the matrix X as follows [25,31]:

$$\mathrm{pinv}(X) = (X^{\mathrm{T}}X)^{-1}X^{\mathrm{T}} \tag{20}$$

Then, the coefficients are calculated using:

$$A = \mathrm{pinv}(X) \cdot y \tag{21}$$

By minimizing the error using least square criterion, this method allows for proper identification of the model coefficients.

3 Performance Assessment of the Generalized Parallel Two-Box Predistorter Model

The flow chart summarizing the evaluation steps of power amplifier linearization using the generalized parallel two-box model based digital predistortion and indirect learning structure is presented in Fig. 5.

The performance assessment steps are classified into four parts: First, one behavioral model is proposed for the power amplifier modeling, and the coefficients of the model are identified using the least square (LS) method. Next, coefficients identification of the digital predistorter based on the generalized parallel two-box model using the indirect learning structure is carried out. In step III, the overall system (PA + DPD) is simulated. Finally, the performance of the proposed predistortion model is compared with the performance of other methods in some papers. A detailed description of each stage is presented below.

Fig. 5 Performance evaluation
steps of the power amplifier and
the proposed digital
predistortion model
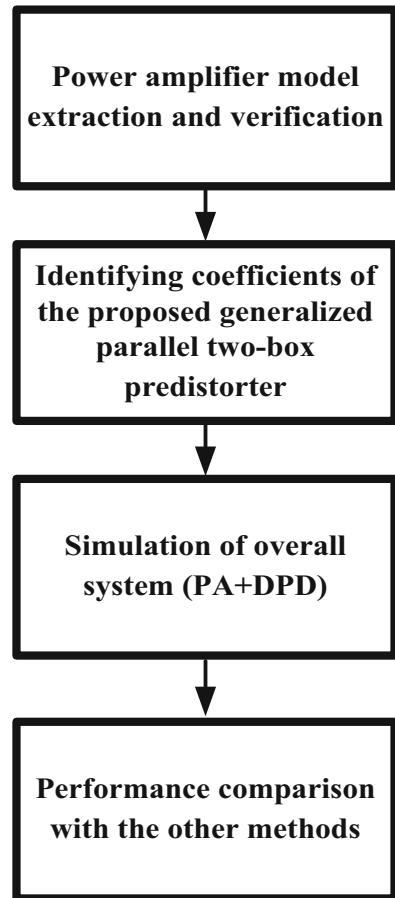
3.1 Power Amplifier Model Extraction and Verification

Before the proposed predistorter model is verified, the power amplifier must be modeled and simulated. For this reason, the memory polynomial function, which was fully described in the last section, has been proposed to model the highly nonlinear power amplifier. The main device under test (DUT), which is utilized in this work for the performance assessment of the proposed predistorter model, is a high power and efficient Doherty power amplifier based on laterally diffused metal oxide semiconductor (LDMOS) technology. The DUT has a maximum output power of 300 W and operates at about 2.1 GHz. It is driven by a 20 MHz signal which was sampled at 120 MHz. The baseband input and output waveforms of the device under test were acquired using the experimental setup described above. The baseband complex input and output data have been gathered in order to identify the coefficients of the memory polynomial model. The nonlinearity order and memory depth of Eq. (10) were set to $K = 20$ and $Q = 10$, respectively, in order to accurately model the power amplifier. Because
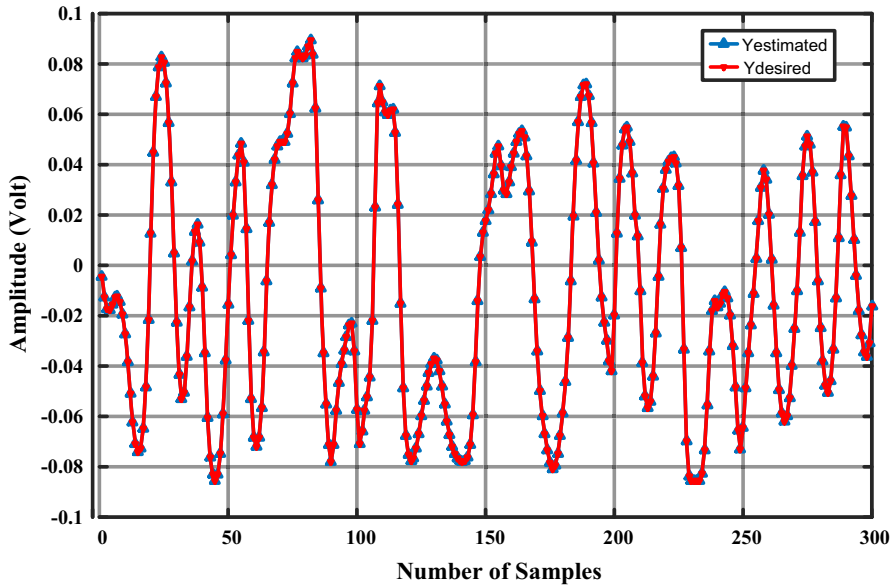
Fig. 6 The real output of the memory polynomial model and Doherty power amplifier

the power amplifier circuit will be utilized for real applications, the values of K and Q have been chosen to be very high in order to model the Doherty power amplifier accurately. The coefficients of the memory polynomial power amplifier model have been identified using the least square (LS) method described in the last section as well as the complex baseband input and data of the Doherty power amplifier.

For model performance evaluation in the time domain, the most straightforward method is to assess error in accordance with the difference between the desired and estimated output signal. The Normalized Mean Square Error (NMSE) is always employed for the performance assessment of behavioral model [10]. This criterion is often expressed in decibels and is defined as follows:

$$\text{NMSE} = 10 \log_{10} \left(\frac{\sum_{n=1}^{N} |y_{\text{desired}}(n) - y_{\text{estimated}}(n)|^2}{\sum_{n=1}^{N} |y_{\text{desired}}(n)|^2} \right) \tag{22}$$

where N denotes the number of samples, $y_{\text{desired}}(n)$ and $y_{\text{estimated}}(n)$. $y_{\text{desired}}(n)$ and $y_{\text{estimated}}(n)$ are the outputs of the power amplifier circuit and memory polynomial power amplifier model, respectively. It is obvious that a lower NMSE indicates superior model accuracy. In order to assess the identified coefficients of the memory polynomial model, the achieved coefficients are placed in the model. Then, the complex input signal is applied to the memory polynomial power amplifier model. The real and imaginary outputs, as well as the desired and estimated outputs of the Doherty power amplifier and memory polynomial model, are illustrated in Figs. 6 and 7, respectively.

It can be seen that the real and imaginary outputs of the memory polynomial power amplifier model have been precisely matched with those of the Doherty power amplifier
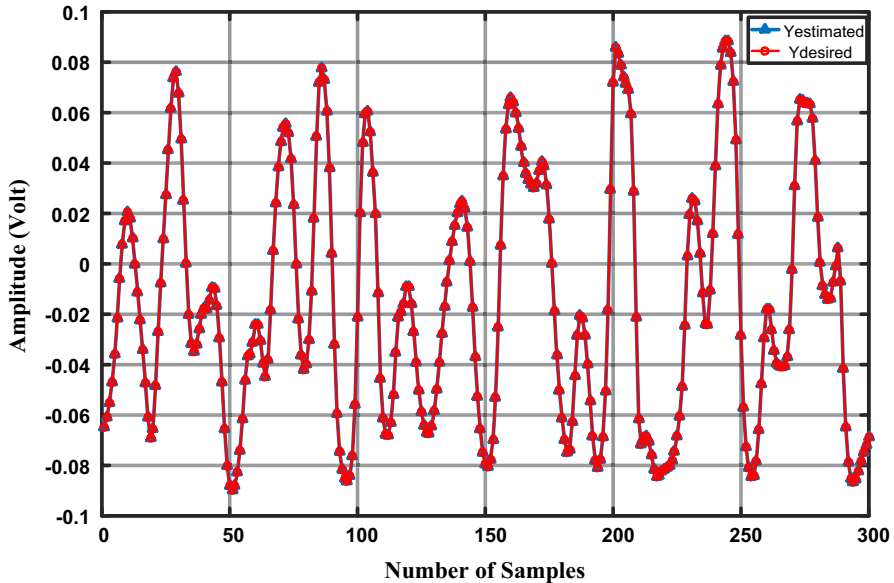
Fig. 7 The imaginary output of the memory polynomial model and Doherty power amplifier

model. The criterion of NMSE is -68.72 dB for this model verification. This NMSE means that the model extraction has been accurately carried out.

Another performance assessment metric is defined in the frequency domain. Since time domain signals are mainly dominated by the in-band components, a more accurate estimation of the model performance in the adjacent channels is required. For this reason and to further validate the accuracy of the memory polynomial model, the power spectrum density (PSD) of the Doherty power amplifier and memory polynomial power amplifier are plotted in Fig. 8.

It can also be concluded from Fig. 8 that the memory polynomial model accurately predicts the measured power spectrum density of the Doherty power amplifier. The output spectrum of the memory polynomial model is almost identical with that generated by the Doherty power amplifier. Therefore, the memory polynomial model accurately emulates both the linear and nonlinear memory effects of the Doherty power amplifier.

3.2 Identifying Coefficients of the Proposed Generalized Parallel Two-Box Predistorter

In order to linearize the power amplifier and eliminate its nonlinearity, the predistortion block which is accurately modeled by the proposed generalized parallel two-box model is placed upstream of the power amplifier. Indeed, the behavior of the predistortion block is ideally the inverse characteristics of the power amplifier. The proposed generalized parallel two-box model shown in the previous section is employed as a digital predistorter and the memory polynomial model is utilized as a power amplifier
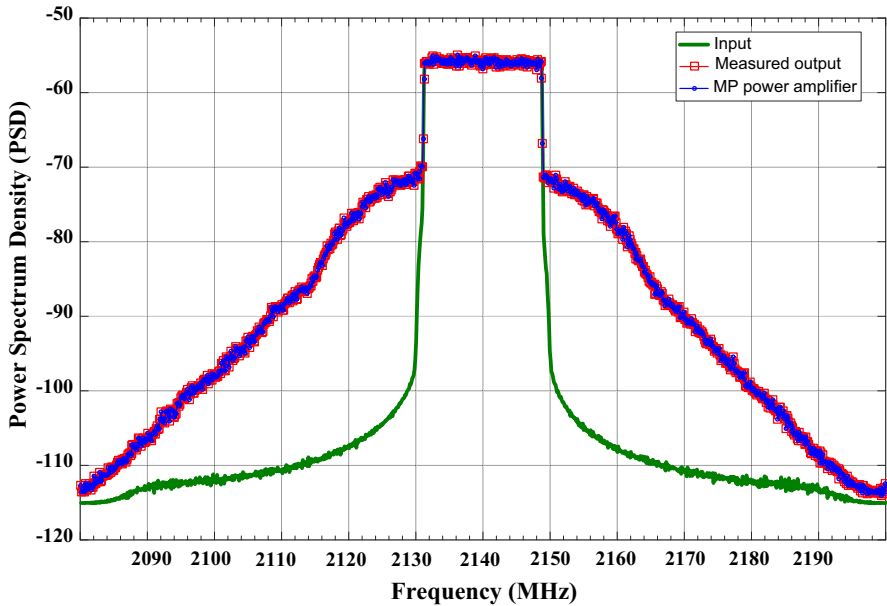
Fig. 8 Measured power spectrum density of Doherty power amplifier and simulated power spectrum density of memory polynomial power amplifier

model. The indirect learning structure employed for coefficients identification of the proposed predistortion is illustrated in Fig. 9. Actually, the indirect learning structure is a careful method in which a learning loop is closed around the power amplifier [3]. The input and output measurements of the Doherty power amplifier, which was described in the previous section, are utilized for extraction of the predistorter model. When the parameters of the predistortion in the learning loop are identified, this predistortion is then directly copied and employed as the predistortion block. The complex baseband input of the proposed predistorter is denoted by $x(n)$; the output of the predistorter and input of the power amplifier are denoted by $u(n)$, and the complex baseband output of the power amplifier is denoted by $y(n)$. To identify the coefficients of the proposed model, the predistorter block located in the upstream of the power amplifier is disconnected and the indirect learning loop is closed. The indirect learning loop includes the power amplifier, predistorter block, and estimation of parameters block.

When the input of the power amplifier and the output of the predistorter block in the feedback path are equal (and consequently an error term, i.e., $e(n) = u(n) - \hat{u}(n) \simeq 0$, is close to zero), the input and output of the system will be linear (i.e., $y(n) = Gx(n)$).

The coefficients of the proposed model have been identified by this structure. In this approach, when the error of energy $\|e(n)\|^2$ is minimum, the algorithm for finding the coefficients of the predistortion is fully converged. The identification method of the predistorter model is similar to the procedure that was clearly described in Sect. 2 by replacing the input of the predistorter with $y(n)/G$, where G is a small signal gain of the power amplifier and the output is $\hat{u}(n)$.
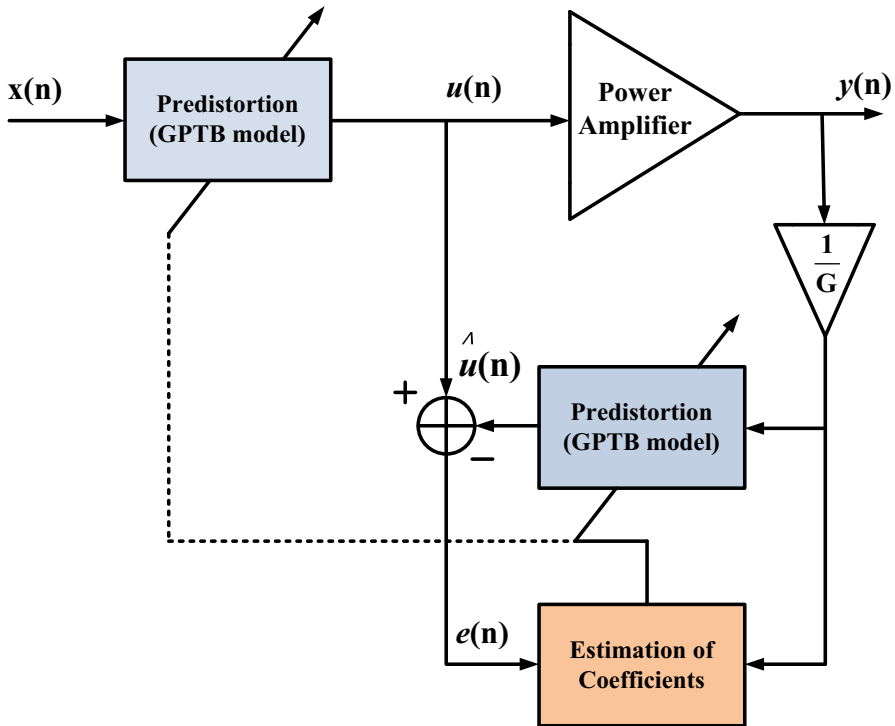
Fig. 9 Indirect learning structure

3.3 Simulation of the Overall System (Power Amplifier + Digital Predistortion)

3.3.1 Simulation of the Transmitter Without Digital Predistortion

The transmitter system depicted in Fig. 10 is designed and simulated for evaluating the modeled power amplifier and digital predistortion. The operation of the designed transmitter is described as follows.

First, the random bit generator module produces a bit sequence such that the probability of a zero and one bit is 0.5. Then, the complex symbol mapper groups consecutive bits into a 64QAM structure. The QAM signal is applied to a complex to the real and imaginary converter. This module converts complex input values to real and imaginary output values. This block reads one sample from the input and writes it to each of the real (Re) and imaginary (Im) outputs. The real and imaginary signals are applied to a raised cosine filter module. In the raised cosine filter block, each symbol is multiplied by a sinc function. Also, this block implements a resampler that uses a raised cosine filter as the interpolating filter. Then, the output signals of the raised cosine filter are applied to the modulator. The modulator module includes a mixer and combiner. This structure reads one sample from its inputs and writes the modulated sample in the high frequency to its output. The oscillator module has been employed in order to generate a signal with a frequency of 2.1 GHz. The power amplifier has an input and output
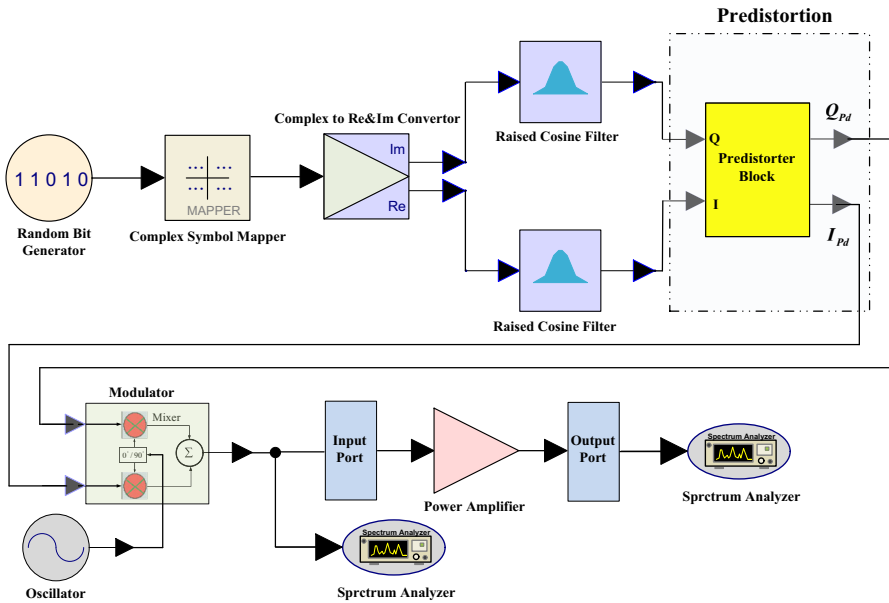
Fig. 10 Simulated transmitter system with and without predistortion

matching network specified in Fig. 10 as input and output ports. The modulated signal, i.e., 20 MHz signal, is applied to the modeled power amplifier. The power amplifier operates at a 2.1 GHz center frequency and its bandwidth is as high as 20 MHz.

In order to assess the power amplifier, the spectrum analyzer has been placed after the modulator and power amplifier. The spectrum analyzer measures the spectrum of a complex envelope signal. The power spectrum density (PSD) curves of the input and output of the power amplifier without using the digital predistortion are depicted in Fig. 11 at the operation frequency of 2.1 GHz and bandwidth of 20 MHz. It is clear that the sidelobe of the output spectrum of the power amplifier has been increased due to the nonlinearity of the power amplifier. The adjacent channel power ratio (ACPR) is commonly employed to quantify the nonlinearity that is generated by power amplifiers driven by modulated signals in the frequency domain. This is a significant linearity parameter since the power that is generated by the nonlinear distortions in the adjacent channels cannot be eliminated by filtering.

Therefore, the power generated in the adjacent channels is considered as an unwanted emission that needs to be minimized and controlled.

3.3.2 Simulation of the Transmitter with Digital Predistortion Based on the Generalized Parallel Two-Box Model

The schematic of the simulated transmitter with digital predistortion is depicted in Fig.10. The digital predistortion based on the generalized parallel two-box model is placed between the raised cosine filter block and modulator. In-phase and quadrature (I and Q) signals are applied to the predistortion block, and the signals are passed
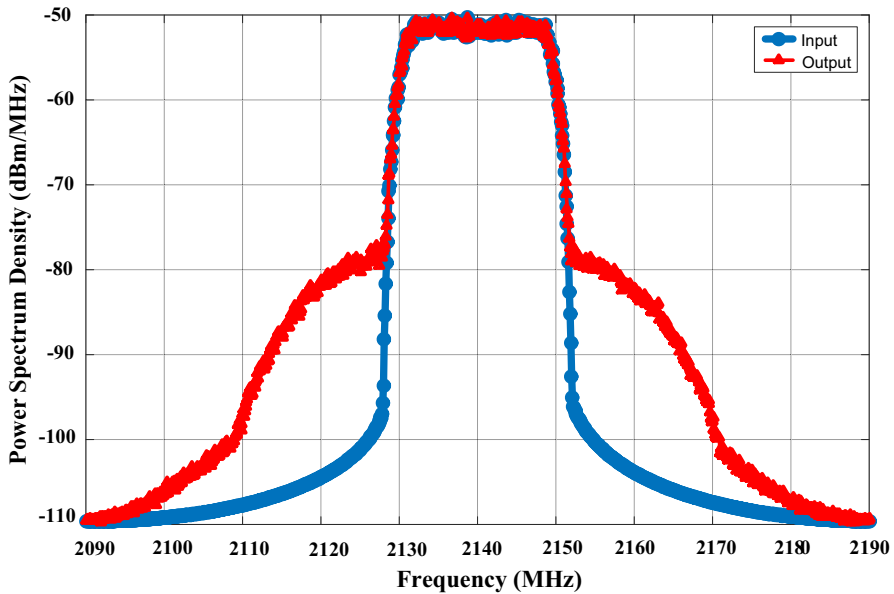
Fig. 11 Simulated input and output spectrum of the power amplifier without using digital predistorter at the center frequency of 2.1 GHz with bandwidth of 20 MHz

through the proposed predistorter model. When these signals are applied to the predistorter, they experience the static and dynamic nonlinearity of the model. Finally, the predistorted signals are applied to the modulator. The generalized parallel two-box model, which was clearly described in Sect. 2, has been employed for the predistorter block. The nonlinearity order, k, and memory depth, q, of the proposed model have been considered with normalized mean square error (NMSE) criterion. When the amounts of nonlinearity order and memory depth are $K_{MLP} = 10$, $M = 12$, $K = 3$, $M_e = 3$, and $K_e = 3$, the NMSE will be as small as possible. If the proposed amounts are greater than these values, the complexity of the model grows and a higher accuracy is not achieved. Using indirect learning structure, the coefficients of the proposed model are accurately identified.

Figure 12 illustrates the input signal spectrum of the power amplifier $X(n)$, the output signal spectrum of the nonlinear power amplifier and the output signal spectrum of the overall system (power amplifier + digital predistortion). It is very clear that the digital predistortion linearization method has compensated for the distortion of the power amplifier, and the spectral regrowth of the power amplifier is totally removed. The measure of adjacent channel power ratio (ACPR) is presented in Table 1. It is very clear that the ACPR of the power amplifier with digital predistortion has been improved to about 16 dB at the offset frequency of 15 MHz from the center frequency.
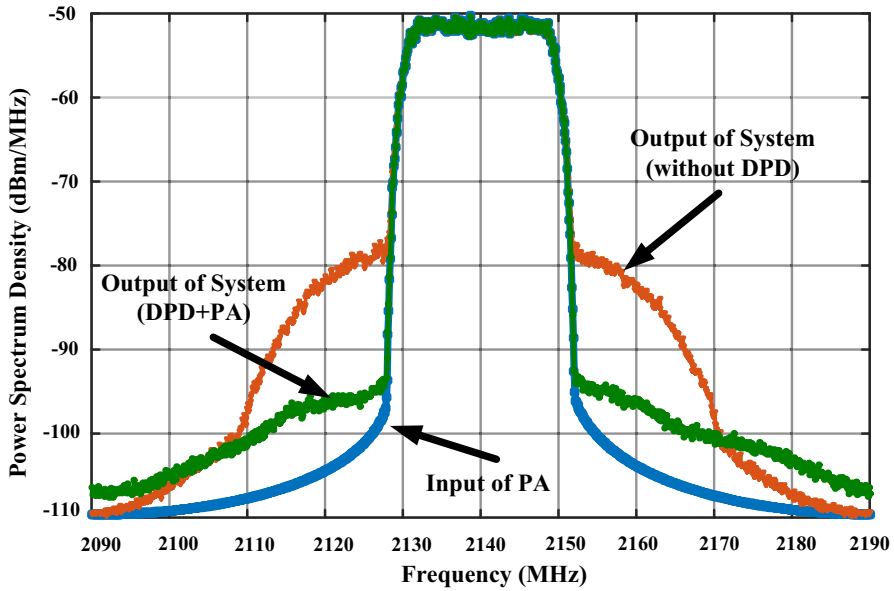
Fig. 12 Power amplifier input spectrum, power amplifier output spectrum without digital predistortion and system output spectrum which consists of the power amplifier and DPD

Table 1 ACPR for power amplifier with and without digital predistortion

	ACPR (dB)			
	$-15\,\mathrm{MHz}$	$+15\,\mathrm{MHz}$	$-25\,\mathrm{MHz}$	$+25\,\mathrm{MHz}$
Without DPD	-28	-29	-36	-36
With GPTB DPD	-44	-44	-46	-48

3.4 Performance Comparison with the Other Methods

In order to compare the proposed model, a memory polynomial model with nonlinearity order and memory depth of $K = 14$ and $M = 5$, respectively, has been chosen and placed in the predistorter model and simulated. The structure shown in Fig. 10 has been simulated twice with two models of the predistortion. First, the memory polynomial and then the proposed generalized parallel two-box model are accurately simulated. The values of the nonlinearity order and memory depth of the proposed model are chosen as $K = 12$, $M = 2$, $M_e = 3$, $K_e = 3$, and $K_{ML} = 10$. The power spectrum density of the simulated transmitter with memory polynomial and the proposed model for digital predistortion is illustrated in Fig. 13. It is obvious that the memory polynomial model could not accurately remove the nonlinear distortion of the power amplifier.

However, the proposed model accurately reduces the spectral regrowth of the power amplifier compared to the memory polynomial model. Because of the separation of
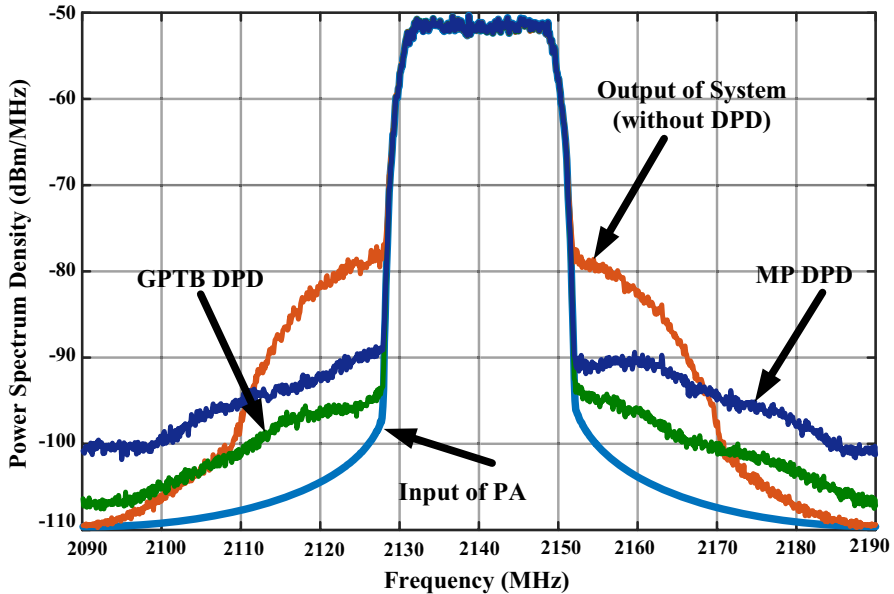
Fig. 13 Simulated power spectrum density of power amplifier input, power amplifier output without digital predistortion, power amplifier output with GPTB and MP digital predistortion spectrum which consists of the power amplifier and DPD

Table 2 The number of coefficients utilized in the proposed model and ACPR of the simulated power amplifier

	Number of coefficients	ACPR (dB)			
		$-15\,\text{MHz}$	$+15\,\text{MHz}$	$-25\,\text{MHz}$	$+25\,\text{MHz}$
MP DPD	$70\,(K = 14,\ M = 5)$	-38	-39	-41	-40
GPTB DPD	$55\,(K = 12,\ M = 2,\ M_e = 3,\ K_e = 3,\ K_{\text{ML}} = 10)$	-48	-46	-45	-48

the static and dynamic parts in the proposed model, the generalized parallel two-box model can effectively diminish the nonlinearity and memory effect of the power amplifier. The features of the proposed model in terms of complexity and accuracy are better than the memory polynomial model. The measure of the adjacent channel power ratio (ACPR) and the employed coefficients are shown in Table 2. The ACPR of the proposed model was improved to about 7 dB compared to the memory polynomial model. Although the utilized coefficients of the proposed model diminished by about 22%, the accuracy of the model in removing spectral regrowth was boosted.

In Table 3, the performance of the proposed predistortion model was compared with the performance of other methods in some papers. As presented in the table, the proposed predistorter model demonstrates a significant improvement in the removal of nonlinear memory effects and ACPR reduction. Obviously, the generalized parallel two-box model can eliminate some distortions generated by the power amplifier. As a

Table 3 Comparison of the performance of the proposed predistortion block with the performance of other methods

References	[8]	[15]	[30]	[20]	[33]	[5]	This work
Frequency	2.5 GHz	2.1 GHz	2–600 MHz	1.85 GHz	2.4 GHz	1.85 GHz	2.1 GHz
Bandwidth	20 MHz	5 MHz	–	5 MHz	2 MHz	5 MHz	20 MHz
Improvement in ACPR	8 dB	15 dB	5 dB	8 dB	5 dB	10 dB	16 dB
Linearization method	DPD	DPD	ADP	DPD	ADP	DPD	DPD

result, the power amplifier can work near its saturation operation point. In other words, the digital predistortion method in addition to improving linearity can enhance the efficiency of the power amplifier circuit. This proposed model (the predistorter model) can be efficiently implemented in real digital circuits, e.g., digital signal processor (DSP) chips and field programmable gate array (FPGA), because only standard structures, e.g., finite impulse response (FIR) filters, adder and multipliers, are employed.

4 Conclusions

This paper proposes the generalized parallel two-box (GPTB) structure for behavioral modeling and digital predistortion of nonlinear power amplifiers exhibiting memory effects. The proposed model includes two boxes, so that the first box emulates the static behavior of the power amplifier, while the second considers the memory effect of the nonlinear power amplifier. The coefficients identification of the proposed model was carried out using the indirect learning structure and the least square method. The proposed model was fully assessed through simulation of the transmitter excited by the 20 MHz 64QAM signal in advanced design system (ADS) software. Simulation results showed that the ability of the proposed model to obtain better performance than the conventional memory polynomial model with complexity reduction was about 22%. Also, the proposed model showed superior performance in suppressing spectral regrowth than the other linearization methods.

References

1. A.R. Belabad, N. Masoumi, S.J. Ashtiani, A fully integrated 2.4 GHz CMOS high power amplifier using parallel class A&B power amplifier and power-combining transformer for WiMAX application. AEU Int. J. Electron. Commun. **67**(12), 1030–1037 (2013)
2. A.R. Belabad, E. Iranpour, S. Sharifian, FPGA implementation of a Hammerstein based digital predistorter for linearizing RF power amplifiers with memory effects. Amirkabir Int. J. Electr. Electron. Eng. **47**(2), 9–17 (2015)
3. A.R. Belabad, S.A. Motamedi, S. Sharifian, An adaptive digital predistortion for compensating nonlinear distortions in RF power amplifier with memory effects. Integr. VLSI J. **57**, 187–191 (2017)
4. J. Cha, J. Yi, J. Kim, B. Kim, Optimum design of a predistortion RF power amplifier for multicarrier WCDMA applications. IEEE Trans. Microw. Theory Tech. **52**(2), 655–663 (2004)
5. Y. Cho, J. Lee, S. Jin, B. Park, J. Moon, J. Kim, B. Kim, Fully integrated CMOS saturated power amplifier with simple digital predistortion. IEEE Microw. Wirel. Compon. Lett. **24**(8), 533–535 (2014)
6. D. Chowdhury, C.D. Hul, O.B. Degan, Y. Wang, A.M. Niknejad, A fully integrated dual-mode highly linear 2.4 GHz CMOS power amplifier for 4G WiMAX applications. IEEE J. Solid-State Circuits **44**(12), 3393–3402 (2009)
7. L. Ding, G.T. Zhou, D.R. Morgan, Z. Ma, J.S. Kenney, J. Kim, C.R. Giardina, A robust digital baseband predistorter constructed using memory polynomials. IEEE Trans. Commun. **52**(1), 159–165 (2004)
8. M. Garcia-Hernandez, A. Prieto-Guerrero, G. Laguna-Sanchez, P.J. Mendoza-Valencia, J. Sanchez-Garcia, Digital predistorter based on Volterra series for nonlinear power amplifier applied to OFDM systems using adaptive algorithms. Int. Meet. Electr. Eng. Res. **35**, 118–125 (2012)
9. F.M. Ghannouchi, O. Hammi, Behavioral modeling, and predistortion. IEEE Microw. Mag. **10**(7), 52–64 (2009)
10. F.M. Ghannouchi, O. Hammi, M. Helaoui, *Behavioral Modeling and Predistortion of the Wideband Wireless Transmitter* (Wiley, New York, 2015)
11. L. Guan, A. Zhu, Low-cost FPGA implementation of Volterra series-based digital predistorter for RF power amplifiers. IEEE Trans. Microw. Theory Tech. **58**(4), 866–872 (2010)

12. O. Hammi, F.M. Ghannouchi, Twin nonlinear two-box models for power amplifiers and transmitters exhibiting memory effects with application to digital predistortion. IEEE Micro. Wireless Compon. Lett. **19**(8), 530–532 (2009)

13. O. Hammi, M. Younes, F.M. Ghannouchi, Metrics and methods for benchmarking of RF transmitter behavioral models with application to the development of a hybrid memory polynomial model. IEEE Trans. Broadcast. **56**(3), 350–357 (2010)

14. S. Jung, H. Park, M. Kim, G. Ahn, J. Van, H. Hwangbo, C. Park, S. Park, Y. Yang, A new envelope predistorter with envelope delay taps for memory effect compensation. IEEE Trans. Microw. Theory Tech. **55**(1), 52–59 (2007)

15. G. Karimi, A. Lotfi, An analog/digital pre-distorter using particle swarm optimization for RF power amplifiers. AEU Int. J. Electron. Commun. **67**, 723–728 (2013)

16. J.S. Kenney, W. Woo, L. Ding, R. Raich, H. Ku, G.T. Zhou, The impact of memory effects on predistortion linearization of RF power amplifiers, in *Proceedings of the 8th International Microwave Optical Technology Symposium*, pp. 189–19 (2001)

17. J. Kim, K. Konstantinou, Digital predistortion of wideband signals based on power amplifier model with memory. Electron. Lett. **37**(23), 1417–1418 (2001)

18. K. Lim, G. Ahn, S. Jung, H. Park, M. Kim, J. Van, H. Cho, J. Jeong, C. Park, Y. Yang, A 60 watt multicarrier WCDMA power amplifier using an RF predistorter. IEEE Trans. Circuits Syst. II Exp. Briefs. **59**(4), 265–269 (2009)

19. T. Liu, S. Boumaiza, F.M. Ghannouchi, Deembedding static nonlinearities and accurately identifying and modeling memory effects in wide-band RF transmitters. IEEE Trans. Microw. Theory Tech. **53**(11), 3578–3587 (2005)

20. T. Liu, S. Boumaiza, F.M. Ghannouchi, Augmented Hammerstein predistorter for linearization of broad-band wireless transmitters. IEEE Trans. Microw. Theory Tech. **54**(4), 1340–1349 (2006)

21. R. Marsalek, Contributions to the power amplifier linearization using digital baseband adaptive predistortion. Ph.D. dissertation, Universite de Marne La Vallee, 2003

22. J. Moon, B. Kim, Enhanced Hammerstein behavioral model for broadband wireless transmitters. IEEE Trans. Microw. Theory Tech. **56**(4), 924–9933 (2011)

23. K.J. Muhonen, M. Kavehrad, R. Krishnamoorthy, Look-up table techniques for adaptive digital predistortion: a development and comparison. IEEE Trans. Veh. Technol. **49**(9), 1995–2002 (2000)

24. T. Nojima, T. Konno, Cuber predistortion linearizer for relay equipment in 800 MHz band land mobile telephone system. EEE Trans. Veh. Technol. **34**(4), 169–177 (1985)

25. R. Penrose, A generalized inverse for matrices, in *Proceedings the Cambridge Philosophical Society* (1995), pp. 406–413

26. H. Qian, H. Huang, S. Yao, A general adaptive digital predistortion architecture for stand-alone RF power amplifiers. IEEE Trans. Broadcast. **59**(3), 528–538 (2013)

27. B. Razavi, *RF Microelectronics*, 2nd edn. (Prentice Hall, Upper Saddle River, 2011)

28. M. Schetzen, *The Volterra & Wiener Theories of Nonlinear Systems* (Wiley, New York, 1989)

29. R. Schumacher, E.G. Lima, G.H.C. Oliveira, RF power amplifier behavioral modeling based on Takenaka–Malmquist–Volterra series. Circuits Syst. Signal Process. **35**, 2298–2316 (2016)

30. M. Seo, K. Kim, M. Kim, H. Kim, J. Jeon, M. Park, H. Lim, Y. Yang, Ultrabroadband linear power amplifier using a frequency-selective analog predistorter. IEEE Trans. Circuits Syst. II Exp. Briefs. **58**(5), 264–268 (2011)

31. J. Stoer, R. Bulirsch, *Introduction to Numerical Analysis* (Springer, Berlin, 2002)

32. K. Yamauchi, K. Mori, M. Nakayama, Y. Mitsui, T. Takagi, A microwave miniaturized linearizer using a parallel diode, in *Proceedings IEEE MTT-S Intemational Microwave Symposium Digest*, pp 1199–1202 (1997)

33. C. Yen, H. Chuang, A 0.25-μm 20-dBm 2.4-GHz CMOS power amplifier with an integrated diode linearizer. IEEE Microw. Wirel. Compon. Lett. **13**(2), 45–47 (2003)

34. J. Yi, Y. Yang, M.G. Park, W.W. Kang, B. Kim, Analog predistortion linearizer for high-power RF amplifiers. IEEE Trans. Microw. Theory Tech. **48**(12), 2709–2713 (2000)

35. M. Younes, F.M. Ghannouchi, An accurate predistorter based on a feedforward Hammerstein structure. IEEE Trans. Broadcast. **58**(3), 454–461 (2012)