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A High-Efficiency CMOS Rectifier with Wide Harvesting Range and Wide Band Based on MPPT Technique for Low-Power IoT System Applications

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Abstract This paper describes a wide-harvesting-range, wide band, and high-efficiency complementary metal-oxide-semiconductor (CMOS) rectifier for low-power application in internet of things systems. Through maximum power point tracking, the proposed rectifier can dynamically detect the output voltage to enable switching between various circuit modes in order to achieve higher power conversion efficiency (PCE), even during sub-1-V operation. The experimental results for a 0.18-μm standard CMOS process with a 1.8-V power supply voltage demonstrate that the proposed rectifier can operate from a low voltage (0.7 V) to a high voltage (1.8 V) while maintaining high PCE. The proposed rectifier achieves a PCE improvement of 16% from the rectifier with a bootstrapping circuit under a peak alternating current (AC) input voltage of 0.85 V, and of 47.5% from the fully cross-coupled rectifier under a 1.8-V peak AC input voltage. Moreover, because its structure is insensitivity to the frequency response, the proposed rectifier provides a wide operating frequency range of 10–960 MHz.

Keywords High efficiency · Wide harvesting range · Wide band · MPPT technique · Rectifier · Internet of things (IoT)

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1 Introduction

With the continuing development of wireless technology and commercial electronic devices, the internet of things (IoT) has become a technological trend that enables ordinary objects capable of exercising independent functions to implement interoperable networks. Cisco is expected to have an IoT market worth US$ 19 trillion within the next decade [14], and analysts have predicted that IoT applications will connect 36 billion devices by 2020 [32]. Energy harvesting plays a key role in IoT applications. Compared with thermal, photovoltaic (PV) [2], and piezoelectric energy harvesting technologies [22,33], radio frequency (RF) energy harvesting is more suitable for use in low-power, low-cost IoT systems such as wireless sensor platforms [1,5,13,19,24,27–29]. As shown in Fig. 1, the working principle of an energy harvester for low-power IoT system applications entails the transmission of an RF alternating current (AC) signal to a near-field coupling coil using a power transmitter and its conversion using a rectifier. The AC signal received by the coupling coil is converted to direct current (DC) power supply and used in a load system that is input to a low-dropout regulator (LDO) to produce a stable DC supply.

In the standard CMOS process, the diodes are generally easily replaced by the diode-connected MOS. However, this architecture is affected by the threshold voltage (V_{TH}), and the instantaneous voltage change through transistor-based switches caused by channel resistance results in the reduction in the output voltage, which in turn affects the overall power conversion efficiency (PCE) [15]. Therefore, many rectifier architectures, such as the gate cross-coupled rectifier (GCCR) [31], fully cross-coupled rectifier (FCCR) [3,6,9], rectifier with unbalanced-biased comparators (RUBC) [8], and rectifier with bootstrapping circuit (RBC) [11,26], have been proposed.

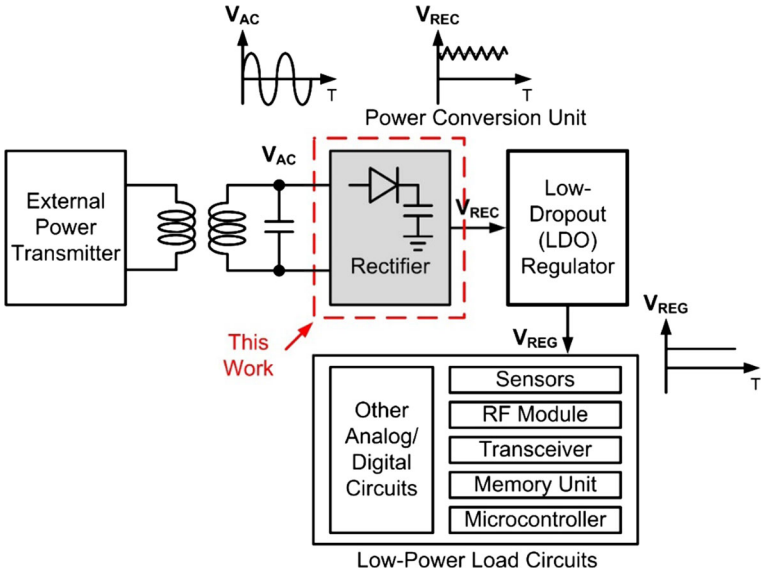


Fig. 1 Block diagram of an energy harvester for use in low-power IoT system

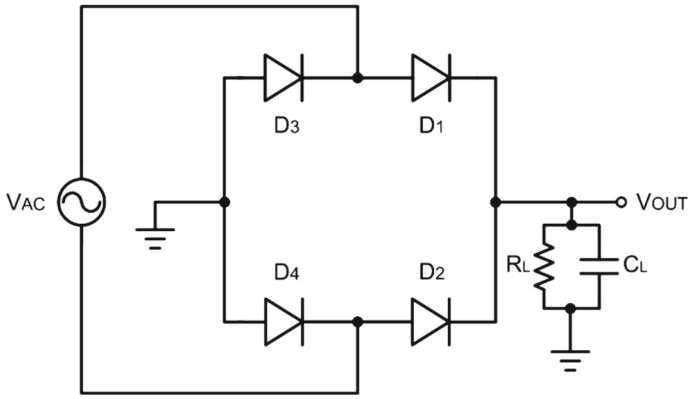


Fig. 2 Full-wave bridge rectifier (FWBR)

The remainder of this paper is organized as follows: Sect. 2 discusses the architecture and characteristics of conventional rectifier topologies. Section 3 presents the proposed rectifier topology based on maximum power point tracking (MPPT) and describes its circuit. Section 4 presents the experimental results of the proposed rectifier and compares it with those of other topologies. Concluding remarks are provided in Sect. 5.

2 Analyses and Comparisons of Conventional Rectifiers

The full-wave bridge rectifier (FWBR) is one of the most common rectifier structures and the most widely implemented full-wave rectifier structure, as shown in Fig. 2. Compared with half-wave rectifiers, it exhibits higher power conversion and lower ripple voltages [31]. The FWBR consists of four diodes and does not require a center-tapped transformer. Because diodes connected to the load are used, a difference is generated between the output voltage (V_{OUT}) and AC input voltage (V_{AC}) for the V_{TH} values of these two diodes.

The GCCR [31] implements the full-wave rectifier with all MOS transistors, as shown in Fig. 3. The GCCR and FWBR differ in that two diodes in the GCCR are replaced by N-type MOS (NMOS)-based switches M_3 and M_4, and the NMOS gate is connected directly to the signal source to obtain a greater voltage swing, thereby enabling the transistor to instantaneously switch between the cutoff and linear regions. Therefore, the favorable transmission characteristics of the low voltage potential in the NMOS-based switch can effectively reduce the output voltage loss caused by the threshold voltage, resulting in higher PCE. However, the GCCR uses diode-connected p-channel MOS (PMOS) switches M_1 and M_2 connected to the load, resulting in a variation in the output voltage and AC input voltage for the V_{TH} of one diode. In low-voltage operation, the voltage conversion efficiency (VCE) degrades considerably because of the V_{TH}, thereby directly affecting the PCE. The V_{OUT}, VCE, and PCE are defined as:

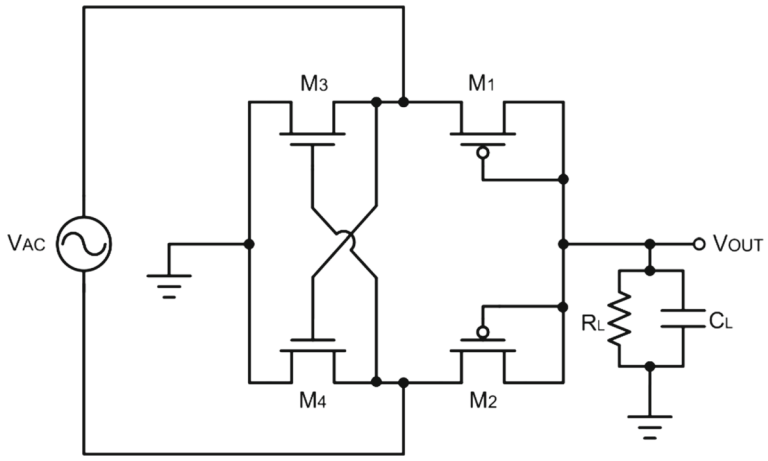


Fig. 3 Gate cross-coupled rectifier (GCCR)

$$V_{\mathrm{OUT}} = V_{\mathrm{AC}} - V_{\mathrm{TH}} \tag{1}$$

$$\mathrm{VCE} = \frac{V_{\mathrm{OUT}}}{V_{\mathrm{AC}}} \times 100\% = \frac{V_{\mathrm{AC}} - V_{\mathrm{TH}}}{V_{\mathrm{AC}}} \times 100\% \tag{2}$$

$$\mathrm{PCE} = \frac{P_{\mathrm{RL}}}{P_{\mathrm{IN}}} \times 100\% = \frac{V_{\mathrm{OUT}} \times I_{\mathrm{RL}}}{P_{\mathrm{IN}}} \times 100\% \tag{3}$$

where P_{RL} is the power consumed by the load, P_{IN} is the total power input, and I_{RL} is the current flowing through the load.

The FCCR [6] differs from the GCCR in that it contains four MOS-based switches ($M_1 - M_4$) in the two main branches, and each gate is cross-connected to the other input signal, as shown in Fig. 4a. In contrast to the GCCR, the FCCR circuit solves the problem caused by the output drop by using a full-switch form. However, it cannot achieve high PCE in an operation over a wide voltage range because it experiences reverse current on PMOS transistors M_1 and M_2 [9], as shown in Fig. 4b. To reduce the difference between the input and output instantaneous voltages in order to suppress the occurrence of reverse current, relative coupling capacitances C_{C1} and C_{C2} are required during high-voltage operation for achieving high conversion efficiency. Therefore, using reverse current to charge the coupling capacitance improves the input DC level.

Notably, on adjusting the size and the corresponding coupling capacitance, the FCCR yields different peaks in the PCE characteristic curve, as shown in Fig. 5. The simulation results all have shunt loads of $C_{\mathrm{L}} = 400\,\mathrm{pF}$ and $R_{\mathrm{L}} = 70\,\Omega$ under various AC input voltages. Consequently, increasing the size of all transistors to enhance the current drive capability, which in turn increases the output load voltage, is essential for achieving the ideal PCE peak in low-voltage operation. Because the input signal is small and the output voltage is relatively low in the FCCR, the problem of reverse current is not too concerning and thus no coupling capacitance aid is required. By contrast, obtaining the ideal PCE peak in high-voltage operation does not require an

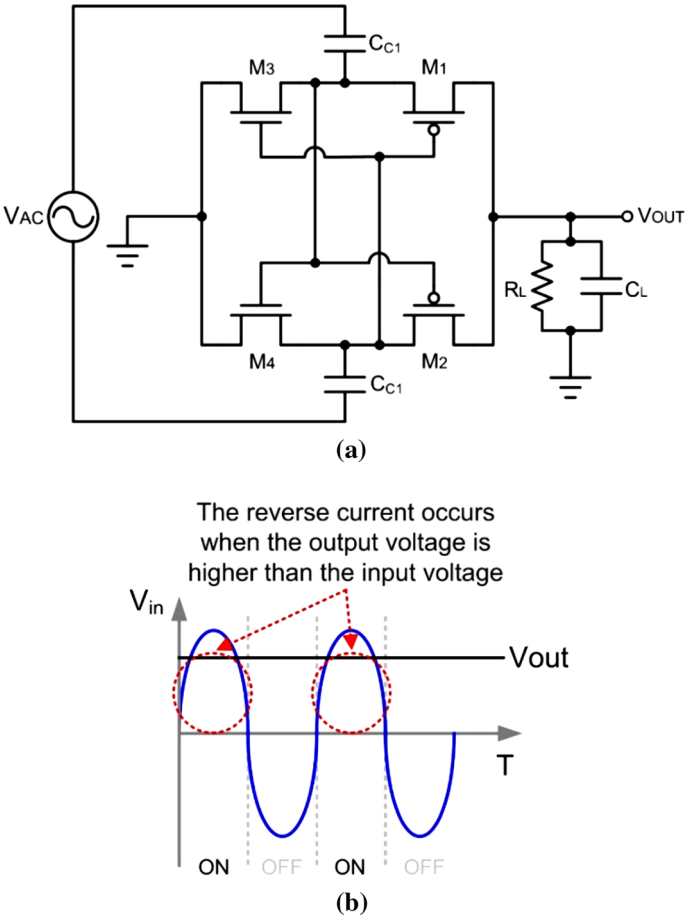


Fig. 4 **a** Full cross-coupled rectifier (FCCR). **b** Condition of the reverse current on PMOS transistors M_1 and M_2

extremely large transistor size to enhance drive capability, but does require auxiliary coupling capacitance to avoid excessive reverse current.

As shown in Fig. 6, the RUBC [8] is based on the FCCR, with the only difference being that the RUBC contains two PMOS transistors controlled by two unbalanced-biased comparators that enable the circuit to more precisely control the switching behavior. Power PMOS transistors M_1 and M_2 are switched on only when the moment input voltage is higher than the output voltage, thereby effectively preventing reverse current without coupling capacitance. Therefore, the RUBC occupies a smaller area but achieves higher PCE performance than does the FCCR when the operation voltage is high. The RUBC exhibits good PCE character curves in high-voltage operation; however, as a trade-off for the high conversion efficiency, the two unbalanced-biased comparators require a certain degree of input voltage drive to operate normally; thus, achieving high efficiency in low-voltage operation is a substantial challenge for the RUBC.

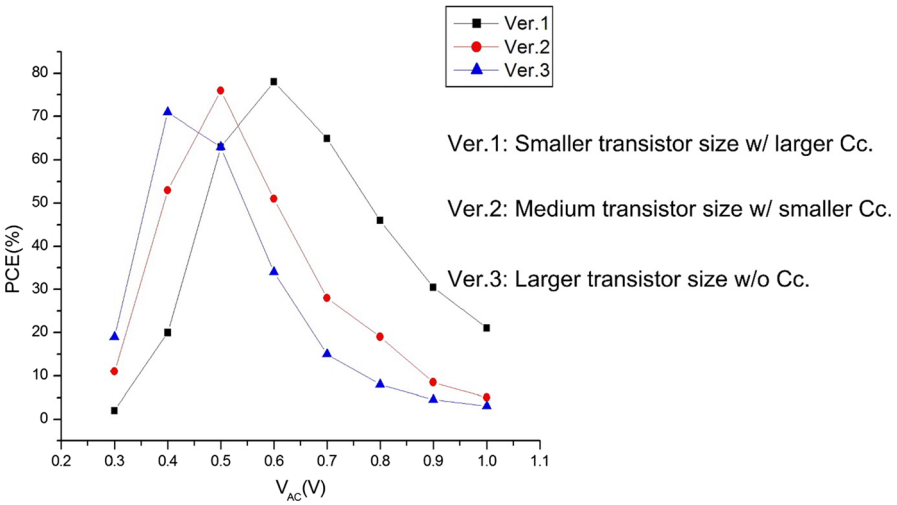


Fig. 5 Simulation results for FCCR under various PCE characteristic curves

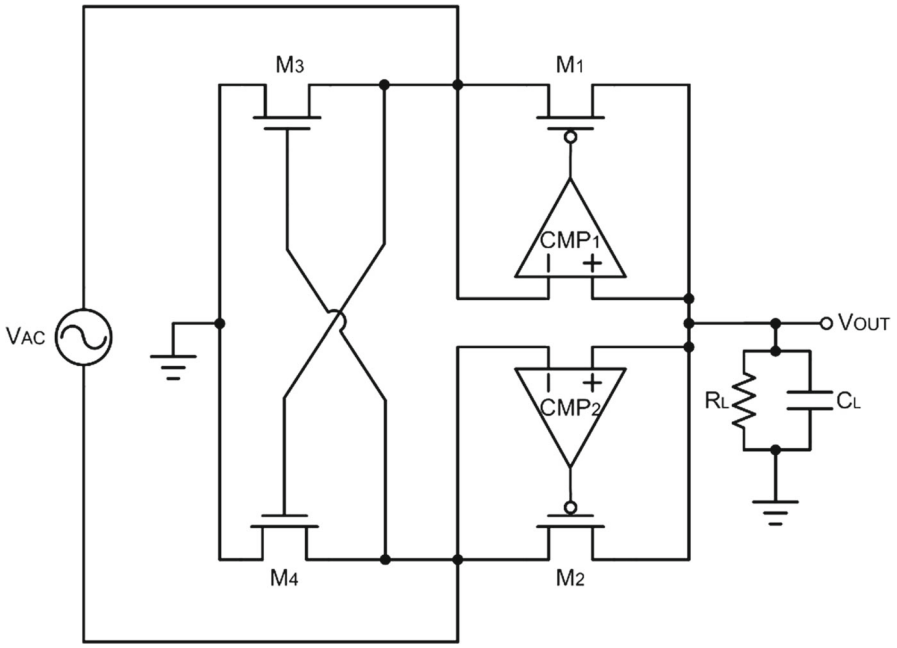


Fig. 6 Rectifier with unbalanced-biased comparators (RUBC)

In most rectifier topologies, the V_{TH} of components decreases the conversion efficiency in low-voltage operation. Only the FCCR can achieve optimal conversion; however, it cannot maintain high PCE over a wide input voltage range because of reverse current. As shown in Fig. 7, the RBC [11,26] uses bootstrapping diodes M_1, M_5, M_7, and C_1 and M_2, M_6, M_8, and C_2 with V_{TH} values lower than those of the

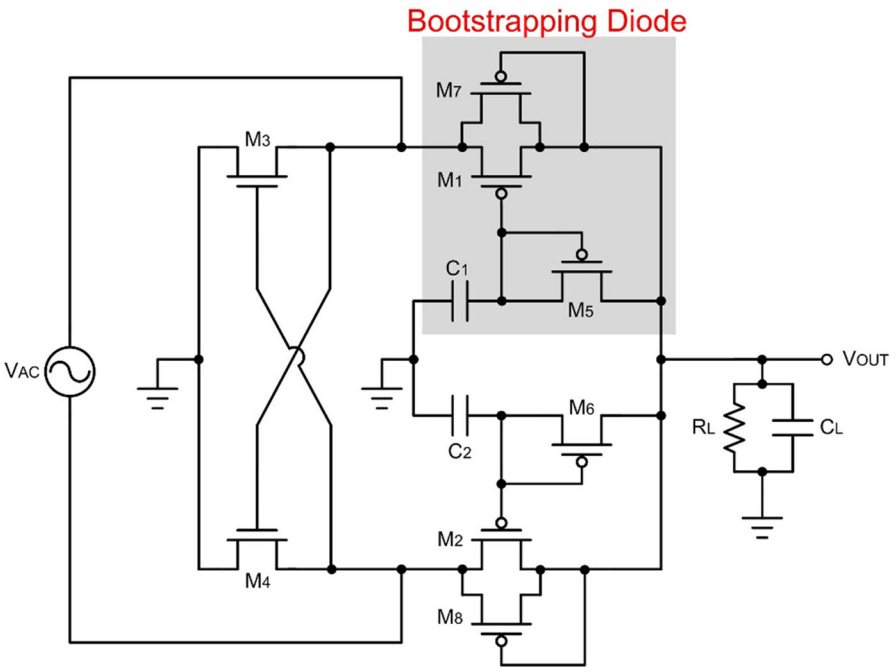


Fig. 7 Rectifier with bootstrapping circuit (RBC)

diode-connected MOS connected to the load in order to obtain higher VCE and more favorable PCE curves. Therefore, the RBC has the potential to mitigate the problems of low voltage input and a wide input voltage range.

In Eq. (4), in contrast to the conventional diode-connected PMOS structure, the effective $V_{\mathrm{TH}}(V'_{\mathrm{TH}})$ of the circuit is reduced. Thus, reducing the V'_{TH} of a standard MOS transistor can increase the output voltage range for an input source voltage:

$$V_{\mathrm{OUT}} = V_{\mathrm{AC}} - V'_{\mathrm{TH}} = V_{\mathrm{AC}} - (|V_{\mathrm{TH1}}| - V_{\mathrm{TH5}}) \tag{4}$$

where the V_{TH} values of MOS transistors $M_1(V_{\mathrm{TH1}})$ and $M_5(V_{\mathrm{TH5}})$ are equal to those of MOS transistors $M_2(V_{\mathrm{TH2}})$ and M_6 (V_{TH6}), respectively.

Figure 8 shows the PCE characteristic curves for the GCCR, FCCR, RUBC, and RBC at the same power transistor size and under a shunt load of $C_{\mathrm{L}} = 400\,\mathrm{pF}$ and $\mathrm{R_L} = 70\,\Omega$. Evidently, the RBC is an evolved version of the GCCR, but it is not as efficient as the FCCR is in low-voltage operation or the RUBC is in high-voltage operation.

Table 1 and the aforementioned description and figures illustrate the advantages and disadvantages of various rectifier topologies and their appropriate operating conditions. In recent years, more and more MPPT techniques are used in the energy harvesting circuits to enhance efficiency [4,23,25,33]. Therefore, this study combines the advantages of the FCCR [6] and RBC [11] with the concept of MPPT technique. Through dynamic sensing, the various output voltage conditions required to switch

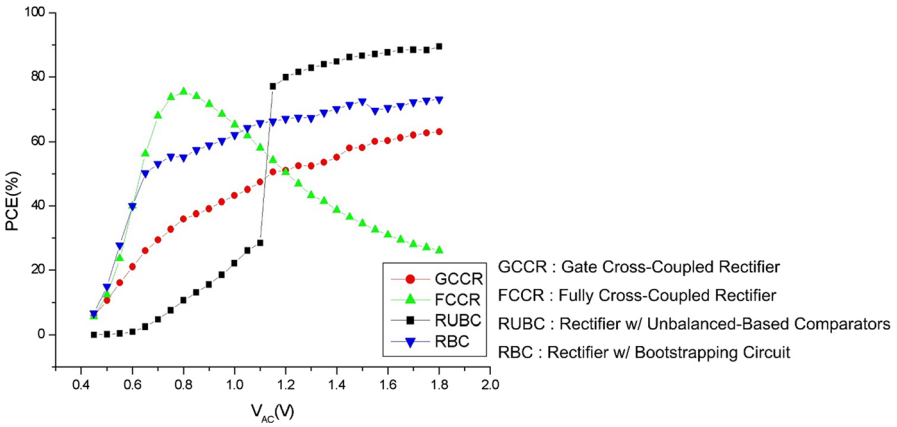


Fig. 8 PCE curves for GCCR, FCCR, RUBC, and RBC

Table 1 Feature comparison of various topology rectifiers

Reference	[31]	[6]	[8]	[11]
Rectifier topology	GCCR	FCCR	RUBC	RBC
Low input voltage	X	V	X	O
Wide input voltage range	V	X	O	V
Wide band	V	V	X	V
High-frequency operation	V	V	X	V
High efficiency	O	V	V	V

V: good; O: average; X: poor

to the most suitable circuit operation mode at any time were obtained to effectively enhance the input voltage range and operating bandwidth and upgrade the overall PCE under different input conditions in correlation with the many system specifications, thereby achieving the goals of low input voltage, wide harvesting range, wide band, and high efficiency.

3 Design of the Proposed Rectifier

As shown in Fig. 8, among the analyzed topology rectifiers, the FCCR exhibits the best PCE performance for low-voltage operation, and it does not require coupling capacitances (Ver. 3 of Fig. 5), thereby greatly reducing the required chip area. In addition, because the FCCR directly controls the MOS switches from the signal input, the PCE characteristic is almost completely unaffected by the different frequency. Therefore, the FCCR is the preferred circuit for low-voltage and wide-frequency operation. For high-voltage operation, the PCE characteristic of the RUBC is the best. However, the use of comparators results in significant degradation of the PCE curve of the RUBC

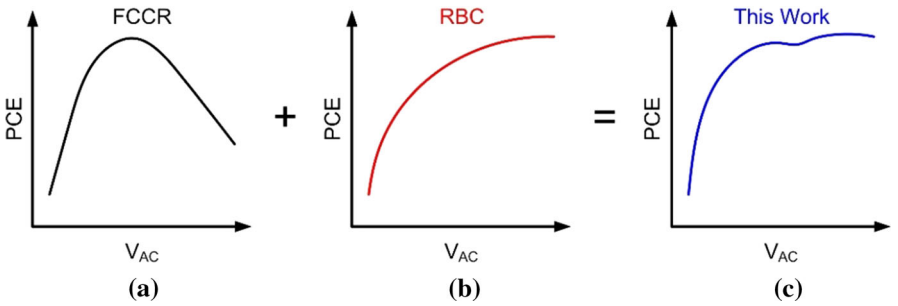


Fig. 9 Efficiencies of the conventional rectifier **a** FCCR and **b** RBC and **c** the PCE of the proposed rectifier

in high-frequency operation. Therefore, the RUBC exhibits lower performance than does the RBC in relatively high-frequency operation.

To achieve maximum PCE under various operating voltages and frequencies, this paper proposes an MPPT-based structure with a wide harvesting range, wide band, and high efficiency. Figure 9 shows the basic concepts used in this work. The proposed rectifier is controlled by a dynamic output voltage detector (DOVD) that combines the advantages of the FCCR in low-voltage operation as shown in Fig. 9a and the RBC in high-voltage operation as shown in Fig. 9b. Figure 9c shows the proposed rectifier is extended by combining both curves in Fig. 9a, b. Because of its compact architecture, the proposed rectifier can reduce the parasitic effects of internal and external nodes and remain unaffected by the variation in input frequency. Therefore, the proposed rectifier can maintain high PCE in both low-voltage operation and high-voltage operation.

Figure 10a shows a concept diagram of the wide-input-voltage-range CMOS rectifier with DOVD, where the power transistor MOS $M_1 - M_4$ is the main path transistor, and all the power transistor MOS operate at linear region as switches with low on-resistance as Eq. 5. As a result, it can reduce voltage drops to achieve higher voltage conversion ratio. When the AC input signal is insufficiently high, V_{OUT} is relatively low. Consequently, the DOVD provides diode-connected PMOS M_6 with a path to ground to send output power transistor PMOS M_5 into the linear region as a switch (Fig. 10b), resulting in the FCCR circuit mode for low-voltage operation achieving a high PCE without coupling capacitance. Thus, the V_{OUT} of FCCR mode is given by Eq. 6. By contrast, when the V_{OUT} is relatively high, the DOVD V_{OUT} (V_{DO}) follows the rectifier V_{OUT} (Fig. 10c), resulting in the RBC circuit mode, and the V_{OUT} can be rewritten as Eq. 7. In high-voltage operation, the circuit output connects to a bootstrapping diode that can effectively block reverse current with only a tiny voltage dropout due to the V_{TH} of the bootstrapping diode in Eq. (4). Therefore, this circuit can achieve a higher VCE and thus a higher PCE.

$$R_{\mathrm{on}} = \frac{V_{\mathrm{DS}}}{I_D} = \frac{L}{\mu_n C_{\mathrm{OX}} W V_{\mathrm{OV}}} \tag{5}$$

$$V_{\mathrm{OUT}} = V_{\mathrm{AC}} \times \frac{R_L}{R_{\mathrm{on,M_{1/2}}} + R_{\mathrm{on,M_{3/4}}} + R_{\mathrm{on,M_5}} + R_L} \tag{6}$$

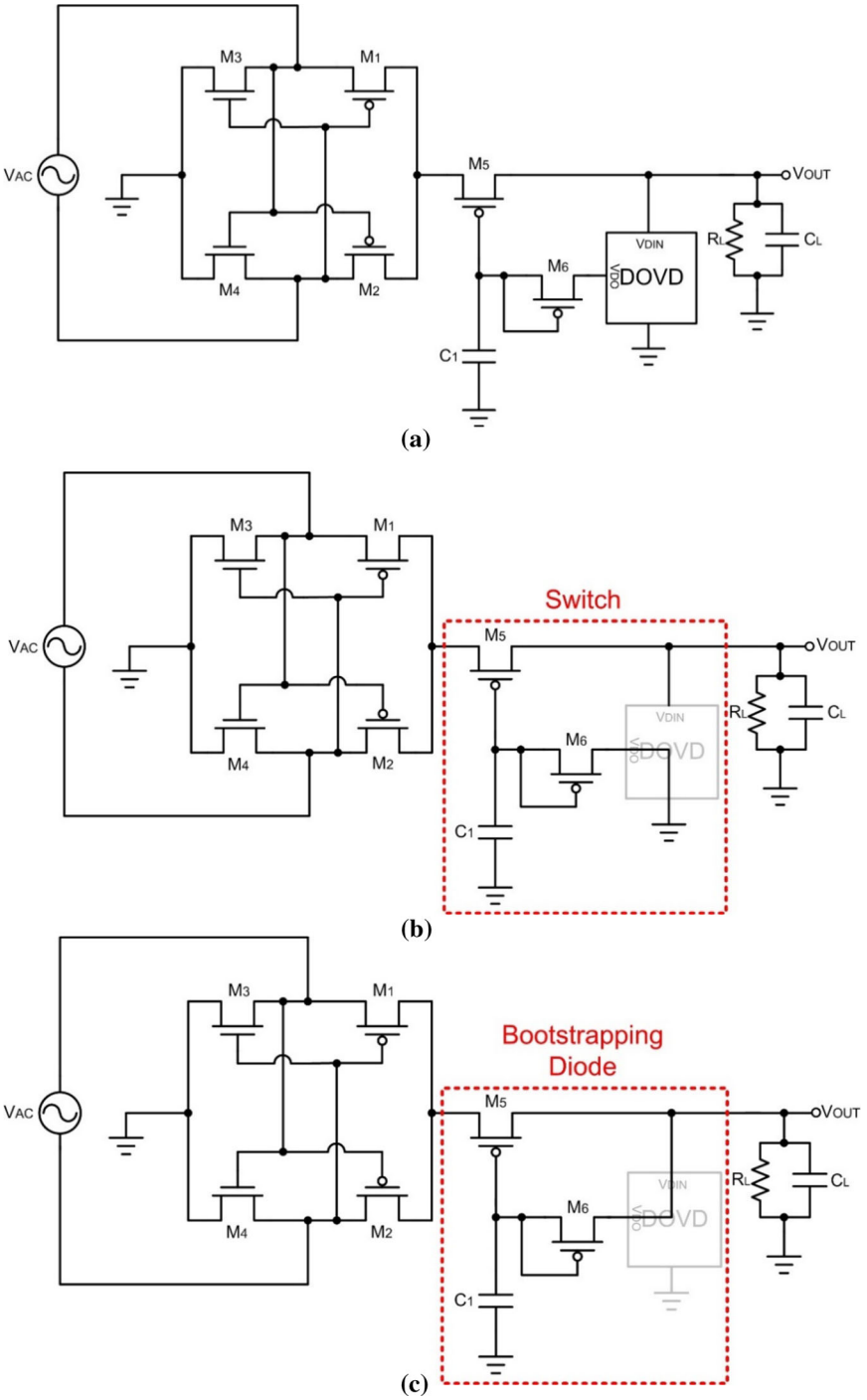


Fig. 10 **a** Concept diagram of wide-input-voltage-range CMOS rectifier with DOVD; **b** operating principle under low voltage as FCCR mode; **c** operating principle under high voltage as RBC mode

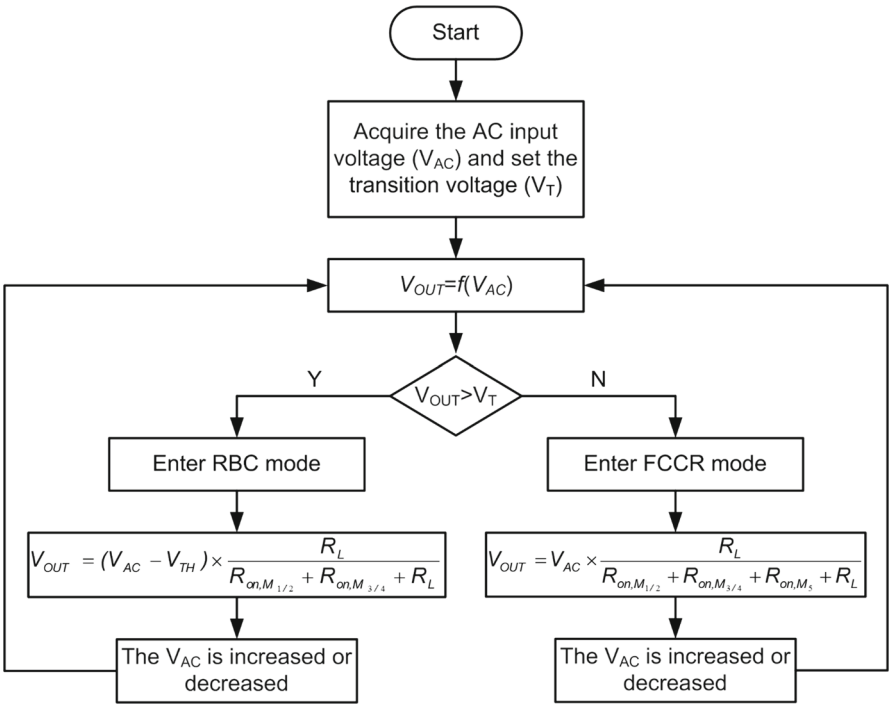


Fig. 11 Flowchart of the proposed rectifier based on MPPT technique

$$V_{\mathrm{OUT}} = (V_{\mathrm{AC}} - V_{\mathrm{TH}}) \times \frac{R_L}{R_{\mathrm{on,M}_{1/2}} + R_{\mathrm{on,M}_{3/4}} + R_L} \tag{7}$$

The proposed rectifier based on an MPPT with DOVD design to dynamically detect V_{OUT} values to enable switching to different circuit modes, thereby achieving high PCE. Figure 11 shows the flowchart of the proposed rectifier based on MPPT technique. The output voltage (V_{OUT}) is the function of AC input voltage (V_{AC}). Once the V_{OUT} is greater than V_{T}, the circuit enters the RBC mode; otherwise, it enters the FCCR mode. Then, the V_{OUT} of RBC mode and FCCR mode is given by Eqs. (6) and (7), respectively. As a result, a higher VCE is achieved by reducing voltage drop, thereby achieving higher PCE.

The complete timing diagram of the proposed rectifier with DOVD is illustrated in Fig. 12. A conceptual diagram of the proposed DOVD is depicted in Fig. 13. The DOVD $V_{\mathrm{OUT}}(V_{\mathrm{DO}})$ is 0 when the DOVD input voltage (V_{DIN}) is lower than the DOVD transition voltage (V_{T}) (line A), and the V_{DO} follows the V_{DIN} when the V_{DIN} is higher than the V_{T} (line B).

Figure 14a illustrates the proposed high-efficiency CMOS rectifier, and its operating principle of the different input voltage cycles under high-voltage operation is shown in Fig. 14b, c. In the positive half cycle of AC input voltage, the power transistor MOS M_2 and $M_3$are turned OFF and the power transistor MOS M_1 and M_4 are turned ON

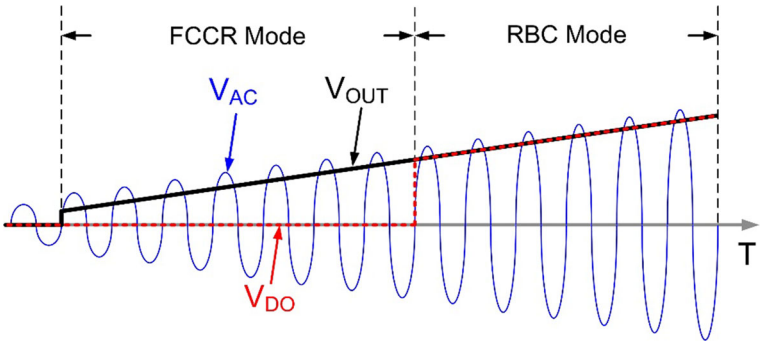


Fig. 12 Timing diagram of the proposed rectifier with DOVD

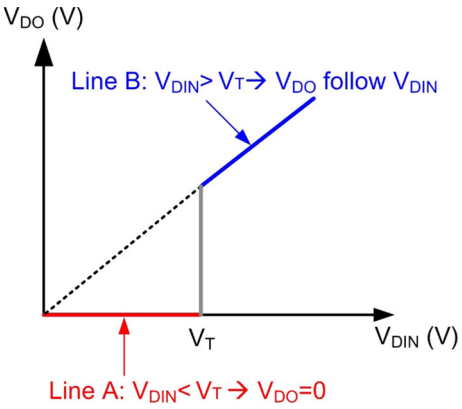


Fig. 13 Concept of proposed dynamic output voltage detector (DOVD)

in the linear region to form the main path. The output voltage (V_{OUT}) connects to a bootstrapping diode formed by PMOS M_5 and M_6 which can effectively block reverse current with only a tiny voltage dropout. By contrast, the power transistor MOS M_1 and M_4 are turned OFF and the power transistor MOS M_2 and M_3 are turned ON in the linear region to form the main path during the negative half cycle of AC input voltage. The proposed DOVD is combined with the FCCR characteristic of high PCE in low-voltage operation without coupling capacitors and the RBC characteristic of effectively preventing reverse current in high-voltage operation with low-voltage dropout, thereby maintaining high voltage and PCE. When the voltage division of the V_{DIN} on resistor R_1 is higher than the V_{TH} of PMOS transistor M_7 (V_{T7}), PMOS transistor M_7 is sent to the linear region, thereby enabling adjustment of the ratio of resistors R_1 and R_2 the determination of the V_{T} in Fig. 13:

$$V_T = V_{T7} \times \frac{R_1 + R_2}{R_1} \tag{8}$$

To enable PMOS transistor M_7 to quickly enter the linear region to obtain a low-dropout V_{DO}, the ratio size of PMOS transistor M_7 and resistor R_3 must be controlled;

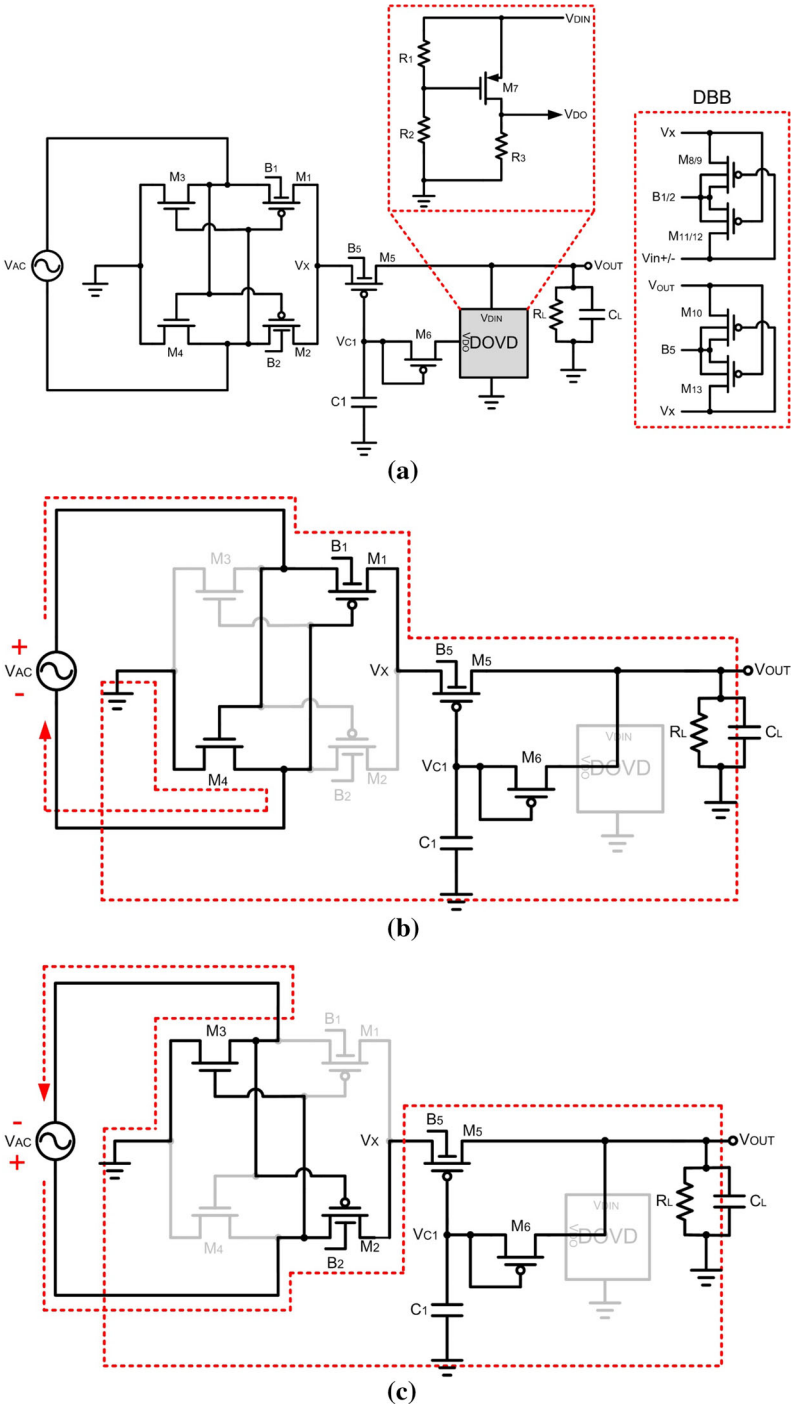


Fig. 14 **a** Proposed wide-input-voltage-range CMOS rectifier; **b** operating principle under positive half cycle; **c** operating principle under negative half cycle

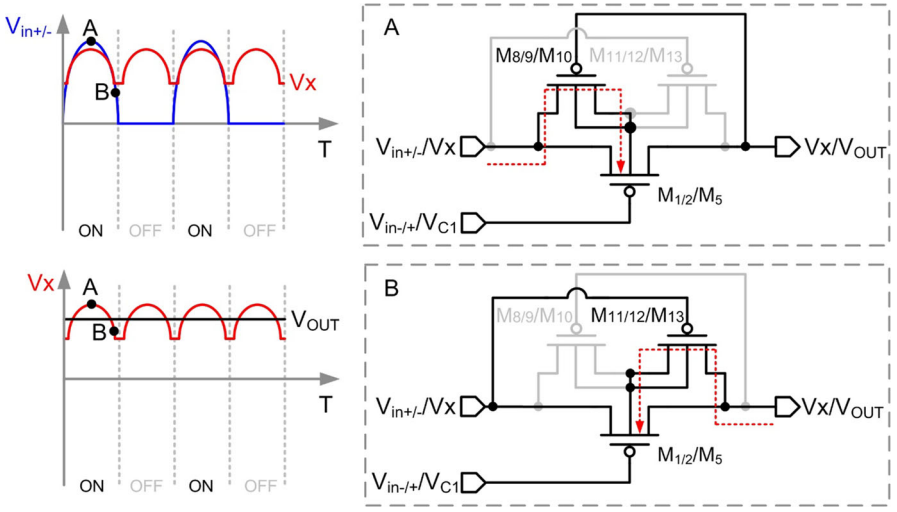


Fig. 15 Operation of dynamic base bias (DBB) circuit

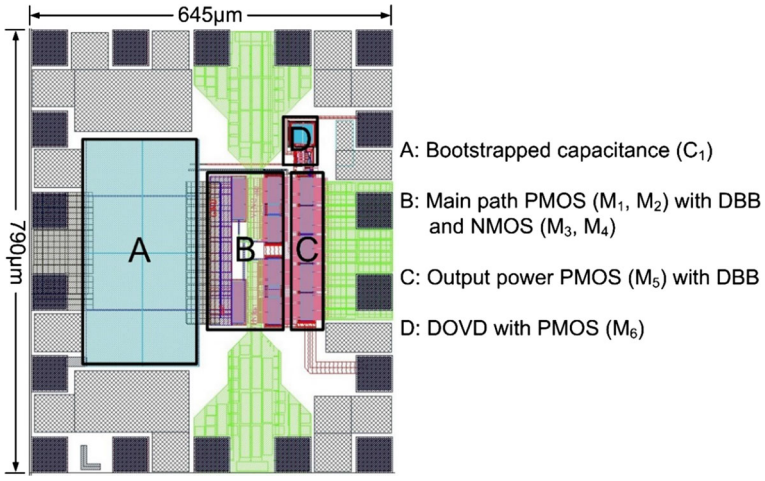


Fig. 16 Layout diagram of the proposed rectifier

a larger transistor size for M_7 or larger resistor value for R_3 enables PMOS transistor M_7 to more quickly and easily enter the linear region.

The main path PMOS transistors M_1 and M_2 and output power PMOS transistor M_5 contribute to a relatively large parasitic capacitance as a smoothing capacitance at node V_X, which causes the DC voltage at the node V_X to rise. However, different DC and AC voltage at V_{AC}, V_X, and V_{OUT} will cause floating source and drain on PMOS transistors M_1, M_2, and M_5. Because of the floating source and drain, the transistor base in the case of conduction cannot receive the highest potential in the circuit, resulting in the body effect, leakage current, and latch-up effect. To mitigate these problems, the dynamic base bias (DBB) circuit [7] is connected to the base

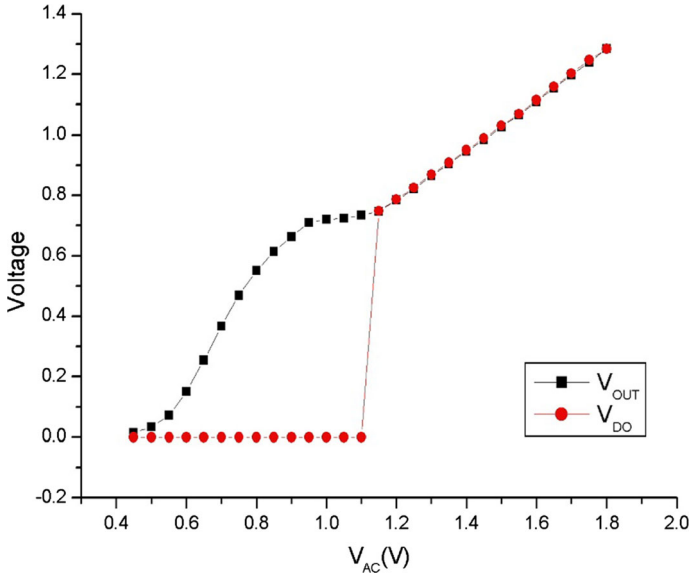


Fig. 17 Simulation results of DOVD under various V_{AC} values

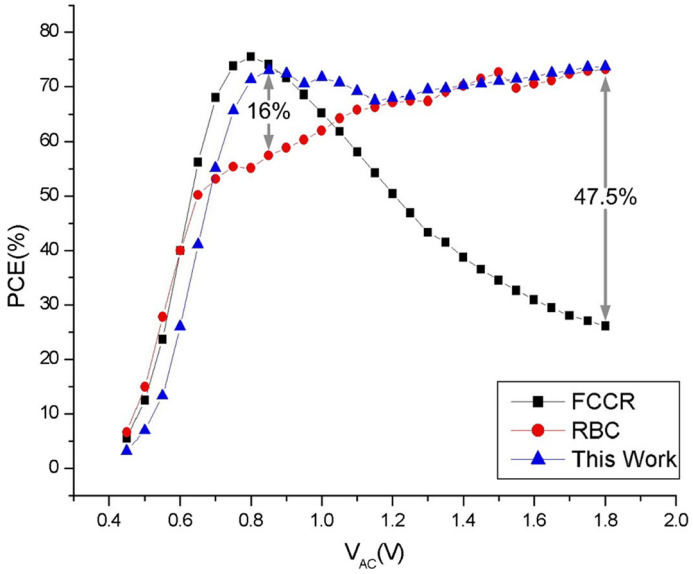
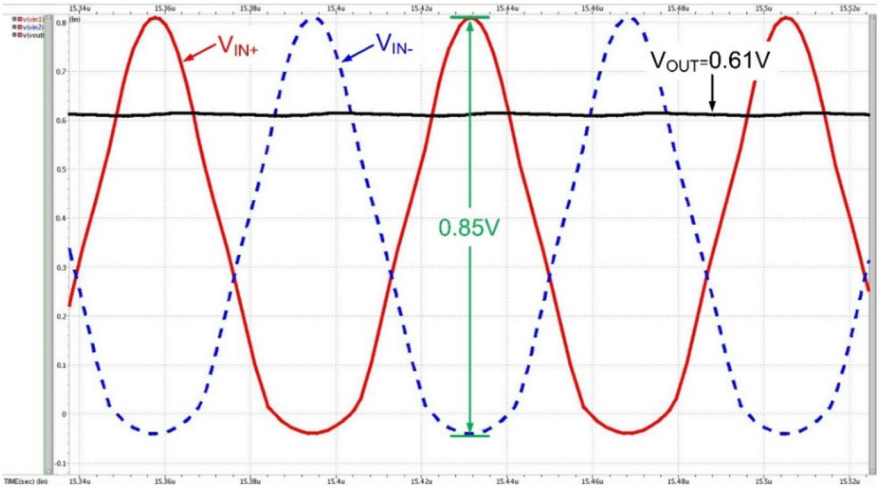


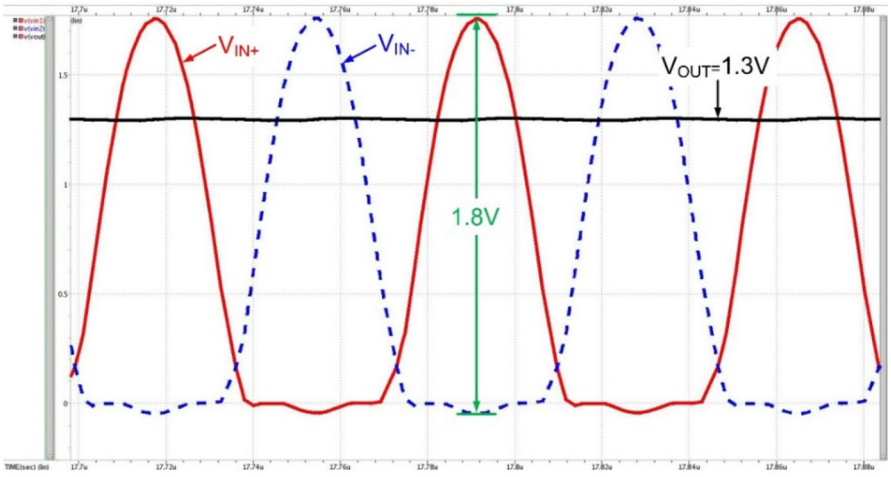
Fig. 18 PCE characteristic curves for simulation of FCCR, RBC, and the proposed rectifier

terminal of PMOS transistors M_1, M_2 and M_5 to ensure that the body bias of PMOS transistors M_1, M_2 and M_5 can be maintained at high potential, as shown in Fig. 15.

Compared with the FCCR, the proposed rectifier can effectively prevent reverse current to achieve a higher PCE without coupling capacitance. Compared with the RBC, PMOS transistors M_1–M_5 in the proposed rectifier operate in the linear area



(a)



(b)

Fig. 19 Simulation waveforms of the proposed rectifier input and output under 13.56 MHz at **a** 0.85 V and **b** 1.8 V in steady state

in low-voltage operation to effectively reduce the source–drain voltage and improve the VCE and PCE. In addition, the reduced use of capacitance results in the proposed rectifier requiring less chip area than does the RBC.

4 Experimental Results

The proposed rectifier was developed through 0.18-μm standard CMOS process with a 1.8-V supply voltage. The layout diagram is shown in Fig. 16. The entire system,

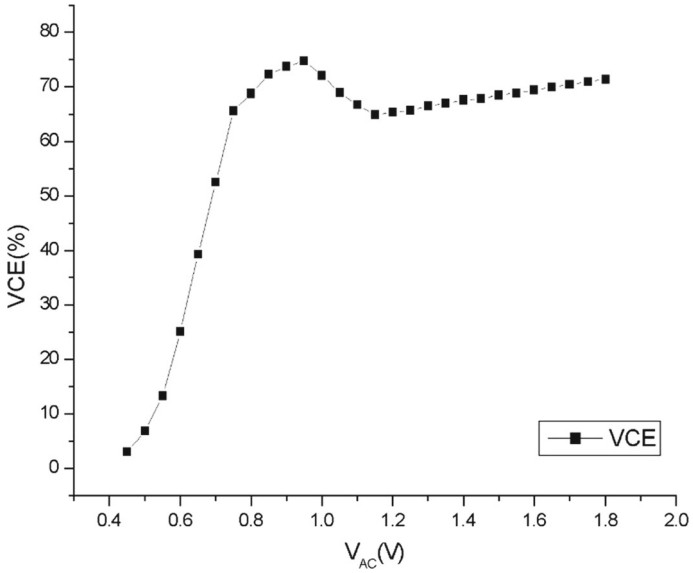
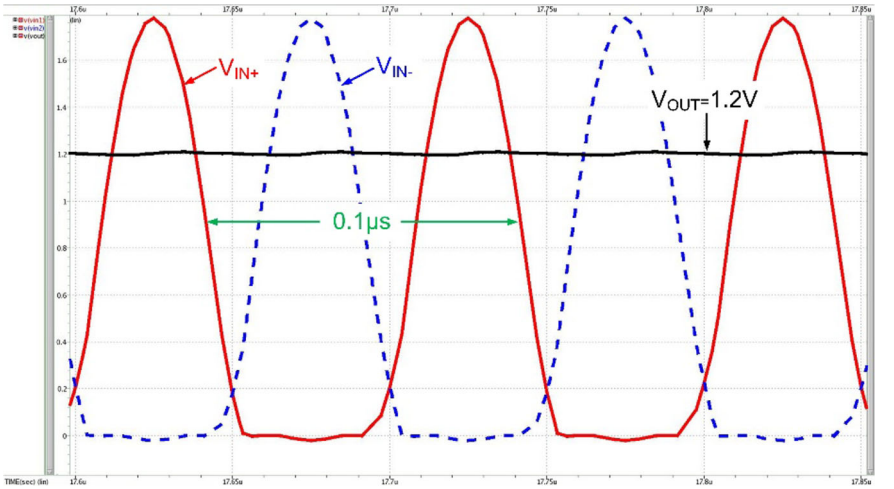


Fig. 20 Simulation results of VCE of the proposed rectifier under various amplitude V_{AC} under a source frequency of 13.56 MHz

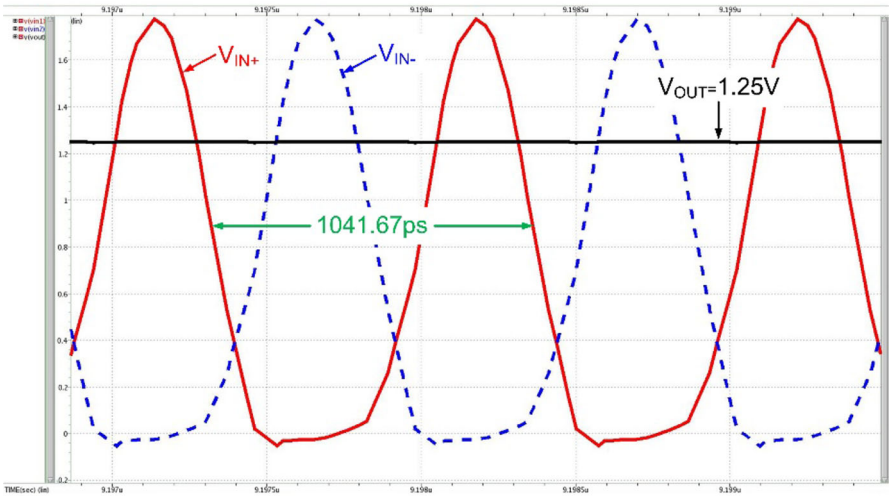
including the I/O pad, required an area of $645 \times 790\,\mu$m. In Fig. 16, region A represents bootstrapped capacitance C_1, region B represents the main path PMOS transistors M_1 and M_2 with DBB circuits and NMOS transistors M_3 and M_4, region C represents the output power PMOS transistor M_5 with DBB circuit, and region D represents the DOVD with PMOS transistor M_6.

Figure 17 presents the simulation results of the DOVD under various V_{AC} values. In this design, the V_T is set at 1.1 V to serve as the circuit mode transition point to maintain the highest possible PCE under various V_{AC} conditions. The V_{DO} is 0 when the V_{AC} is less than 1.1 V; otherwise, the V_{DO} follows the V_{OUT}. The V_T of this circuit can be adjusted according to the load conditions. Appropriate to set the V_T in the cross-point of PCE of the two adopted circuit architectures (FCCR and RBC) can achieve the overall best PCE output.

PCE is often used to compare the characteristics of various rectifier structures. In this section, we compare the previously discussed FCCR and RBC simulation results with those of the proposed rectifier. Figure 18 shows the PCE characteristic curves and peak input amplitudes of three rectifiers with identical main path power MOS ($M_1 - M_4$) and shunt loads of $C_L = 400\,$pF and $R_L = 70\,\Omega$. Compared with the RBC, the proposed rectifier achieves a 16% PCE upgrade in the case of a 0.85-V peak V_{AC}; moreover, because of the use of less capacitance than does the RBC, the proposed rectifier requires a relatively small area to achieve higher performance. Because of the lack of reverse current in high-voltage operation, PCE does not degrade as it does in the FCCR structure. The proposed rectifier achieves a PCE upgrade of 47.5% from that of the FCCR in the case of a 1.8-V peak V_{AC}.



(a)



(b)

Fig. 21 Simulation waveforms of the proposed rectifier input and output under **a** 10 MHz and **b** 960 MHz at 1.8 V in steady state

Figure 19a and b shows the simulation waveforms of the proposed rectifier with V_{OUT} values of 0.61 and 1.3 V at 0.85 and 1.8 V V_{AC}, respectively, under 13.56 MHz in steady state. Figure 20 shows the simulation results of the VCE characteristic curves for the load under a source frequency of 13.56 MHz. The voltage conversion efficiencies were 52.51, 72.3, and 71.35%, and the overall power efficiencies were simulated to be 55.1, 73.03, and 73.66% at peak input source amplitudes of 0.7, 0.85, and 1.8 V, respectively. Figure 21a and b shows the simulation waveforms of the proposed rectifier with V_{OUT} of 1.2 and 1.25 V at 1.8-V V_{AC} and 10

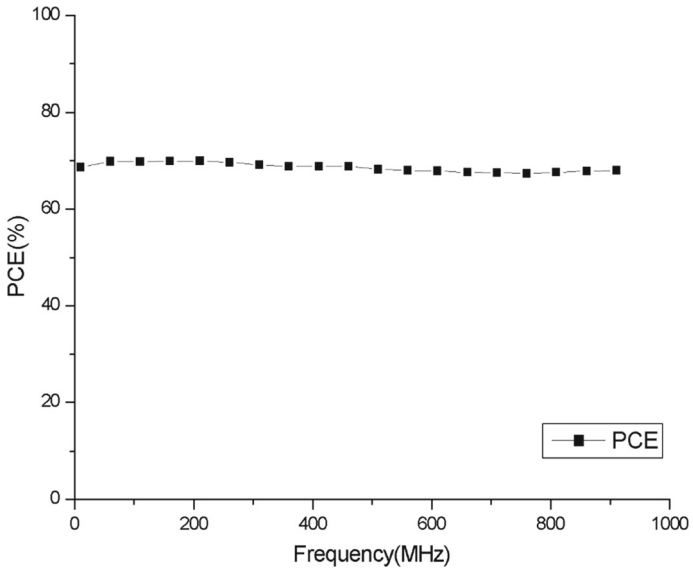


Fig. 22 Simulation results of PCE of the proposed rectifier under various frequency operating points with 1-V peak amplitude V_{AC}

and 960 MHz, respectively, in steady state. Figure 22 presents the PCE simulation results for the proposed rectifier under various frequency operating points with a 1-V peak amplitude V_{AC}. No significant changes in PCE were observed from 10 to 960 MHz, and the overall power efficiencies were simulated to be approximately 70%.

The proposed CMOS rectifier has the features of a wide harvesting range, wide band, and high efficiency and is based on the FCCR and RBC according to different input voltages for the appropriate switch. The proposed rectifier is designed to adjust the most suitable circuit mode through the DOVD sensing circuit to obtain the highest possible PCE at each operating point. Because of the insensitivity of the FCCR and RBC to the frequency response, the operating frequency range can include the biomedical (low frequency) and IoT (high frequency) bandwidths, thus achieving wide band operation.

Table 2 compares the performance of recently developed state-of-the-art rectifiers. As evident from the table, the proposed rectifier circuit can be applied to biomedical systems operating at a relatively low frequency (13.56 MHz) [16–18,20,30] and achieves high PCE performance. In addition, the proposed rectifier has been used in an IoT system at relatively high frequencies of 400–950 MHz [10,12,21,28,34]. Because of the high-frequency operation and parasitic effects engendering low PCE, the input voltage range is often affected by the efficiency of the lifting mechanism. Therefore, enhancing the performance, bandwidth, and input voltage range of the proposed rectifier in high-frequency operation is crucial problem associated with rectifier application in all systems. The proposed rectifier exhibits high PCE performance under low input voltage, wide input range, and wide band.

Table 2 Rectifier parameter comparison

Reference	[17]	[18]	[30]	[21]	[10]	[12]	This work
Technology (μm)	0.5	0.5	0.18	0.25	0.18	0.13	0.18
Input amplitude (V_{AC})	1.72 V	2.2 V	1.192 V	N.A.	N.A.	N.A.	0.8–1.8 V
Output voltage (V_{REC})	2.4 V@R_L = 1KΩ	3.1 V@R_L = 500Ω	2 V@R_L = 100Ω	N.A.	2 V@R_L = 1MΩ	3.2 V@R_L = 1MΩ	0.55–1.3 V @70 Ω
Maximum output current	2.4 mA	6.2 mA	20 mA	N.A.	N.A.	N.A.	20 mA
Rectifier output power	5.8 mW	20 mW	40 mW	10 μW	30 μW	32 μW	4–23 mW
Frequency (MHz)	13.56	13.56	13.56	906	830	902–928	10–960
Power conversion efficiency (PCE)	78%@R_L = 1KΩ	70%@R_L = 500Ω	85%@R_L = 100Ω	30%@R_L = 333KΩ	35.7%@R_L = 1MΩ	32%@R_L = 1MΩ	> 70%@R_L = 70Ω
	68%@R_L = 150Ω				44.1%@R_L = 144KΩ		

5 Conclusion

Energy harvesting technologies, which have grown rapidly in recent years, have been applied in various devices. However, varying degrees of RF decay occur because of various environmental factors. Therefore, many conditions of real applications for energy harvesting circuits must be considered to prevent the possibility of heavily affecting the output characteristics and subsequent operation of the entire system.

This study proposed a wide-harvesting-range, wide band, high-efficiency CMOS rectifier based on an MPPT with DOVD design to dynamically detect V_{OUT} values to enable switching to different circuit modes, thereby achieving high PCE. The VCE was 52.51, 72.3, and 71.35% and the overall PCE was 55.1, 73.03, and 73.66% at peak input source amplitudes of 0.7, 0.85, and 1.8 V, respectively. Moreover, the overall PCE in the 10–960 MHz range was approximately 70% at peak input source amplitudes of 1 V. The main feature of the proposed rectifier is its ability to maintain high PCE in both low-voltage operation (approximately 0.7 V) and high-voltage operation (approximately 1.8 V) and under wide band operation (10–960 MHz), rendering it suitable for low-power IoT applications and RF energy harvesting systems.

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