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Multi-objective Low-Noise Amplifier Optimization Using Analytical Model and Genetic Computation

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Abstract The purpose of this paper is to introduce a methodology for multi-objective radio frequency (RF) low-noise amplifier (LNA) optimization using an analytical model of the MOS transistor in combination with genetic computation. The optimum performance is defined by a figure of merit (FoM) that considers both the power efficiency and the RF performance of the system. Using a short-channel EKV model, the analysis of this FoM suggests that the optimum MOS inversion level lies in the moderate inversion. This knowledge can be used as a strong starting point for the design and optimization procedures. Initially, the LNA component values are extracted using the analytical model. The model does not fully take into consideration the parasitic behaviour of the components in a real design; thus, it produces an approximation of the optimum design. The final circuit fine tuning is achieved with the use of a genetic algorithm that takes advantage of the aforementioned approximation as an initialization aiming at faster convergence. To demonstrate the effectiveness and the operation of this methodology, a 5 GHz common source LNA with inductive degeneration has been designed using the proposed design and optimization methodology. The same design has been statistically investigated using Monte Carlo simulations to address process variability as well as temperature and supply voltage variations. Finally, the optimization procedure is demonstrated also on different topologies including cascode or common gate structures, as well as multi-stage distributed and resistive shunt feedback amplifiers.

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1 Introduction

Radio frequency (RF) and analog mixed signal technologies serve the rapidly growing communication market. The growing demand for larger bandwidth motivates the RF circuit designers to advance to higher frequencies. RF circuit design is increasingly taking advantage of the aggressive scaling of submicrometer CMOS technologies that make higher operating frequencies possible and provides the potential to integrate complete telecommunication systems in a system single chip (SoC). Low-noise amplifiers (LNAs) are among the most important blocks of any telecommunication system. Their importance lies in the fact that they impact the noise performance more than any of the other blocks in the receiver chain. During the LNA design procedure, designers face the problem of trading-off quantities like gain, noise figure, consumption, linearity and input/output matching. A perfect balance of these design quantities would lead to an optimum LNA. Numerous design methodologies that use analytical models and circuit analysis procedures have been reported in the literature. Rules-of-thumb and analytical procedures provide important guidelines for LNA design. In [5], the authors present a methodology that determines the inversion level of the LNA by heuristically choosing a ratio of $f_t/f_0 \geq 5$, while using continuous expressions for noise, f_t, g_m, etc. vs inversion level. Parametric studies using analytical models and full circuit simulation showed that optimum LNA performance is reached in moderate inversion [22,35]. In [38] and [27], an optimal noise factor is determined considering the quality factor of the input matching network, restricting, however, the analysis to strong inversion, opting for higher unity gain frequency f_t, but decreased power efficiency. In [1–4,12,31–33,36], the figure of merit $G_m f_t$-to current ratio is used for ultra-low-power RF design, which is shown to give an optimum performance in moderate inversion. Specific low-power designs have been discussed for RF LNAs [31–33,36], as well as other RF and analog circuitry [12].

However, passive elements, notably integrated inductors, have important imperfections which make such procedures ineffective. Therefore, they can only be useful for approximating the optimum design and the final fine tuning has to be performed by hand. One solution for the final fine tuning is employing evolutionary computing and in particular genetic algorithms (GA). Genetic algorithms are iterative, randomized global search algorithms that are used for solving complex optimization problems. They incorporate the procedures of natural selection, reproduction and mutation found in nature. In a genetic algorithm, each unknown design variable is called a gene, and the collection of all the design variables a chromosome or an individual. The genetic algorithm uses a number of chromosomes called population, and in each iteration (generation) the goal is to evolve the population to yield better performing individuals. The performance of each individual is quantified by a quantity called fitness which is calculated by an objective function that incorporates parameters like gain or noise figure in the case of an LNA. These performance parameters are obtained using an evaluation tool, in this case a circuit simulator. Once the fitness of the individuals is not further

improving, the GA has converged to a final result. This might be a time-consuming procedure depending on the number of genes, but the algorithm's micro-management cannot be challenged by hand-performed trial and error practices. The works of [19] and [8] employ genetic computation to circumvent the inconvenience of parasitics and achieve optimum results, providing, however, no analytical analysis of the circuit.

In the present work, we propose an LNA design and optimization methodology, based on [26] that utilizes a combination of a MOS transistor analytical model and a genetic algorithm that optimizes performance parameters like noise figure, gain, consumption and input/output matching in addition to the selected figure of merit. The analytical model is used to calculate the initial parameters of the LNA, but it does not fully take into consideration the parasitic behaviour of the components in a real design, notably that of the integrated inductors; therefore, the performance of the LNA is slightly different than the expected one. The use of the genetic algorithm alleviates this problem by expertly modifying some of the design parameters. Aiming at faster convergence, the GA embeds the design parameters calculated by the analytical model as an initialization. The optimum operation is defined by the figure of merit (FoM) $G_m f_t$-to current ratio that considers both the power efficiency and speed of the system. Using the short-channel EKV3 [4,29], MOS transistor model for the analysis of this FoM suggests that the optimum region of operation is the moderate inversion, balancing the trade-off between power efficiency and speed. To showcase the effectiveness of the methodology, a 5 GHz common source LNA has been designed and simulated using a mixed signal/RF 90nm CMOS process. The statistical behaviour over process variation has also been simulated as well as the performance of the LNA for temperature and supply voltage variations. Finally, the method is also applied to different LNA topologies, namely common gate and cascode common source LNAs as well as two ultra-wideband amplifiers, a three-stage distributed LNA and a two-stage resistive shunt feedback LNA.

2 Figure of Merit Analysis

A convenient way to judge the performance of RF systems—or to compare RF systems among themselves—is to formulate general figures of merit containing the main performance parameters. The most common figure of merit for LNA design is given by:

$$\mathrm{FoM_{LNA}} = \frac{\mathrm{Gain[dB]} \cdot \mathrm{Freq[GHz]}}{(\mathrm{NF[dB]} - 1) \cdot P_{\mathrm{DC}}[\mathrm{mW}]} \tag{1}$$

where Gain, NF and P_{DC} are the small-signal gain, noise figure and power consumption, respectively. Additional more simplistic figures of merit can be used, the unity gain frequency (f_t) or the maximum frequency of oscillation ($f_{\max}$). Even though f_t and $f_{\max}$ provide knowledge about the speed limits of the system, they do not present any indication about its power efficiency, which is of utmost importance in low-power designs. Power efficiency can be represented by the ratio G_m/I_D, also known as transconductance efficiency.

In low-power RF systems, both power efficiency and maximum speed of operation should be equally considered. Consequently, the selected figure of merit is $G_m f_t$-to

current ratio $G_m f_t / I_D$ that incorporates knowledge about the RF performance of the system alongside with the transconductance efficiency. The authors in [33] have shown that this figure of merit can actually be used instead of the conventional FoM given in (1) since the performance parameters of both FoMs are related to each other.

The signal gain and noise figure are proportional to the square of the MOS transconductance ($\text{FoM}_{\text{LNA}} \propto g_m^2$), and I_D/g_m^2, respectively. Power consumption is simply dc current multiplied by the supply voltage. Combining all these approximations leads to the conclusion that the FoM_{LNA} is proportional to g_m^2/I_D. In the selected figure of merit, the unity gain frequency is proportional to g_m; therefore, $FoM \propto g_m^2/I_D$. Hence, the selected figure of merit can substitute FoM_{LNA}.

The analysis of this FoM begins using the short-channel EKV model [14,29] that incorporates the effect of velocity saturation. The normalized source transconductance is given by [21]:

$$g_{\text{ms}} = \frac{2q_{\text{s}}}{\sqrt{4(1+\lambda_c)+\lambda_c^2(1+2q_{\text{s}})^2}} \tag{2}$$

q_{s} represents the normalized inversion charge at the source terminal and the parameter λ_c accounts for the velocity saturation effect and is defined as:

$$\lambda_c = \frac{2U_{\text{T}}}{E_{\text{C}}L} \tag{3}$$

where U_{T} represents the thermal voltage, E_{C} is the critical longitudinal field and L the device length. The normalized current at the drain under velocity saturation is given by:

$$i_{\text{dsat}} = \frac{4(q_{\text{s}}+q_{\text{s}}^2)}{2+\lambda_c+\sqrt{4(1+\lambda_c)+\lambda_c^2(1+2q_{\text{s}})^2}} \tag{4}$$

Inverting (4) gives the normalized charge as a function of the drain current:

$$q_{\text{s}} = \frac{\sqrt{i_{\text{dsat}}^2\lambda_c^2+2i_{\text{dsat}}\lambda_c+4i_{\text{dsat}}+1}}{2} - \frac{1}{2} \tag{5}$$

The normalized drain current is given by the ratio I_D/I_{spec}, where the normalization current I_{spec} is defined as

$$I_{\text{spec}} = 2nU_{\text{T}}^2\mu_0 C'_{\text{ox}}\frac{W}{L} \tag{6}$$

When the transistor operates in saturation, the normalized drain current is synonymous to the inversion coefficient (IC). This parameter defines the inversion level of the channel and divides the inversion level into three regions:

- $\text{IC} < 0.1$: Weak inversion
- $0.1 < \text{IC} < 10$: Moderate inversion
- $\text{IC} > 10$: Strong inversion

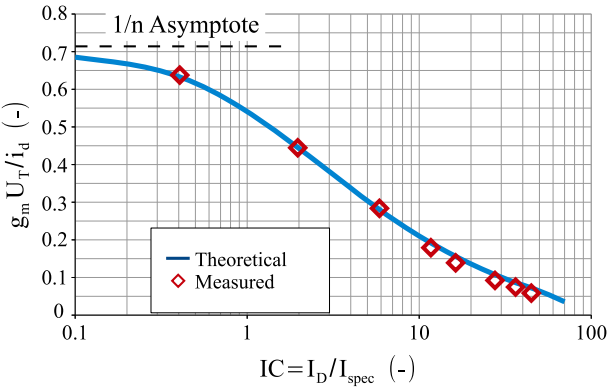

Fig. 1 Measured and simulated transconductance efficiency versus inversion coefficient. The measurements have been taken on a 100 nm device with 40 × 2 µm width and $V_{DD} = 1$ V

The normalized unity gain frequency f_t is given as the ratio of the normalized tranconductance g_m to the normalized total gate capacitance:

$$f_t = \frac{g_m}{2\pi c_{gg}} \tag{7}$$

In saturation, the parameter g_m is given by g_{ms}/n, where n is the slope factor ranging from 1.4 to 1.6 in small channel devices. The total gate capacitance can be approximated by the sum of the gate to source capacitance c_{gs}, the gate to bulk capacitance c_{gb} and the overlap capacitances. In saturation the parameters c_{gs} and c_{gb} are given by:

$$c_{gs} = \frac{q_s}{3}\frac{2q_s + 3}{(q_s + 1)^2} \tag{8}$$

$$c_{gb} = \frac{n-1}{n}\frac{q_s^2 + 3q_s + 3}{3(q_s + 1)^2} \tag{9}$$

Finally, the figure of merit is defined in terms of the normalized quantities as:

$$\text{FoM} = \frac{g_{ms} f_t}{i_d} \tag{10}$$

Figures 1 and 2 show that the measurements on a 100 nm device follow the analytical model meaning the transconductance efficiency peaks at weak inversion, while the unity gain frequency shows maximum performance at strong inversion. Therefore, plotting the product of these two figures of merit as a function of the inversion coefficient shows that the peak of the graph is located in moderate inversion (Fig. 3), and more precisely at a convenient inversion coefficient of $1/\lambda_c$. Additionally, as Fig. 4 depicts, the optimum inversion level moves towards the centre of the moderate inversion when the parameter λ_c becomes larger, and always for IC $= 1/\lambda_c$. Equation 3

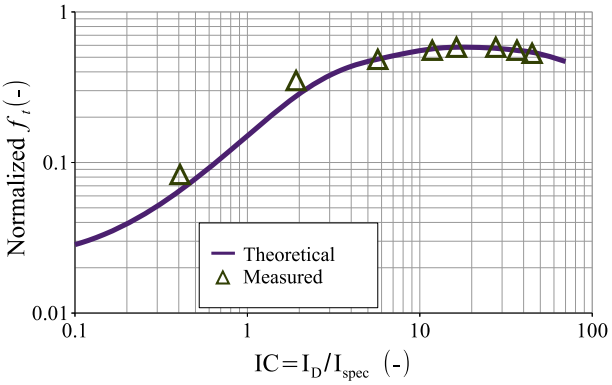

Fig. 2 Measured and simulated unity gain frequency versus inversion coefficient. The measurements have been taken on a 100 nm device with 40 × 2 µm width and $V_{DD} = 1$ V

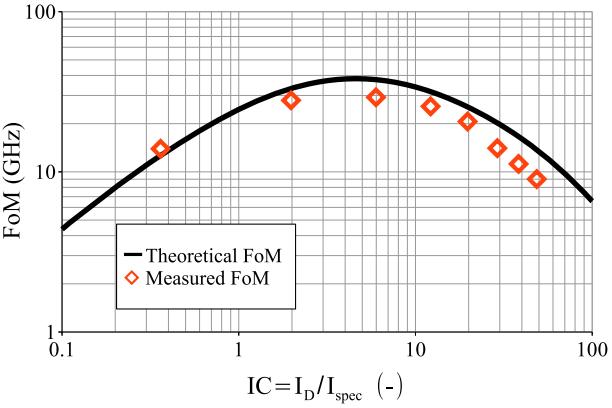

Fig. 3 Measured and simulated figure of merit versus inversion coefficient. The measurements have been taken on a 100 nm device with 40 × 2 µm width and $V_{DD} = 1$ V

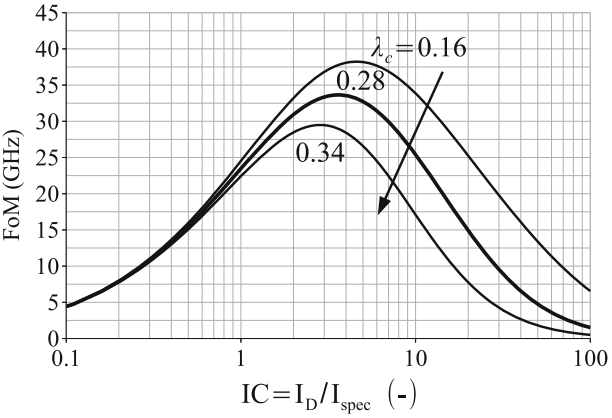

Fig. 4 The selected figure of merit ($G_m f_t$-to current ratio) as a function of the inversion coefficient for different values of the λ_c parameter

shows that λ_c grows by moving to shorter channel technologies. Therefore, with technology scaling the optimum inversion level progresses towards the centre of moderate inversion (IC = 1).

3 Noise Figure Analysis

Since the noise figure of the LNA impacts the most on the total noise performance of the receiver, there is a need for an extensive understanding about the noise contributors and their behaviour under different operating conditions. The main noise contributor of the amplifier is the active device itself. For frequencies much higher than the corner frequency, which is the frequency where flicker noise becomes equal to channel thermal noise, $\mathrm{NF}_{\min}$ in the MOS is dominated by channel thermal noise. The channel thermal noise power spectral density (PSD) is calculated through:

$$S_{\mathrm{id}} = 4kT\frac{I_{\mathrm{spec}}}{U_{\mathrm{T}}}g_n \tag{11}$$

The parameter g_n is the normalized thermal noise conductance and is related to the transistor's transconductance g_m via the parameter γ_n called excess noise factor:

$$\gamma_n \triangleq \frac{g_n}{g_m} \tag{12}$$

The parameter γ_n is of major importance for the noise performance of circuits, since it represents the noise that is generated at the drain of the transistor for a given transconductance. Multiple RF noise measurements presented in the literature ([1–4] and [7]) have shown that the excess noise factor parameter is bias dependent. In [13], a model for the calculation of γ_n has been presented, based on the inversion coefficient. Using a long-channel EKV approximation for a transistor that operates in saturation, the excess noise factor is given by:

$$\gamma_{\mathrm{long}} = \frac{2}{3}\frac{q_{\mathrm{s}} + 3/4}{q_{\mathrm{s}} + 1} \tag{13}$$

Where in this case the normalized inversion charge is given by the long-channel model [14]:

$$q_{s_{\mathrm{long}}} = \sqrt{\frac{1}{4} + IC} - \frac{1}{2} \tag{14}$$

With channel length scaling though, short-channel effects should be considered in noise calculation. The excess noise factor from [13] is formulated here in terms of inversion charge q_{s}:

$$\gamma_n = \gamma_{\mathrm{long}} \cdot \left[1 + (q_{s_{\mathrm{long}}} + 1) \cdot \frac{v_{\mathrm{sat}} \cdot \tau_r}{L_{\mathrm{eff}}}\right] \tag{15}$$

In (15), the parameter v_{sat} corresponds to the saturation velocity, L_{eff} denotes the effective channel length and τ_r is the relaxation time. Relaxation time is used as a fitting parameter with typical value $\tau_r \approx 1\,ps$.

Besides channel thermal noise, at high frequencies the noise figure is also directly affected by the induced gate noise with a PSD that is given by:

$$S_{\text{ing}} = \frac{4}{5} kT\gamma_n \delta_{\text{G}} \frac{(C_{\text{gs}} \cdot \omega)^2}{g_m} \tag{16}$$

where δ_{G} is defined as the gate noise coefficient. Similar to the definition of the thermal noise parameter at the drain, δ_{G} measures the deviation of the induced gate noise transconductance g_{ng} with respect to the transconductance g_m [14]:

$$\delta_{\text{G}} \triangleq \frac{g_{\text{ng}}}{g_m} \tag{17}$$

For a transistor operating in saturation, the theoretical long-channel value of the gate noise coefficient is 1 in weak inversion and 4/3 in strong inversion. The long-channel approximation with respect to the inversion charge q_{s} is given by [34,35]:

$$\delta_{\text{G}} = \frac{1}{3} \frac{32q_{\text{s}}^3 + 114q_{\text{s}}^2 + 132q_{\text{s}} + 45}{\sqrt{(4q_{\text{s}}^2 + 10q_{\text{s}} + 5)(2q_{\text{s}} + 3)}} \tag{18}$$

Since the induced gate noise is caused due to the channel thermal noise, there is a correlation between these two noise sources. This correlation is modelled by the parameter c called the correlation factor and defined as:

$$c \triangleq \frac{S_{\text{ing}} S_{\text{id}}^*}{\sqrt{S_{\text{ing}} S_{\text{id}}}} \tag{19}$$

In long-channel devices and in saturation, the theoretical value of the correlation factor is approximately equal to $-j\,0.57$ in weak inversion and $-j\,0.395$ in strong inversion. Expressing c as a function of the inversion charge:

$$|c| = \frac{\sqrt{5}(q_{\text{s}}^2 + 3q_{\text{s}} + 3/2)}{\sqrt{(q_{\text{s}} + 3/4)(32q_{\text{s}}^3 + 114q_{\text{s}}^2 + 132q_{\text{s}} + 3)}} \tag{20}$$

Combining the information for all the MOS noise contributors, the minimum noise factor is calculated as [1,4]:

$$F_{\text{min}} = 1 + 2\gamma_n \frac{\omega}{\omega_t} \sqrt{\frac{\beta_{\text{G}}}{\gamma_n}(1 - c^2)} \tag{21}$$

where the parameter β_{G} is equal to $\delta_{\text{G}}/(5n)$. Even though Eq. (18) is accurate for long-channel devices, there is no information on the influence of short-channel effects

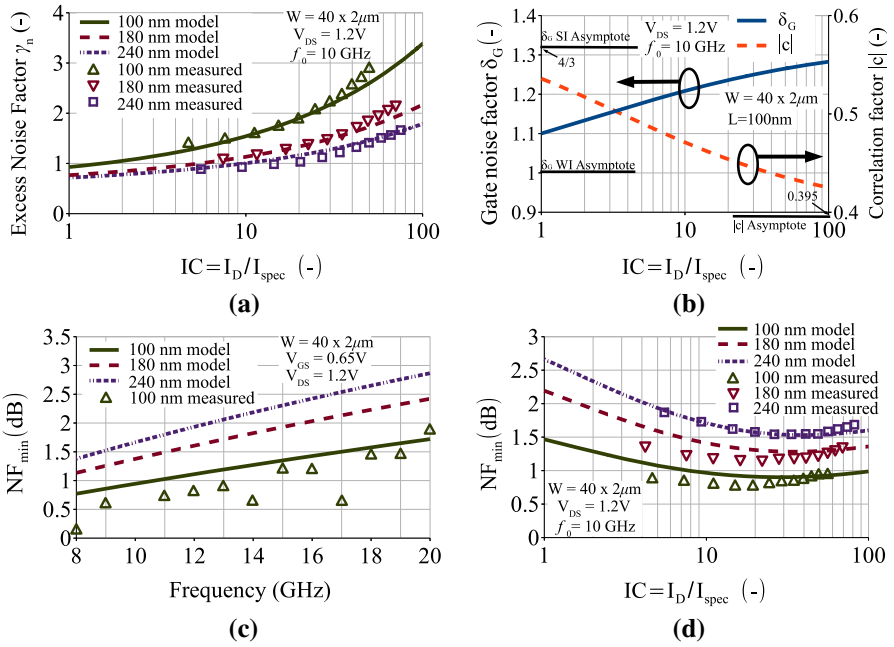

Fig. 5 **a** Measurements and simulation of the excess noise factor as a function of inversion coefficient for three different MOS lengths, **b** gate noise factor and correlation factor as a function of the inversion coefficient, **c** simulated minimum noise figure as a function of frequency for three different MOS lengths, **d** measurements and simulation of the minimum noise figure as a function of the inversion coefficient for three different MOS lengths. The measurements have been taken on a 90nm CMOS process. The noise model uses parameters $\tau_r \approx 1ps$, $v_{\text{sat}} \approx 4 \times 10^4$ m/s, $I_0 = 461$ nA

on the induced gate noise parameter. Therefore, two assumptions are made: first, it is assumed that that the correlation factor c is not affected by short-channel effects and second, the ratio γ_n/δ_G does not change from the long-channel approximation ($\gamma_n/\delta_G \approx 2$). For the calculation of the minimum noise figure, only the ratio is of interest and not the absolute value of δ_G.

Figure 5a presents the simulated excess noise factor in contrast to the corresponding RF noise measurements for three different gate lengths. As it can be seen, the model presents a decent behaviour judging from the small relative error between the measurements, especially for larger values for the gate length. Figure 5b illustrates the model for the gate noise factor and correlation coefficient. It shows that in strong inversion the parameter δ_G approaches the theoretical value of 4/3, on the same note correlation factor $|c|$ also seems to converge to the theoretical value of j 0.395.

The minimum noise figure as a function of frequency is shown in Fig. 5c. The NF_{min} seems to follow a near-linear behaviour in respect to operating frequency. Finally, Fig. 5d presents the minimum noise figure model as a function of the inversion coefficient as well as RF measurements for three different gate lengths. The model provides a decent approximation of the transistor's actual noise performance with respect to biasing. This final figure is of utmost importance for the circuit designers, since it helps to determine the minimum noise figure of the low-noise amplifier.

4 Low-Noise Amplifier Design Procedure

The figure of merit analysis of the previous section can provide the starting point in the design of optimized low-noise amplifiers. Knowing that the peak of the figure of merit is in the moderate inversion and more specifically at an inversion coefficient close to $1/\lambda_c$, the first step is to find a pair of current consumption and transistor width to achieve such condition. The normalization current I_{spec} given by (6) solely depends on the transistor width, since the length is always chosen to be the shortest available in a given technology, providing lowest noise figure and highest f_t. Selecting a desired current consumption leads to a corresponding transistor width in order to maintain the condition $\text{IC}_{\text{opt}} = 1/\lambda_c$:

$$\text{IC}_{\text{opt}} = 1/\lambda_c \Rightarrow \frac{I_D}{I_{\text{spec}}} = 1/\lambda_c \Rightarrow W_{\text{opt}} = \frac{I_D \lambda_c L}{I_0} \tag{22}$$

where the technology current is defined as $I_0 = 2n\mu_0 C'_{\text{ox}} U_{\text{T}}^2$.

Figure 6 shows the topology of the common source LNA with inductive degeneration. The source inductor is called the degeneration inductor and helps in increasing the linearity of the design. In addition, the degeneration inductor L_{s} along side with the gate inductor L_{g} is part of the input matching network. The external capacitor connecting the gate and source of the transistor is used to decouple the transistor's intrinsic capacitance and the quality factor of the matching network. Additionally, it helps in case the degeneration inductance is not realizable, artificially reducing the f_t of the transistor. The input impedance Z_{in} of the topology is:

$$Z_{\text{in}}(s) = (L_{\text{s}} + L_{\text{g}})s + \frac{1}{sC_{\text{t}}} + \omega_t L_{\text{s}} \tag{23}$$

where C_{t} is the sum of the total gate capacitance C_{gg} and the value of the external capacitor C_{ext}. The parameter ω_t is the radian unity gain frequency of the MOS transistor and is related to f_t through $f_t = 2\pi\omega_t$. The input is matched when the real part

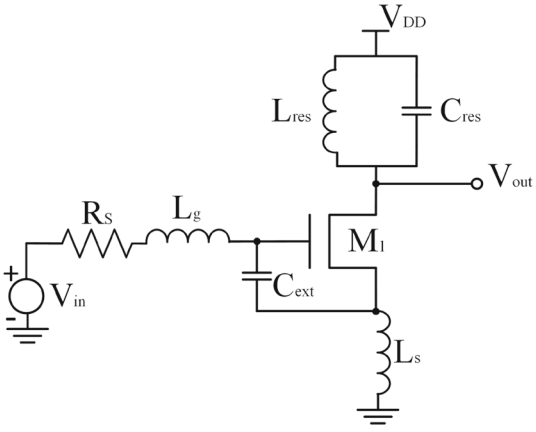

Fig. 6 Common source low-noise amplifier with inductive degeneration

of the input impedance is equal to the source resistance R_s and the imaginary part is equal to zero at the frequency of interest ω_0:

$$\Re\{Z_{in}(j\omega_0)\} = R_s \Rightarrow \omega_t L_s = R_s \tag{24}$$

$$\Im\{Z_{in}(j\omega_0)\} = 0 \Rightarrow L_s + L_g = \frac{1}{\omega_0 C_t} \tag{25}$$

Substituting ω_t with $f_t/2\pi$ in (24) and using (7) leads to:

$$L_s = \frac{2\pi R_s C_{gg}}{g_m} \tag{26}$$

The transconductance g_m is calculated dividing the expression (2) with the slope factor n. The value of the total gate capacitance is given by:

$$C_{gg} = W_{opt} L C'_{ox}(c_{gs} + c_{gb}) + C_{overlap} \tag{27}$$

where the normalized capacitances c_{gs} and c_{gb} are given by (8) and (9). The parameter $C_{overlap}$ is the sum of all the MOS overlap capacitances which are slightly bias dependent meaning they can be considered constant for a given MOS geometry. Having calculated the value of the degeneration inductor L_s, the value of the gate inductor is calculated using (25) and the matching network is completed.

The inductance at the output node is used to tune the gain of the amplifier to the frequency of interest. The inductance should resonate with the MOS drain capacitance, the output capacitance and the input capacitance of the following stage at the frequency of interest f_0. A common technique is the use of an L–C tank that lowers the value of the output inductor leading to a more narrowband response. The values of the components for the resonator are calculated through:

$$f_0 = \frac{1}{2\pi\sqrt{C_{res} L_{res}}} \tag{28}$$

When the tuning is realized without an L–C tank, the inductor value becomes larger since it has to resonate with the MOS drain capacitance, which is relatively small and essentially reduces to the overlap capacitance when the transistor operates in saturation. Consequently, the amplifier's response is more wideband, considering that the bandwidth is inversely proportional to the quality factor of the resonator, which in turn is inversely proportional to the value of the inductor. These LNA design steps are executed with the assumption that the integrated inductors are ideal, i.e. have quality factors reaching infinity. A more accurate representation of an integrated inductor is shown in Fig. 8. An integrated inductor apart from the inductance itself contains complex networks of parasitic inductances, capacitances and resistances that model the metal losses.

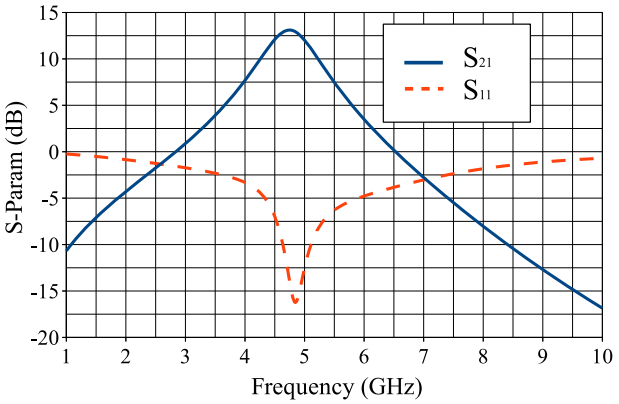

Fig. 7 Small-signal response of a 5 GHz LNA designed using the procedure described in Sect. 2

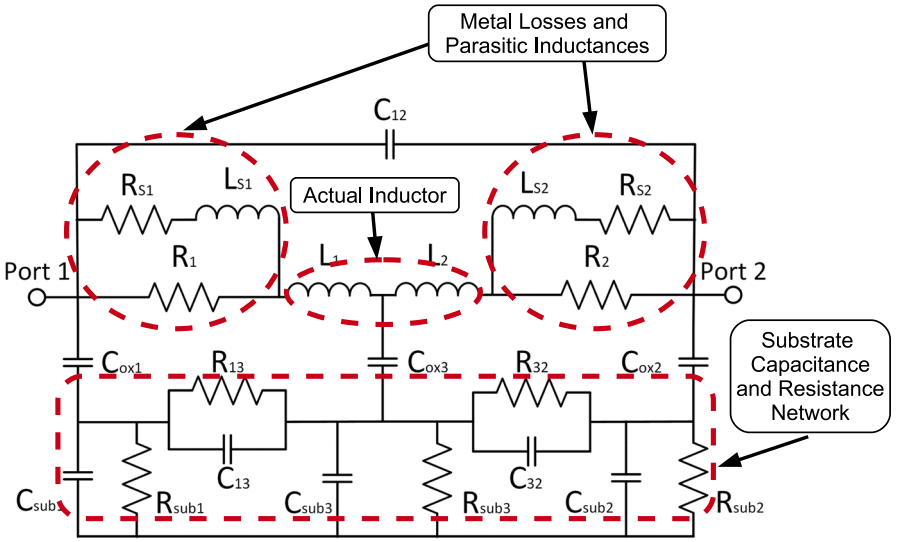

Fig. 8 The equivalent circuit of a standard integrated inductor including all the parasitic elements

5 Genetic Optimizer

Using the design procedure of the previous section leads to an LNA design that is performing slightly different than expected. Figure 7 shows exactly this behaviour; the amplifier's response has been shifted to roughly 4.8 GHz instead of 5 GHz while the input matching shows the same outcome accordingly. The reason for this phenomenon is the parasitic behaviour of the components used. The design methodology does not fully take into consideration all the non-idealities mostly of passive components, which explains this somewhat unpredictable behaviour. The actual model of the inductor contains, besides the inductance itself, a number of parasitic elements as shown in Fig. 8. Hence, full circuit simulation is necessary to obtain globally optimized LNA

design. Trying to embed the precise models for the passive components in the design procedure is not practical since the complexity will rise accordingly. In addition, using the precise models means that the methodology can produce optimum LNA designs that only use components from a specific process design kit.

To overcome this complication, the final fine tuning is made by a genetic algorithm. The chromosomes are comprised by the number of turns, and the radii of the three inductors, as shown in Fig. 6, accompanied by the NMOS number of fingers (N_{f}) and finger width (W_{f}). Optimization of the number of fingers and finger width is important, since RF parameters, such as f_t or NF, may significantly be impacted by the choice of N_{f} and W_{f} [16,17]. The chromosomes do not contain design parameters regarding the capacitors, since their parasitic behaviour is far less pronounced than that of the integrated inductors'.

The first step of the genetic algorithm is the initialization of the unknown design variables through a random number generator. Aiming at faster convergence, the first chromosome of the population is not initialized randomly, but with the parameter values calculated from the design procedure of the previous section. This supported initialization will ultimately reach the optimum design much faster. Afterwards, the performance of each chromosome is evaluated through the SpectreRF circuit simulator of the Cadence Virtuoso ADE. The performance parameters are then used to calculate the fitness of each individual using the fitness function:

$$\text{fitness} = w_{S11}h_{S11} + w_{S21}h_{S21} + w_{S22}h_{S22} + w_{\mathrm{NF}}h_{\mathrm{NF}} + w_{\mathrm{ID}}h_{\mathrm{ID}} + w_{1\mathrm{db}}h_{1\mathrm{db}} \quad (29)$$

In the fitness function formula the parameters h_i (i = S_{11}, S_{21}, S_{22}, NF, I_D and 1-dB) are the performance functions extracted from the simulator. The h_{S11} and h_{S22} correspond to the input and output matching of the LNA and are defined as the square difference between the simulated performance and the ideal input/output matching. The performance function h_{S21} describes the gain of the amplifier and is defined as $1/S_{21@f_0}$, where f_0 is the frequency of interest. The parameters h_{NF} and h_{ID} are used to measure the performance of noise figure and current consumption, respectively. Finally, the $h_{1\,\mathrm{db}}$ performance metric corresponds to the 1-dB compression point and is calculated as the square of the input power at the 1-dB compression point in milliwatts. The definition of all these performance parameters is seen in Table 1. The trade-offs between the performance metrics can prove challenging for the algorithm's convergence. To alleviate this concern, the weighing parameters w_i are used to enhance the impact of some performance parameters over the others. The values of these weights are chosen heuristically, and since this work aims at LNA design optimization, the weighting parameters are emphasizing the noise performance. An individual is performing best when its fitness function is the lowest possible.

The next step of the genetic algorithm is to generate the new population through the processes of selection, crossover and mutation. The selected probabilities of crossover and mutation are set 0.5 and 0.1, respectively. The population number is chosen to be 25 chromosomes; thus, typically in each generation 2.5 mutations take place. Using a such mutation probability ensures that the genetic algorithm will expand the search space faster. The population evolution is repeated until a termination condition is

Table 1 Design parameters after genetic optimizer

Performance parameter	Definition	Description
h_{S11}	$\lvert\mathrm{Re}\{S_{11}\}\rvert^2_{@50\Omega} + \lvert\mathrm{Im}\{S_{11}\}\rvert^2_{@50\Omega}$	Simulated input matching difference from ideal matching conditions ($h_{S11} = 0$)
h_{S21}	$1/S_{21}\lvert_{5\,\mathrm{GHz}}$	Simulated small-signal gain at the centre frequency. As the gain increases, the value of h_{S21} decreases
h_{S22}	$\lvert\mathrm{Re}\{S_{22}\}\rvert^2_{@50\Omega} + \lvert\mathrm{Im}\{S_{22}\}\rvert^2_{@50\Omega}$	Simulated output matching difference from ideal matching conditions ($h_{S22} = 0$)
h_{NF}	$\mathrm{NF}\rvert^2_{5\,\mathrm{GHz}}$	The square of the simulated noise figure at the centre frequency. The square is used to augment the small changes of NF
h_{ID}	$\lvert 1 - \frac{I_D}{I_{\mathrm{Dspecified}}}\rvert^2$	Square difference of the simulated drain current and the specified drain current
$h_{1\,\mathrm{db}}$	$1/P_{1\,\mathrm{db}}$	Simulated power value at 1-dB compression point. As power increases, the value of $h_{1\,\mathrm{db}}$ decreases

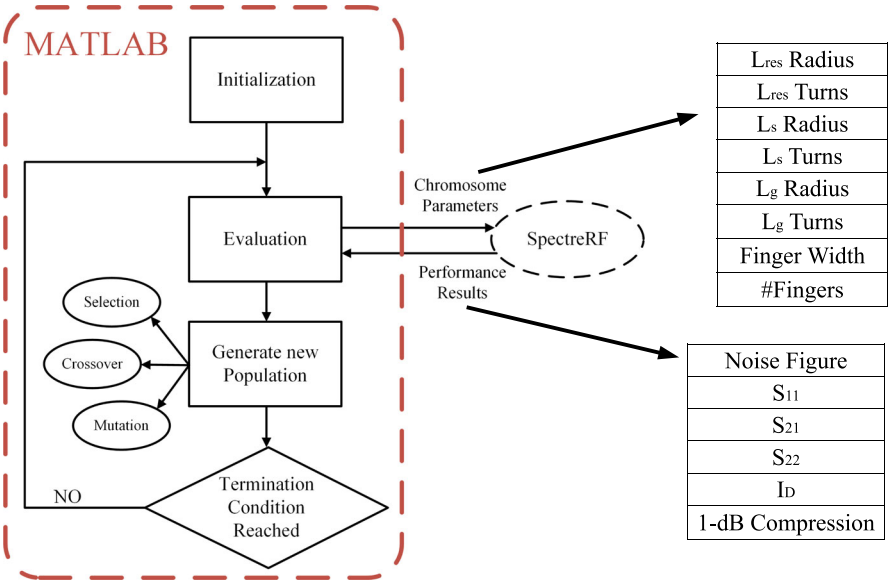

Fig. 9 The flowchart of the LNA optimization using genetic algorithm

reached. Termination condition can be a maximum number of generations or the fitness function has reached the lowest possible value. This iterative procedure is illustrated in the flowchart of Fig. 9.

Table 2 Design parameters after genetic optimizer

Inductor	Inductor width (μm)	Inner radius (μm)	Number of turns	Device width	
L_{res}	15	27	0.5	Finger width	4.65 μm
L_s	15	17	0.75	Number of fingers	46
L_g	3	79	2.5	Total width	213 μm

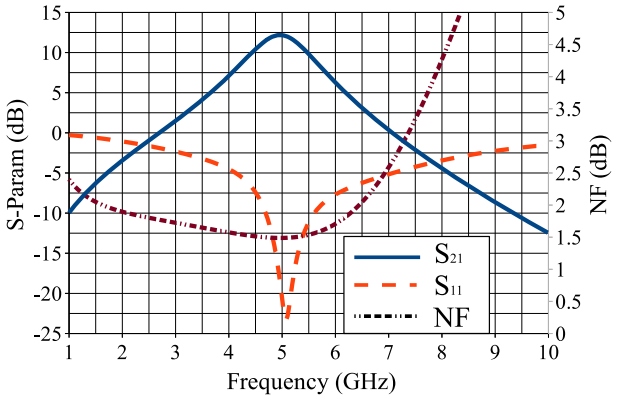

Fig. 10 Small-signal response of the genetically optimized 5 GHz LNA

6 A 5 GHz Common Source LNA Case Study

To illustrate the effectiveness of the design and optimization methodology in combination with the genetic algorithm, a 5 GHz common source LNA with inductive degeneration (Fig. 6) has been designed using a 90 nm standard bulk CMOS process. Since the technique is called current specified, the first step is to define the current consumption, which in this case is chosen to be 10 mA. Afterwards, following the design procedure of Sect. 4 the values of the design components are calculated.

When the first design has been extracted from the analytical model, the initial parameters for the inductors and the transistor width are imported into the genetic algorithm as a chromosome. The optimizer then tries to find the individual with the best fitness value according to (29). The optimized design parameters are shown in Table 2. Figure 10 illustrates the small-signal performance of the amplifier, while Fig. 11 shows the large signal response and more specifically the 1-dB compression point. Judging by the results, the methodology seems to have found a balance in each design category, producing an LNA with high gain at 13.2 dB, low-noise figure at 1.48 dB and matched input/output with −23.2 and −20.5 dB, respectively, at the centre frequency. Additionally, the choice of an inductively degenerated LNA topology proves to be adequately linear for most applications with an 1-dB compression point at an input power of roughly −0.6 dBm. The inversion coefficient has converged at 6.2; thus, the optimum operation of the LNA is indeed the moderate inversion. Finally, with an inversion coefficient of 6.2 the unity gain frequency f_t is 81 GHz.

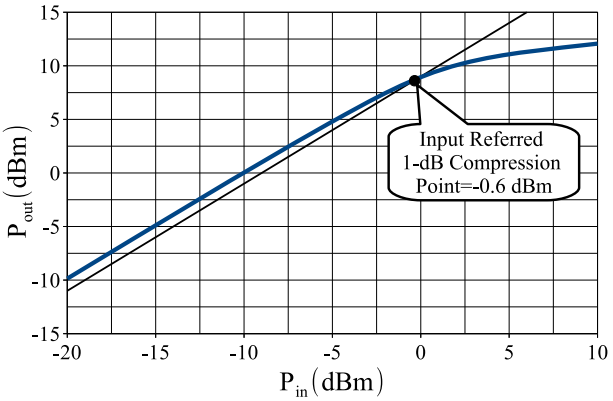

Fig. 11 1-dB Compression point of the genetically optimized 5 GHz LNA

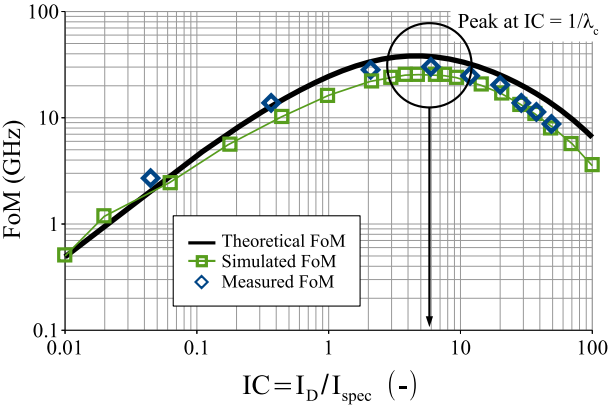

Fig. 12 Figure of merit according to the analytical model, the measurements on a 100 nm device and the simulated results. The measurements have been taken on a 100 nm device with 40 × 2 μm width and $V_{DD} = 1$ V

The current consumption of the circuit is 11.5 mA which is a 15% increase from the originally selected current. This behaviour is due to the optimization procedure, requiring some adjustments to find a balance between the trade-offs of the design. With such current consumption and a supply voltage of 1.2 V, the static power consumption is 13.8 mW. For the verification of the theoretical analysis, the same design methodology has been used to produce the common source LNA topology for different inversion levels ranging from weak to strong inversion. The simulated results are illustrated in Fig. 12 in contrast with the theoretical response and the measurements taken on a 100 nm device. It can clearly be seen that according to the selected figure of merit $g_m f_t / i_d$, the optimum region of operation can be found in the moderate inversion. Additionally, the peak of the normalized FoM lies at an inversion coefficient around 6.2, demonstrating the accuracy of the theoretical analysis, since the LNA case study is designed for such an inversion coefficient.

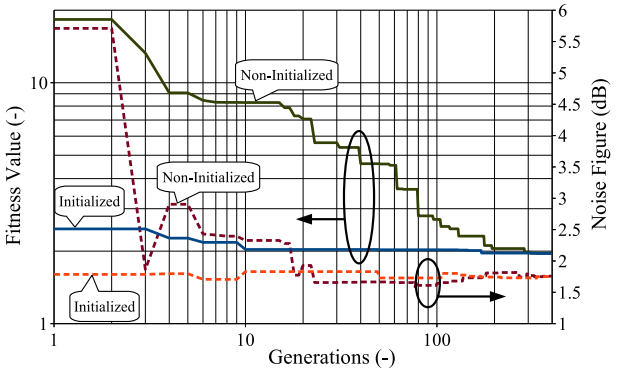

Fig. 13 Convergence of the initialized and the non-initialized genetic algorithms. The *solid lines* show the evolution of the fitness value, while the *dotted lines* correspond to the evolution of the noise figure

A critical point of this paper is the use of the analytical model as an input for the genetic optimizer. The advantage of this approach is illustrated in Fig. 13. The solid line shows the difference in the number of generations needed to find the optimum fitness value between the initialized GA and a non-initialized one. The non-initialized GA converges after 309 generations, whereas the initialized converges much faster after 171 generations, a decrease of 44%. Using a first-generation Intel Core i7 CPU the computing time for the initialized genetic algorithm is less than an hour when the non-initialized algorithm converges in about two hours. Additionally, the starting fitness value of the initialized GA is 2.47 and the converged fitness is 1.95. In contrast, the GA with the randomized initialization, in this test, starts at a fitness value of 15.13 and converges at a value of 1.96. The dotted lines of the figure show the evolution of the noise performance for the two algorithms. The initialized one starts at a significantly smaller noise figure and converges much faster to the optimum value. The final difference in the noise figure is seen because the two algorithms converge to different designs but with approximately the same fitness value. Therefore, the noise figure of the non-initialized case might be slightly larger, but this is compensated in some other performance parameter.

7 PVT Variation Analysis of the 5 GHz Common Source LNA

Both MOS parameters and passive components values can experience significant statistical uncertainty due to chemical mechanical polishing, sub-wavelength lithographic errors, diffusion process, uneven oxide thickness and other sources of manufacturing variations as process technology scales [24]. Another concern regarding the statistical behaviour of the LNA is introduced from the environmental uncertainties like the temperature of operation and the variations of the supply voltage; voltage drops due to degraded battery in wireless devices or voltage spikes resulting from an array of uncertainties like faulty power electronics. Therefore, the PVT (process-voltage-temperature) analysis is necessary to provide insight for the operating corners or the yield of a system under such uncertainties.

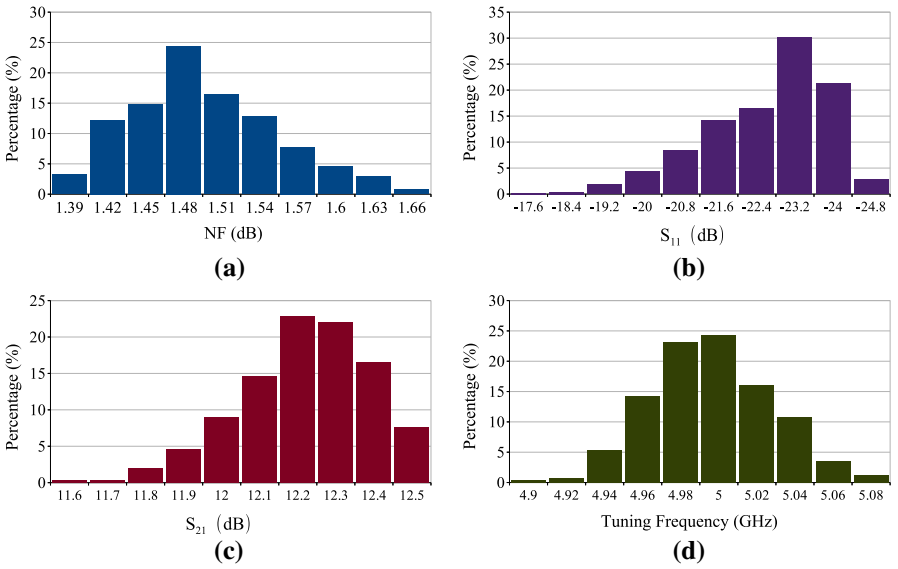

Fig. 14 The distribution of some performance metrics after 200 Monte Carlo simulations. **a** Noise figure, **b** input matching (S_{11}), **c** small-signal gain (S_{21}), **d** maximum gain frequency

7.1 Process Variation

The amplifier's response over process variation can be simulated using Monte Carlo simulations with a model that changes the behaviour of the active or passive components using random distributions. After 200 simulations, the statistical behaviour of some performance parameters over process variation are depicted in Fig. 14. It can be seen that some performance parameters are more susceptible to process variation than others. For example, the S_{11} and S_{21} parameters that correspond to the input matching and small-signal gain, respectively, still perform adequately for most applications. In contrast, the noise performance is impacted the most out of the statistical uncertainties with values ranging from 1.39 to 1.66 dB.

The parasitic resistance of either the active or passive components contributes to the noise figure in the form of thermal noise. As seen in (11) and (12), the power spectral density of the thermal noise is a function of the transconductance g_m which changes over process variation. Additionally the channel thermal noise PSD is related to the device geometry that change over process variation. Furthermore, the noise figure is also directly affected by the induced gate noise with a PSD given by (16). Therefore, the induced gate noise is heavily affected by variability which adds to the overall noise figure distribution. The noise performance is also affected by the input source admittance which changes as the values of the input matching network are changed due to variability. Finally, the parasitic resistances of the passive components that model the metal losses also affect the noise performance and their values are sensitive to variation. Consequently, the noise performance of the system is strongly related to all the components of the circuit and that explains why the noise figure is largely susceptible to process variation.

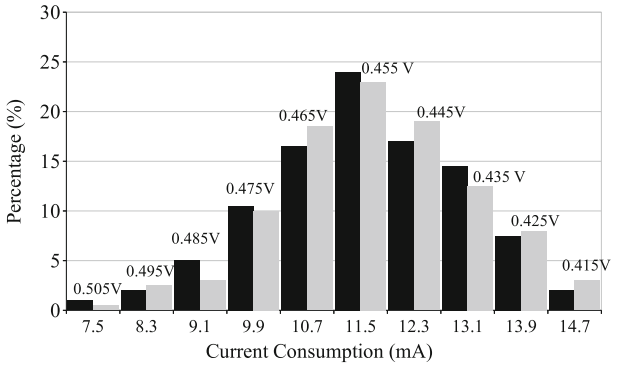

Fig. 15 The distributions of the current consumption and the threshold voltage after 200 Monte Carlo simulations. The *black bars* correspond to the current consumption and the *grey bars* to the threshold voltage

Figure 15 illustrates the distributions of the current consumption and the threshold voltage. It can clearly be seen that there is a strong connection between these two parameters. The Pearson correlation coefficient is a measure of the linear correlation between two random variables X,Y. It is defined as:

$$\rho_{X,Y} = \frac{\text{cov}(X, Y)}{\sigma_X \cdot \sigma_Y} \tag{30}$$

where $\text{cov}(X, Y)$ is the covariance of the two random variables and σ_X, σ_Y are the standard deviations of X and Y. The parameter $\rho_{X,Y}$ has a value between -1 and 1, where 0 is no correlation and -1, 1 are total negative and positive correlation, respectively. Using this metric, the correlation between the current consumption and the threshold voltage has been calculated -0.98, meaning that the distribution of the current consumption is close to an absolute linear function of the threshold voltage distribution.

The tuning frequency is also affected by variability as depicted in Fig. 13d. The chart shows the distribution of the frequency where the small-signal gain of the amplifier is maximum. One reason behind this frequency shift is the variation at the values of the components in the L–C tank. The most impactful reason for the frequency shift though is the input matching. Since the parameters of the input matching network are affected by process variation, the frequency of the optimum matching also experiences a slight shift, just like the case in the performance parameters of Fig. 7. This claim is cemented by the Pearson correlation coefficient which has been calculated -0.85. Thus frequency shift is strongly related to the input matching network variation.

Figure 15 illustrates the selected figure of merit after the Monte Carlo simulations. The solid black lines indicate the typical, fast and slow process corners. Each individual figure of merit not only changes in amplitude, but also shows a slight shift on the horizontal axis depending on the component parameters' variability. The optimum inversion region remains the moderate inversion for every simulation, confirming once again the moderate inversion as the best region for the design of RF systems,

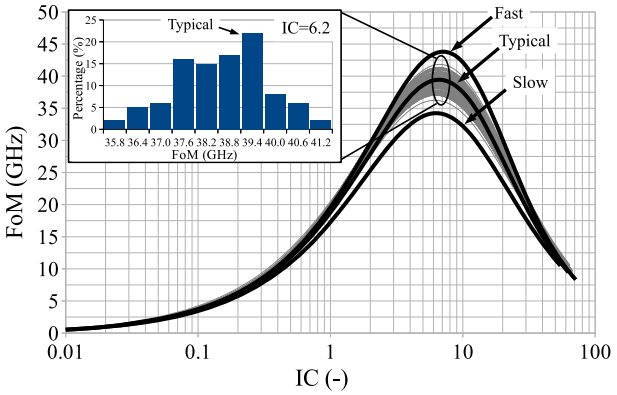

Fig. 16 Figure of merit after 200 Monte Carlo simulations. The *thick black lines* correspond to the process corners. The *inset* shows the histogram corresponding to IC = 6.2

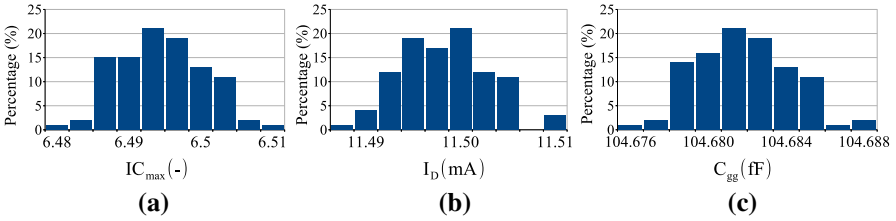

Fig. 17 The histograms of some parameters related to FoM in the case where the process variation applies only to passive devices. **a** Inversion level of the FoM peak, **b** MOS current, **c** MOS total gate capacitance

immune even to process variation. The exact inversion level changes though, with the inversion coefficient ranging from 6 to roughly 7. In any case, Fig. 16 shows that fast/slow process case files adequately capture the upper and lower bounds of the variability as observed in the Monte Carlo simulations.

7.2 Inversion Level Shift Study

The shift of the optimum inversion level is a result of the variation of many parameters mostly related to the active device. Running the Monte Carlo simulation in the case where only the passive devices are affected by process variation can prove this assumption as shown in Fig. 17. Figure 17a shows that the optimum inversion level is slightly affected by the variation of the passive devices with a standard deviation of only 0.01. The parasitic resistances of the passive devices introduce some minor voltage drops which directly affect the transistor's current. Consequently, since the parasitic resistances are subject to statistical changes, the current will also display a similar behaviour as shown in Fig. 17b. Additionally, since the change in current results in the change of the MOS operating point, parameters like the total gate capacitance are also affected (Fig. 17c).

Since the variability of passive devices does not significantly affect the variability of the figures of merit, the active devices are the main responsible for the variability seen in Fig. 16. The figure of merit $g_m f_t / i_d$ consists of normalized values that are only a function of the inversion coefficient. The actual value of the FoM is given by:

$$\mathrm{FoM}_{\mathrm{unorm}} = \frac{g_m f_t}{i_d} \cdot \frac{1}{U_{\mathrm{T}}} \cdot \frac{G_{\mathrm{spec}}}{C'_{\mathrm{ox}} \cdot W \cdot L} \tag{31}$$

where G_{spec} is the normalization factor of the transconductance g_m and is defined as $I_{\mathrm{spec}}/U_{\mathrm{T}}$. The parameter I_{spec} is defined in (6). Substituting these relations into (31):

$$\mathrm{FoM}_{\mathrm{unorm}} = \mathrm{FoM}_{\mathrm{norm}} \cdot \frac{1}{U_{\mathrm{T}}} \cdot \frac{\frac{2nU_{\mathrm{T}}^2 \mu_0 C'_{\mathrm{ox}} W/L}{U_{\mathrm{T}}}}{C'_{\mathrm{ox}} \cdot W \cdot L} = \mathrm{FoM}_{\mathrm{norm}} \cdot \frac{2n\mu_0}{L^2} \tag{32}$$

Considering that the slope factor n remains almost constant, the FoM is also a function of the mobility μ_0 and the MOS length which are both affected by process variation. Mobility has an immediate effect on the velocity saturation parameter λ_c given by (3), since the critical longitudinal E_{c} field is equal to V_{sat}/μ_0.

As mentioned earlier, $\mathrm{FoM}_{\mathrm{norm}}$ is a function of the inversion coefficient. When the transistor operates in saturation, the inversion coefficient is roughly equal to $q_{\mathrm{s}}^2 + q_{\mathrm{s}}$, where q_{s} is the normalized source charge and is a function of the normalized pinch-off voltage through:

$$v_{\mathrm{p}} - v_{\mathrm{s}} = 2q_{\mathrm{s}} + \ln(q_{\mathrm{s}}) \tag{33}$$

where v_{s} is the normalized source voltage with a constant value. The pinch-off voltage is equal to:

$$v_{\mathrm{p}} \cong \frac{V_{\mathrm{G}} - V_{\mathrm{T0}}}{n \cdot U_{\mathrm{T}}} \tag{34}$$

When the gate voltage V_{G} and the source voltage V_{S} are held constant, the normalized source charge is a function mainly of the threshold voltage V_{T0}. Hence, the variability of the threshold voltage is directly causing variability in inversion charge, therefore, also in drain current, transconductance, noise etc. On the other hand, the distribution of the threshold voltage has already been discussed and shown in Fig. 15. The threshold voltage is susceptible to process variation since it is connected with a large number of factors like the flat-band voltage (V_{FB}), channel doping concentration (N_{sub}), oxide thickness (t_{ox}) or length (dL) and width (dW) offsets.

Figure 18 shows the distributions for some of the parameters related to the shift of the optimum inversion level. Note that the parameter λ_c and the mobility μ_0 have almost identical distributions with a correlation factor of 0.99, which is to be anticipated since these two parameters are linearly related as mentioned earlier.

The overlap capacitance C_{ovlgd} (the same applies for C_{ovlgs}) is strongly related to oxide thickness (t_{ox}) and the length offset (dL) with correlation factors -0.99 and -0.98, respectively. The statistics also show that the overlap capacitances and the width offset are also linked but with a lower value at 0.72.

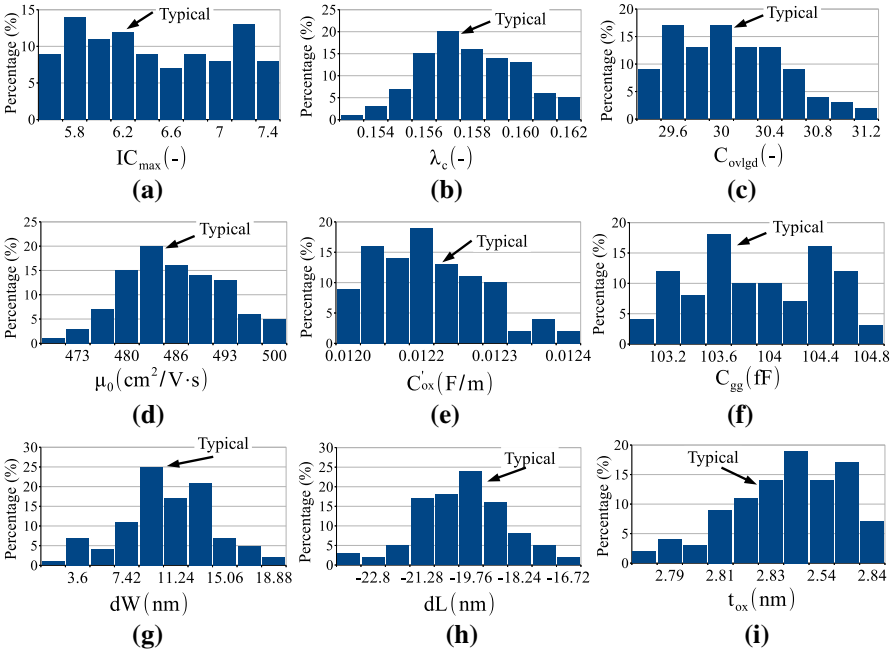

Fig. 18 The distribution of main MOS parameters related to FoM shift. **a** Inversion level of the FoM peak, **b** the parameter λ_c that accounts for velocity saturation, **c** gate–drain overlap capacitance, **d** electron mobility, **e** oxide capacitance, **f** total gate capacitance, **g** MOS width offset, **h** MOS length offset, **i** MOS oxide thickness

Finally, the correlation factors among oxide thickness, width and length offsets on the one hand, and threshold voltage, on the other, amount to 0.83, −0.99 and 0.83, respectively. This result is expected from the above discussion.

7.3 Voltage and Temperature Response

The final step to create a complete picture for the behaviour of the LNA is the voltage and temperature investigation. Figure 19 illustrates the simulation of the circuit for different operating conditions; temperatures ranging from −45 °C up to 80 °C as well as supply voltages with values from 0.80 to 1.30 V. The first figure shows the noise performance for different temperature values. Since the thermal noise is proportional to temperature, the noise figure is minimum at low temperatures as expected.

Figure 19b shows the input matching response for different supply voltages and temperatures. While the temperature rises, the input matching improves and saturates to an almost constant value at around 50 °C. The small-signal gain shows the opposite response; the S_{21} value is almost constant for cold temperatures and degrades as the temperature rises. Regarding the supply voltage, the small-signal gain experiences a rise for larger supply voltages as expected. On the contrary, the input matching is better for lesser voltages.

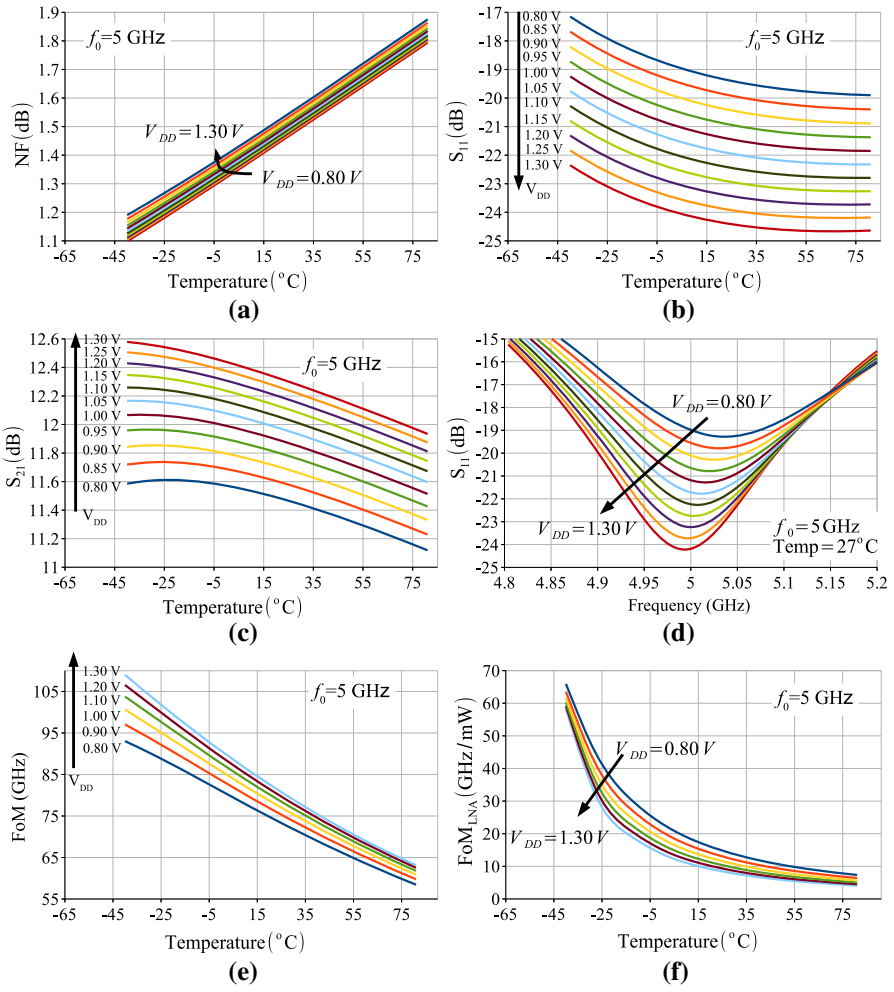

Fig. 19 Supply voltage and temperature analysis of the common source 5 GHz LNA. **a** Noise figure versus temperature, **b** S_{11} versus temperature, **c** S_{21} versus temperature, **d** frequency response of the S_{11} parameter for different supply voltages, **e** figure of merit versus temperature, **f** FoM_{LNA} versus temperature. All figures cover supply voltage values from 0.8 to 1.3 V

Furthermore, Fig. 19d illustrates the frequency response of the input matching network for the nominal temperature (27 °C) and for different supply voltages. It can be seen that there is a strong dependence of the input matching and supply voltage. Since V_{DD} is one the main factors that dictate the operating point of the transistor, different V_{DD} values lead to different intrinsic and extrinsic capacitance values which play a significant role in the balance of the fragile input matching network.

Finally, Fig. 19e presents the study of the selected figure of merit as a function of temperature and supply voltage. It can be seen that the figure of merit shows better results when the temperature is low and the supply voltage high. Considering that

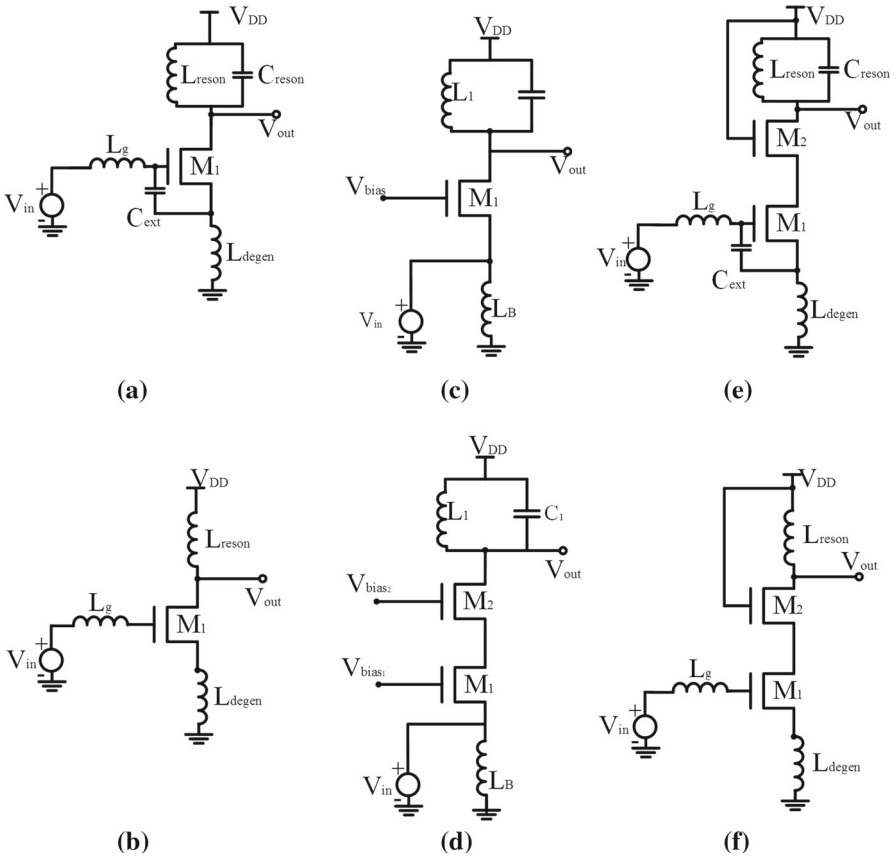

Fig. 20 Different LNA topologies and variations. **a** Narrowband common source LNA (CS_1), **b** wideband common source LNA (CS_2), **c** common gate LNA (CG_1), **d** cascode common gate LNA (CG_1), **e** narrowband cascode common source LNA (CCS_1), **f** wideband cascode common source LNA (CCS_2)

the typical LNA figure of merit is proportional to the selected figure of merit, their behaviour is similar for different temperatures and supply voltages as seen in Fig. 19f.

8 Discussion of Different LNA Topologies

The combination of analytical model, circuit analysis and genetic algorithm can also be used for the design of different LNA topologies. Figure 20 illustrates six different simple single-stage LNA designs. There are three topologies and two variations of each topology; (a) and (b) are common source LNAs, (c) and (d) are common gate LNAs and finally, (e) and (f) are cascode common source LNAs. Each circuit shows different strengths and weaknesses; therefore, the fitness function has to be adjusted so the genetic algorithm can provide the desired results. For example, it is known that the common gate topologies cannot provide ideal input matching conditions and

low-noise figure simultaneously. The advantage of the common gate topology though resides in its high linearity and wideband response. In essence, the choice of the weighting parameters which is different for each topology pertains to the experience of the designer as well as overall constraints.

The chromosomes of the genetic algorithm also have to be adjusted for each topology. In the case of the common gate amplifiers, the load resistance is an important parameter in the design procedure as it is used to dictate the gain and the noise figure. The load resistance is actually the resonator inductor parasitic resistance which cannot be known beforehand. During the genetic optimization procedure the inductance value might change significantly to achieve the desired parasitic (load) resistance and match the specified gain or noise performance. Since the inductance changes significantly from the initial calculation, the load capacitor also has to change accordingly to tune the amplifier at the specified frequency. Consequently, the common gate circuits (CG_1) and (CG_2) cannot be optimized with fixed capacitor values which have to be incorporated in the optimization procedure. Additionally, the bias voltages for the transistors in the common gate circuits also have to be in the optimization procedure. All these design-related issues lead to a chromosome with many more genes than any other topology which in turn leads to increasing computing time.

In addition to these six single-stage LNA designs, Fig. 21 shows two additional more complex LNA designs, namely an ultra-wideband distributed amplifier and an ultra-wideband two-stage resistive feedback amplifier. The design procedure for these complex amplifiers is initiated by computing the parameter values using the analytical methodology. The following stages are designed according to the bandwidth, gain and noise figure specifications as seen in [11]. Since these topologies are comprised of a large number of components, the chromosomes of the genetic optimizer are substantially more crowded than the designs of Fig. 20 resulting in a more time-consuming optimization procedure. Indicatively, the distributed amplifier of Fig. 21a requires approximately 800 generations to optimize 33 design variables including the transistor width parameters, input and interstage matching components, and parameters for the tuning inductors.

The simulation results of all these designs are summarized in Table 3. The grey scale shading indicates the relative performance for each parameter (lighter meaning better). The single-stage circuits that do not have an L–C tank at the output node show a wider bandwidth as expected. Common gate topologies underperform on the S_{11} and S_{21} parameters but show high linearity; conversely, the cascode common source LNAs show high gain and good matching but lack in linearity. Regarding noise performance, the common source LNA of the case study (CS_1) dominates the other designs, where the common gate and the wideband common source LNAs are not so potent. Furthermore, complex topologies show significantly higher small-signal gain, satisfactory noise figure and large bandwidth. On the contrary, these topologies lack on the input/output matching parameters, are highly nonlinear and show high power consumption. The commonly used LNA figure of merit of (1) shows that the best performing simple design is the wideband cascode common source LNA with the LNA of the case study close second. The complex topologies show adequate FoM_{LNA} results, and especially the two-stage amplifier shows the best FoM of all the designs. The interpretation of this figure of merit requires some care. For instance, the figure

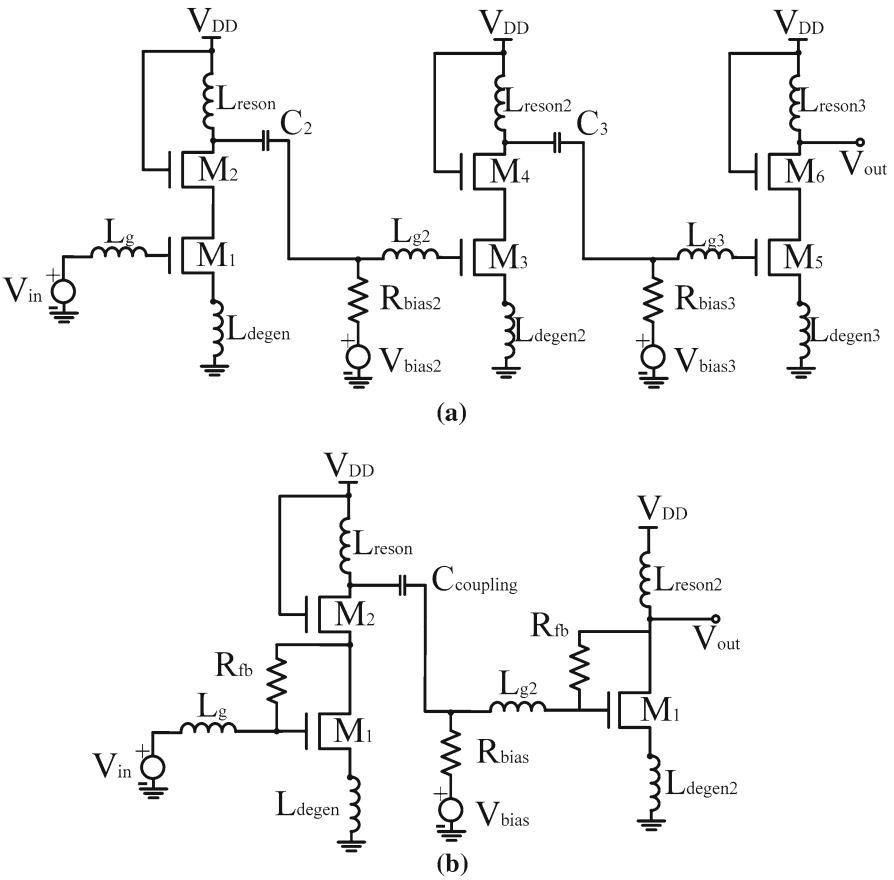

Fig. 21 **a** Distributed ultra-wideband three-stage low-noise amplifier (3SD), **b** ultra-wideband two-stage resistive shunt feedback low-noise amplifier (2SR)

Table 3 Performance results of the LNA designs of Fig. 20

Topology (simple)	S_{11} (dB)	S_{21} (dB)	S_{22} (dB)	NF (dB)	1-dB compression (dBm)	I_D (mA)	FoM_{LNA} (GHz/mW)	BW (GHz)
CS_1	–23.2	13.20	–20.5	1.48	–0.60	11.50	10.0	1.21
CS_2	–15.12	12.11	–15.57	2.12	–1.90	20.47	2.65	2.78
CG_1	–5.20	4.63	–10.50	1.97	>10	29.12	0.82	3.36
CG_2	–3	3.17	–2.69	2.90	9.26	9.77	0.85	3.22
CCS_1	–18.61	12.40	–6.41	1.89	–9.55	16.22	4.23	0.89
CCS_2	–21.4	18.11	–11.05	1.79	–9.12	11.01	10.4	3.10
Topology (complex)	S_{11} (dB)	S_{21} (dB)	S_{22} (dB)	NF (dB)	1–dB compression (dBm)	I_D (mA)	FoM_{LNA} (GHz/mW)	BW (GHz)
3SD	–16.1	30.43	–1.83	1.70	–20.2	25.1	8.65	5.1
2SR	–10.1	30.80	–13.01	1.44	–22.1	30.1	11.6	5.4

of merit does not distinguish among wideband and narrowband designs and does not include linearity or area of the design. Consequently, the common gate designs show the worst performance of all the simple topologies.

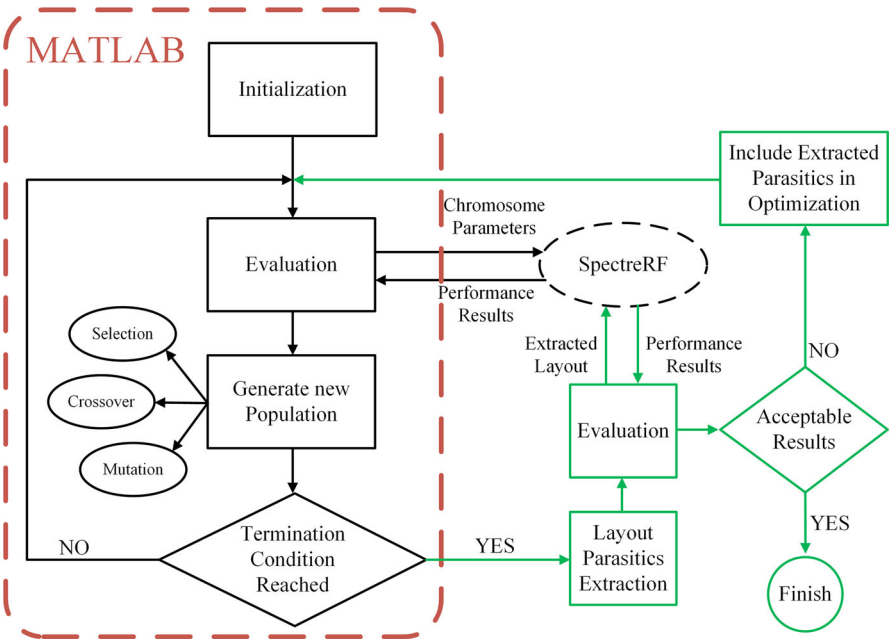

Fig. 22 The expanded flowchart of the methodology that includes the layout parasitics extraction procedure in the optimization sequence. The *green lines* correspond to the additional steps required for the layout optimization

The different LNA designs of this section have proved the versatility of the optimization procedure, since it has been applied to simple single-stage LNAs for narrowband or wideband applications and additionally, to more complex designs with an ultra-wideband response. The procedure may be applied to different topologies as well, with the appropriate chromosome and fitness function adjustments. The optimization methodology—at this state—is not directly applicable as is to multi-standard LNA designs [10] and could be the object of a separate study.

Finally, the methodology can be expanded to include the layout place and routing procedures of the LNA. During the layout design, additional parasitic components appear due to the interconnections between the components. These layout dependent parasitics mainly lead to slightly mistuned amplifiers, gain losses and unmatched input/output. Typically, the S-parameters show a slight shift to lower frequencies and reduced gain. Additionally, the noise performance is worsening and the frequency of the lowest noise figure also offsets. This S-parameter behaviour, if not addressed, not only affects the noise and gain performance, but may also lead to instability issues which makes the amplifier unusable.

The flowchart of the expanded methodology is shown in Fig. 22 where the green lines correspond to the additional steps for the layout optimization. After the convergence of the genetic algorithm, the layout place and routing as well as the parasitics extraction, SpectreRF circuit simulator performs the post-layout simulations. If the performance results are not adequate, then the next step is to model the extracted

Table 4 Comparison of CMOS LNA designs

References	LNA topology	Process (nm)	S_{11} (dB)	S_{21} (dB)	S_{22} (dB)	NF (dB)	Supply (V)	Power (mW)	Frequency (GHz)	FoM_{LNA} (GHz/mW)
[30][a]	Cascode CS	180	−10.0	9.30	−12.0	2.80	1.5	30.0	5.0	0.86
[37][a]	Cascode CS	90	−10.1	12.3	−14.3	2.70	1.2	–	5.5	–
[20][a]	Differential	65	−13.0	25.6	–	2.50	1.2/1.8	55.0	1.7	0.52
[15][a]	Differential	32	−29.0	12.0	–	3.50	1.8	19.8	2.5	0.66
[28][b]	Current reused	130	−18.6	28.0	–	2.46	1.2	1.00	2.4	46.0
[18][b]	Cascode CS	180	−14.0	12.5	−16.0	4.50	0.6	0.32	5.0	54
[25][a]	Differential	40	−18.0	38.7	–	3.50	1.1	53.0	2.5	0.73
[9][a]	Differential	90	−23.0	15.0	−23.0	3.20	1.8	15.3	5.2	2.31
This work[b]	CS	90	−23.2	13.2	−20.5	1.48	1.2	13.8	5.0	10.0

[a] Measurements
[b] Pre-layout simulations

parasitics and include them in the initial design. Afterwards, the genetic algorithm is called again and attempts to find the new optimum design that embeds the extracted parasitics. This procedure is then repeated until the specifications are met.

9 Conclusion

This paper introduces a low-power RF LNA design methodology that incorporates the use of an analytical model and a genetic algorithm, to produce optimum results. The performance of the circuit is quantified by the figure of merit $g_m f_t / i_d$, which suggests that the optimum operation region is found in the moderate inversion, a notion that is verified by the measurements and the simulated results. A new analytical model has been developed for the thermal noise excess noise factor γ_n in terms of the inversion charge or inversion coefficient, which may prove highly useful in many circuit analyses. The design procedure begins with the knowledge of the optimum operation region and afterwards the genetic algorithm uses a multi-objective fitness function to optimize not only the selected figure of merit, but also additional key performance parameters in an RF LNA. The proposed design methodology has been illustrated for a common source LNA, and the method has been shown to be effective in achieving well-balanced, low-power RF amplifiers. Furthermore, the optimization technique has been demonstrated for single-stage narrowband or wideband topologies, to multi-stage ultra-wideband LNAs topologies.

The behaviour of the LNA over process variation has also been discussed leading to useful information about the correlations of the performance parameters. The selected figure of merit still shows that the optimum operation region is the moderate inversion, but the exact inversion level cannot be known beforehand, like the typical case. It has been proved that the main concern for the optimum-inversion-level shift is the variation of the active device since Monte Carlo simulations for the passive components show only a slight impact on the FoM. Temperature and supply voltage variations have also been discussed furthering the understanding of the LNA for various conditions.

Finally, to compare the optimized LNA with similar works, Table 4 presents the results of the common source LNA with inductive degeneration of the case study with other LNA implementations found in the literature. The table clearly shows that the proposed design methodology has proven its capability to produce satisfactory results, with exceptional noise performance, adequate gain and decent input/output matching.

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