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# A Unified Delay, Power and Crosstalk Model for Current Mode Signaling Multiwall Carbon Nanotube Interconnects

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**Abstract** Multiwall carbon nanotube (MWCNT) has been investigated as a potential interconnect material for future advanced technology nodes. The present paper analyzes performance of MWCNT interconnects using current mode signaling (CMS) scheme. The novelty of the present work can be stated as: Firstly, a unified model is proposed for both copper and MWCNT interconnects using finite-difference time-domain (FDTD) technique. Secondly, this model is applicable for both the conventional voltage mode signaling and more versatile CMS schemes. Furthermore, the presented FDTD-based model is valid for single as well as $M$-line coupled interconnects in integrated circuits. The model also incorporates CMOS gate as driver for MWCNT interconnect. Thirdly, power model using FDTD technique is investigated for the first time. Accurate formulation and computation of power dissipation in CMS MWCNT interconnects are presented in the paper. Propagation delay, power dissipation and power_delay_product (PDP) are the performance metrics considered for single-line CMS MWCNT interconnect. Crosstalk is analyzed for 2-Line and 5-Line coupled interconnects. It is investigated that CMS scheme leads to about 4 times lesser propagation delay and 2.5 times reduced PDP in MWCNT interconnect than the conventional copper interconnect for interconnect length of 4500 μm. The technology node consid-

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ered is 32 nm. The response of the system is accurately computed using the proposed FDTD-based model. The maximum percentage error between results obtained by the proposed analytical model and SPICE simulation model is $<3\%$ for the various test cases.

**Keywords** Complementary metal-oxide semiconductor · Current mode signaling · Finite-difference time-domain (FDTD) · Multiwall carbon nanotube (MWCNT) · On-chip interconnect

## 1 Introduction

The tetravalent and member of group XIV of the periodic table, carbon, forms various allotropes. The most common allotropes of carbon are diamond (in which carbon atoms are $sp^3$ bonded with each other and arranged in tetrahedral lattice structure), graphite (where arrangement of $sp^2$ bonded carbon atoms are arranged as sheets of hexagonal lattice), graphene (which is a monolayer of graphite and consists of a single hexagonal layer of $sp^2$ bonded carbon atoms) and fullerene (where carbon atoms are $sp^2$ bonded with each other and are arranged in spherical or ellipsoidal shape) [20,31]. Graphene-based carbon nanotube (CNT) and graphene nanoribbon (GNR) are other few nanomaterials that have recently gained much attention in microelectronics/nanoelectronics applications [5]. This is due to their high current carrying capability, remarkable physical strength, high mean free path and long ballistic transport length, high thermal conductivity and high mechanical and thermal stability [3,16,26,27,36,38].

CNTs comprise of graphene sheets that are rolled-up as hollow cylindrical tube. Depending on the rolled-up direction (chirality) of graphene sheets, CNTs exhibit different structures and properties. The chirality in CNTs is defined by circumferential vector $\vec{C}$. $\vec{C}$ is expressed as $\vec{C} = p \cdot \hat{a}_1 + q \cdot \hat{a}_2$, where $\hat{a}_1$ and $\hat{a}_2$ are lattice vectors, and $p$ and $q$ are chiral indices [20]. Based on chiral indices $(p, q)$ values, CNTs manifest different structures as chiral or achiral. For chiral CNT structures, the chiral indices are not equal ($p \neq q$). The chiral CNTs are mostly semiconductive in nature. On the other hand, achiral CNTs are categorized as armchair ($p = q$) and zigzag ($p = 0$ or $q = 0$) [22]. Armchair CNTs are always metallic in nature, whereas zigzag CNTs can be either metallic or semiconductive in nature depending on the chiral indices [38]. For interconnect applications, metallic CNTs are useful. CNTs can be also broadly classified as single-wall carbon nanotube (SWCNT) and multiwall carbon nanotube (MWCNT). SWCNT has only one shell with diameter ranging from 0.4 to 4 nm. MWCNT has several concentric shells, and diameter of the shells varies from several nanometers to tens of nanometers [23]. The large diameter of MWCNTs results in long electron mean free path and large number of conducting channels. As against to SWCNT, MWCNT is always metallic in nature because of large diameter of shells and their contribution in conduction even if these are of semiconductive chirality [36]. MWCNTs and SWCNTs (metallic nature) have similar current carrying capability. However, MWCNTs are easier to fabricate due to better control over growth process [22]. In [11,22,23,25,31], it is reported that performance of MWCNT at global interconnect levels is better as compared to copper and SWCNT interconnects.

MWCNT interconnect is hence one of the promising and potential candidate for future on-chip VLSI interconnections in integrated circuit designs.

Several researches have been performed on MWCNT interconnects [11,19,20,22,23,25,31,36]. Naeemi et al. [25] have given physics-based circuit models for MWCNT interconnects in. In [11,22], performance comparison has been shown in between MWCNT, SWCNT and copper interconnects using simulation-based model. However, no mathematical formulation has been presented for the performance analyses of these structures. In [31], performance of CNT interconnect has been evaluated using *RC*-based model. However, the accuracy of this model has been limited as at high frequencies inductance becomes significant and interconnects need to be modeled as transmission line model. For accurate analysis of driver-interconnect-load (DIL) system, interconnect driver has to be modeled carefully. In [19,23], crosstalk modeling of MWCNT interconnect has been performed using finite-difference time-domain (FDTD) method. In these methods, nonlinear CMOS gate driver has been approximated by linear resistive and capacitive elements. This approximation, however, leads to less accurate results as CMOS gate operates partially in linear and saturation regions during signal transition periods, and therefore, CMOS gate cannot be approximated by single lumped elements for different regions of operation of MOS transistors in a CMOS gate. Similarly, in [22,31,36] resistive driver model has been used. Moreover, analytical formulation for power computation has not been presented in any of these research papers.

Until now, majority of the research work in carbon nanomaterial based interconnects has been implemented and analyzed using voltage mode signaling (VMS) scheme. The voltage swing in VMS scheme is full rail-to-rail. On the contrary, voltage swing over interconnects is smaller in current mode signaling (CMS) [2]. The advantage of CMS scheme is smaller latency and higher bandwidth [7,37,40]. Low voltage swing in CMS scheme is achieved by providing small load impedance termination. This is effective realized by incorporating specialized current mode receiver circuits [2,12,40]. CMS scheme has been explored for copper interconnects [1,2,4,12,37,40]. However, no significant work has been reported in literature for carbon nanomaterial-based interconnects. Hence, analysis of MWCNT interconnects using CMS scheme has become significant and considered in the present research work.

The present work gives a unified model for copper and MWCNT interconnects. This model is applicable for both VMS and CMS schemes as well. The paper comprises of five sections. The current section briefly reviews work related to MWCNT interconnects. In Sect. 2, a unified DIL model for copper and MWCNT interconnects using VMS and CMS schemes is proposed. Analytical model using FDTD technique is formulated in Sect. 3. Performance analyses of copper and MWCNT interconnects for VMS and CMS schemes are presented in Sect. 4. Finally, conclusion is drawn in Sect. 5.

## 2 Unified DIL Model for Copper and MWCNT Interconnects

A unified DIL model for copper and MWCNT interconnects using VMS and CMS schemes is presented in Fig. 1. The driver is implemented using CMOS gate. In [22], MWCNT interconnect is modeled by multiconductor circuit (MCC). Using this model,

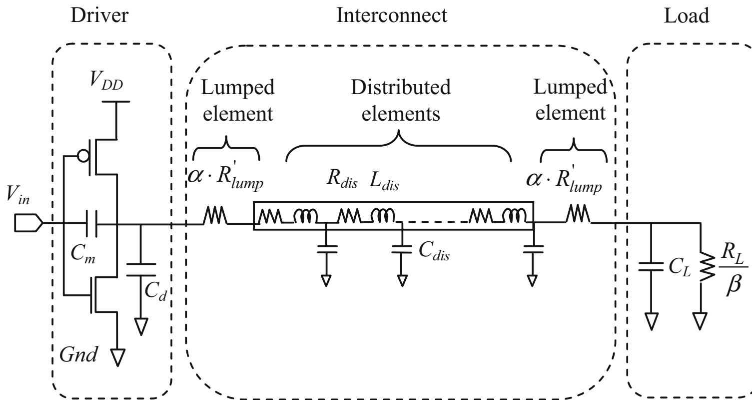


**Fig. 1** Unified driver-interconnect-load (DIL) model for copper and MWCNT interconnects using VMS and CMS schemes

MWCNT interconnect with $N$ number of shells leads to computationally expensive $2N$ system dimensional differential equations solution [19]. This is mitigated by using simplified equivalent single conductor (ESC) model [33] and is considered for the present analysis. In the figure, parameter $\alpha$ determines the interconnect materials. It is '0' for copper and '1' for MWCNT. The load impedance termination in VMS is high and often implemented using CMOS gate. It is equivalently modeled by load capacitance ($C_{\mathrm{L}}$) [19,22,23,31,36]. In CMS scheme, impedance termination to interconnect is smaller and current mode receiver is equivalently modeled by load resistance ($R_{\mathrm{L}}$) and $C_{\mathrm{L}}$ [1,4,37]. Parameter $\beta$ defines the signaling schemes in the proposed DIL model. It is '0' for VMS and '1' for CMS scheme.

The schematic of MWCNT interconnect with $N$ number of shells is illustrated in Fig. 2. $d_1$ and $d_N$ are diameters of the innermost and outermost shells of MWCNT interconnect. $\delta$ is the Van der Waal's gap (0.34 nm) and represents distance between two neighboring concentric shells [20].

The number of shells ($N_{\text{shell}}$) in MWCNT is given as [19]

$$N_{\text{shell}} = 1 + \text{Integer}\left(\frac{d_N - d_1}{2\delta}\right) \tag{1}$$

The number of conduction channels ($N_{\text{ch}}$) in MWCNT is obtained as [25]

$$N_{\text{ch}}^{i} \approx \begin{pmatrix} k_1 T d_i + k_2; & d_i > d_{\mathrm{T}}/T \\ 2/3; & d_i < d_{\mathrm{T}}/T \end{pmatrix} \tag{2}$$

where $i$ represents the shell number and varies from 1 to $N$. $d_i$ is the diameter of $i$th shell in MWCNT. $d_T$ is the function of gap between sub-bands and thermal energy of electrons and is equal to 1300 nm K at room temperature. $T$ denotes temperature. $k_1$ and $k_2$ are curve fitted parameters and equal to $3.87 \times 10^{-4}$ nm$^{-1}$ K$^{-1}$ and 0.2, respectively [25].

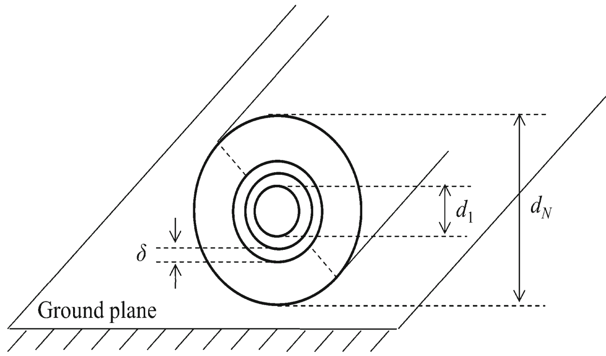


**Fig. 2** Schematic of MWCNT with $N$ shells above ground plane

The MWCNT interconnect represented by ESC model is presented in Fig. 1. It comprises of various interconnect parasitic elements which are formulated in "Appendix 1." The copper interconnects parasitics are obtained using the formulations presented in "Appendix 2."

## 3 Analytical Model Formulation Using FDTD Technique

A unified model for $M$-Line coupled copper and MWCNT interconnects is shown in Fig. 3. $N_0$, $N_1$,..., $N_Nz+2$ represent node points in Fig. 3. The input voltage $[V_{\text{in}}]$, NMOS $[I_n]$ and PMOS $[I_p]$ drain currents are defined as

$$[V_{\text{in}}] = \begin{bmatrix} V_{\text{in}}(1) \\ V_{\text{in}}(2) \\ \vdots \\ V_{\text{in}}(M) \end{bmatrix}, \quad [I_n] = \begin{bmatrix} I_n(1) \\ I_n(2) \\ \vdots \\ I_n(M) \end{bmatrix}, \quad [I_p] = \begin{bmatrix} I_p(1) \\ I_p(2) \\ \vdots \\ I_p(M) \end{bmatrix} \tag{3}$$

The drain diffusion capacitance $[C_d]$, gate-drain coupling capacitance $[C_m]$, load capacitance $[C_{\text{L}}]$, load resistance $[R_{\text{L}}]$ and lumped resistance $[R'_{\text{lump}}]$ are $M$ x $M$ diagonal matrices and expressed as

$$\begin{aligned} &[C_m] = \text{diag}\left[C_m^1, C_m^2, \ldots, C_m^M\right], \\ &[C_{\text{d}}] = \text{diag}\left[C_{\text{d}}^1, C_{\text{d}}^2, \ldots, C_{\text{d}}^M\right], \\ &[C_{\text{L}}] = \text{diag}\left[C_{\text{L}}^1, C_{\text{L}}^2, \ldots, C_{\text{L}}^M\right], \\ &[R_{\text{L}}] = \text{diag}\left[R_{\text{L}}^1, R_{\text{L}}^2, \ldots, R_{\text{L}}^M\right], \\ &\left[R'_{\text{lump}}\right] = \text{diag}\left[R'^1_{\text{lump}}, R'^2_{\text{lump}}, \ldots, R'^M_{\text{lump}}\right] \end{aligned} \tag{4}$$

The interconnects are driven by CMOS gates. The voltage, current and distributed interconnect elements of the ESC model can be modeled using Telegraph's equations. This is presented in "Appendix 3."

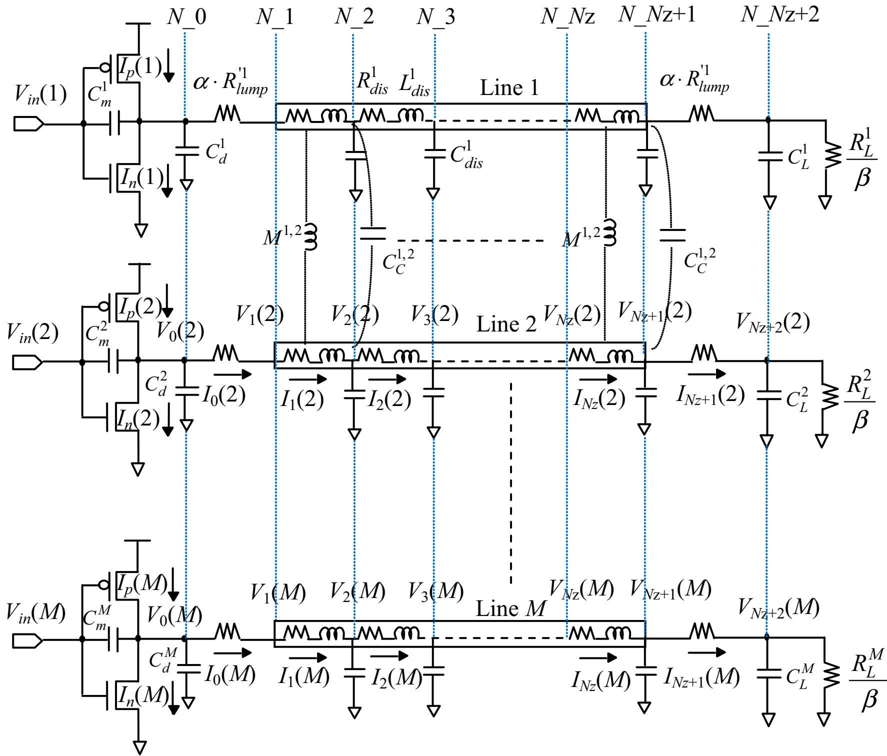


**Fig. 3** Unified model for $M$-Line coupled CMOS gate-driven copper and MWCNT interconnects

### 3.1 DIL Modeling Using FDTD Technique

The analytical model formulation using FDTD technique is carried out in the following subsections:

#### *3.1.1 Formulation of Recursive Equations for Computation of Currents and Voltages Along the Length of Interconnect*

The differential Telegraph's expressions as represented by (60) and (61) in "Appendix 3" are discretized into difference expressions. The discretization is performed in spatial and temporal domains. This is illustrated in Fig. 4. The discretized voltage and current variables are evaluated alternatively and are separated by $\Delta t/2$ and $\Delta z/2$ in time and position, respectively. $\Delta t$ and $\Delta z$ are infinitesimal small time step and distance in temporal and spatial domains, respectively. These are governed by Courant condition [39] and defined as:

$$\Delta t \leq \Delta z/v \tag{5}$$

where $v$ is phase velocity.

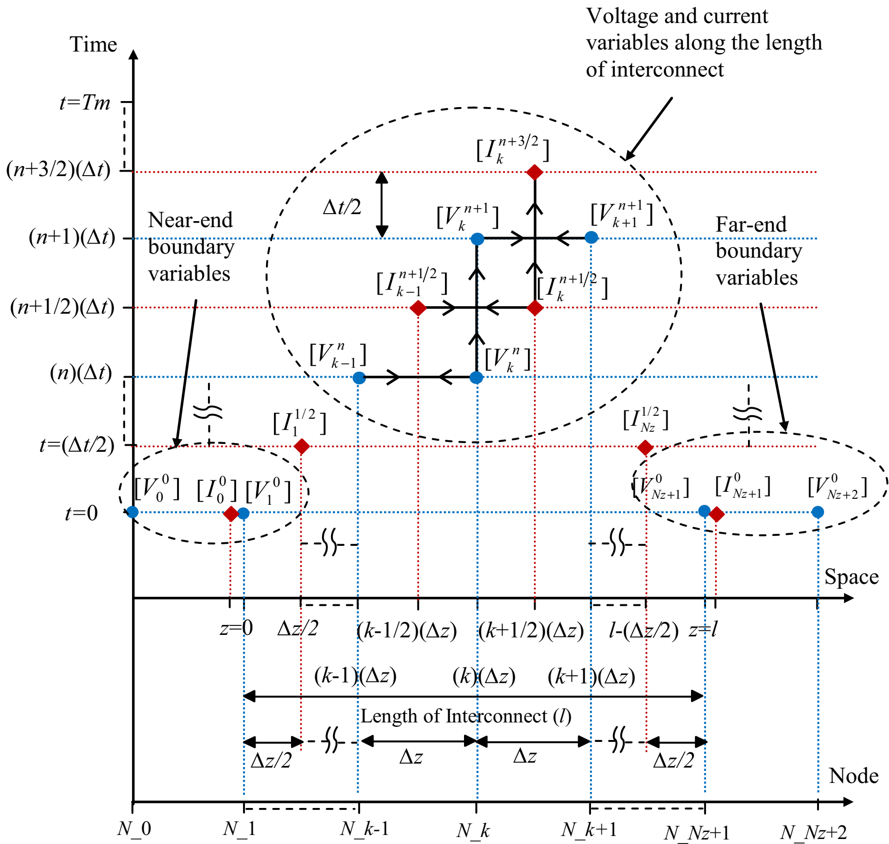


**Fig. 4** Voltage and current discretization in spatial, nodal and temporal domains

The discretized voltage and current at any instant of time and position in Fig. 4 are defined as

$$\left[V_k^n\right] \equiv [V] \quad (k\Delta z, n\Delta t) \tag{6}$$

$$\left[I_k^{n+1/2}\right] \equiv [I] \quad ((k+1/2)\,\Delta z, (n+1/2)\,\Delta t) \tag{7}$$

where $k$ and $n$ are positive integer values.

The Telegraph's first differential equation represented by Eq. (60) in "Appendix 3" is discretized as

$$\left[\frac{\left[V_{k+1}^{n+1}\right]-\left[V_k^{n+1}\right]}{\Delta z}+[L]\left(\frac{\left[I_k^{n+3/2}\right]-\left[I_k^{n+1/2}\right]}{\Delta t}\right)\right.$$
$$\left.+[R]\left(\frac{\left[I_k^{n+3/2}\right]+\left[I_k^{n+1/2}\right]}{2}\right)\right]=0 \tag{8}$$

Simplifying (8) gives:

$$\left[I_k^{n+3/2}\right] = [B]\,[D]\left[I_k^{n+1/2}\right] + [B]\left(\left[V_k^{n+1}\right] - \left[V_{k+1}^{n+1}\right]\right) \tag{9}$$

where $[B] = \left(\frac{\Delta z}{\Delta t}\,[L] + \frac{\Delta z}{2}\,[R]\right)^{-1}$, $[D] = \left(\frac{\Delta z}{\Delta t}\,[L] - \frac{\Delta z}{2}\,[R]\right)$, $k = 1, 2, 3, \ldots, Nz$.

Similarly, discretizing second Telegraph's equation [Eq. (61) in "Appendix 3"] results in

$$\frac{\left[I_k^{n+1/2}\right] - \left[I_{k-1}^{n+1/2}\right]}{\Delta z} + [C]\,\frac{\left[V_k^{n+1}\right] - \left[V_k^{n}\right]}{\Delta t} = 0 \tag{10}$$

Equation (10) is further solved as

$$\left[V_k^{n+1}\right] = \left[V_k^{n}\right] + [A]\left(\left[I_{k-1}^{n+1/2}\right] - \left[I_k^{n+1/2}\right]\right) \tag{11}$$

where $[A] = \left(\frac{\Delta t}{\Delta z} \cdot \frac{1}{[C]}\right)$, $k = 2, 3, 4, \ldots, Nz$.

Equations (9) and (11) are the recursive expressions to evaluate current and voltage along interconnects. The node voltages and branch currents along interconnect depend on the near-end and far-end boundary conditions. These are formulated in the following subsections.

### *3.1.2 Formulation of Near-End Boundary Condition*

The near-end boundary condition is defined by $[V_0]$, $[V_1]$ and $[I_0]$ at nodes$N_0$ and $N_1$. Using KCL, $[I_0]$ is obtained as

$$\left[I_0^{n+1}\right] = \left[I_p^{n+1}\right] - \left[I_n^{n+1}\right] + [C_m]\left(\frac{\left[V_{\text{in}}^{n+1}\right] - \left[V_{\text{in}}^{n}\right]}{\Delta t}\right) - [C_m + C_{\text{d}}]\left(\frac{\left[V_0^{n+1}\right] - \left[V_0^{n}\right]}{\Delta t}\right) \tag{12}$$

$\left[I_n^{n+1}\right]$ and $\left[I_p^{n+1}\right]$ are characterized by $n$th power law model [32]
The near-end voltage $[V_0]$ is derived using Ohm's law as

$$\left[V_0^{n+1}\right] = \left[V_1^{n+1}\right] + \alpha\left[R'_{\text{lump}}\right] \cdot \left[I_0^{n+1}\right] \tag{13}$$

Using (12) and (13) gives

$$\left[I_0^{n+1}\right] = [H] \left( \begin{array}{l} \left[I_p^{n+1}\right] - \left[I_n^{n+1}\right] + [C_m] \left( \frac{\left[V_{\text{in}}^{n+1}\right] - \left[V_{\text{in}}^n\right]}{\Delta t} \right) - ([C_m] + [C_{\text{d}}]) \left( \frac{\left[V_1^{n+1}\right] - \left[V_1^n\right]}{\Delta t} \right) \\ + \alpha \left[R'_{\text{lump}}\right] ([C_m] + [C_{\text{d}}]) \left( \frac{\left[I_0^n\right]}{\Delta t} \right) \end{array} \right) \tag{14}$$

where

$$[H] = \left( U + \frac{\alpha \left[R'_{\text{lump}}\right] ([C_m] + [C_{\text{d}}])}{\Delta t} \right)^{-1} \tag{15}$$

$U$ is a $M \times M$ unity matrix.

The voltage at node $N_1$ $\left(\text{i.e., } \left[V_1^{n+1}\right]\right)$ is expressed by substituting $k = 1$ in (11) as

$$\left[V_1^{n+1}\right] = \left[V_1^n\right] + 2[A] \left( \left[I_0^{n+1/2}\right] - \left[I_1^{n+1/2}\right] \right) \tag{16}$$

Here $\Delta z$ is replaced by $\Delta z/2$ in $[A]$ since the current at node $N_0$ and $N_1$ are separated by $\Delta z/2$ [1].

$\left[I_0^{n+1/2}\right]$ can be defined as

$$\left[I_0^{n+1/2}\right] = \frac{\left[I_0^n\right] + \left[I_0^{n+1}\right]}{2} \tag{17}$$

Using (16) and (17), $\left[V_1^{n+1}\right]$ is simplified as

$$\left[V_1^{n+1}\right] = \left[V_1^n\right] + 2[A] \left( \frac{\left[I_0^n\right] + \left[I_0^{n+1}\right]}{2} - \left[I_1^{n+1/2}\right] \right) \tag{18}$$

Substituting (14) in (18), gives

$$\left[V_1^{n+1}\right] = \left( \begin{array}{l} \left[V_1^n\right] - 2[E][A]\left[I_1^{n+1/2}\right] + [E][A][H] \left( \left[I_p^{n+1}\right] - \left[I_n^{n+1}\right] \right) \\ + [E][A][H] \left\{ [C_m] \left( \frac{\left[V_{\text{in}}^{n+1}\right] - \left[V_{\text{in}}^n\right]}{\Delta t} \right) + \left( \frac{U}{[H]} + \frac{\alpha \left[R'_{\text{lump}}\right]([C_m] + [C_{\text{d}}])}{\Delta t} \right) \left[I_0^n\right] \right\} \end{array} \right) \tag{19}$$

where

$$[E] = \left( U + \frac{[A]\,[H]\,([C_m] + [C_\mathrm{d}])}{\Delta t} \right)^{-1} \tag{20}$$

Equations (13), (14) and (19) are used to compute voltage and current variables at near-end boundary condition.

*3.1.3 Formulation of Far-End Boundary Condition*

The far-end boundary condition is defined by $[V_{Nz+1}]$, $[V_{Nz+2}]$ and $[I_{Nz+1}]$ at nodes$N_N$z+1 and $N_N$z+2.

$\left[I_{Nz+1}^{n+1}\right]$ can be evaluated by applying KCL at node $N_Nz$+2 as

$$\left[I_{Nz+1}^{n+1}\right] = [C_\mathrm{L}] \left( \frac{\left[V_{Nz+2}^{n+1}\right] - \left[V_{Nz+2}^{n}\right]}{\Delta t} \right) + \frac{\beta \left[V_{Nz+2}^{n+1}\right]}{[R_\mathrm{L}]} \tag{21}$$

Using Ohm's law, far-end voltage $\left[V_{Nz+2}^{n+1}\right]$ is computed as

$$\left[V_{Nz+2}^{n+1}\right] = \left[V_{Nz+1}^{n+1}\right] - \alpha \left[R'_\mathrm{lump}\right] \cdot \left[I_{Nz+1}^{n+1}\right] \tag{22}$$

Substituting (22) in (21) gives

$$\left[I_{Nz+1}^{n+1}\right] = [J] \left( \left( \frac{\alpha \left[R'_\mathrm{lump}\right] [C_\mathrm{L}]}{\Delta t} \right) \left[I_{Nz+1}^{n}\right] + \left( \frac{[C_\mathrm{L}]}{\Delta t} + \frac{\beta}{[R_\mathrm{L}]} \right) \left[V_{Nz+1}^{n+1}\right] - \left( \frac{[C_\mathrm{L}]}{\Delta t} \right) \left[V_{Nz+1}^{n}\right] \right) \tag{23}$$

where

$$[J] = \left( U + \frac{\alpha \left[R'_\mathrm{lump}\right] [C_\mathrm{L}]}{\Delta t} + \frac{\alpha \beta \left[R'_\mathrm{lump}\right]}{[R_\mathrm{L}]} \right)^{-1} \tag{24}$$

The voltage at node $N_Nz + 1$ $\left(\text{i.e., } \left[V_{Nz+1}^{n+1}\right]\right)$ is computed from recursive voltage expression (11) by substituting $k = Nz + 1$. Here also $\Delta z$ is replaced by $\Delta z/2$ in $[A]$.

$$\left[V_{Nz+1}^{n+1}\right] = \left[V_{Nz+1}^{n}\right] + 2\,[A] \left( \left[I_{Nz}^{n+1/2}\right] - \left[I_{Nz+1}^{n+1/2}\right] \right) \tag{25}$$

where

$$\left[I_{Nz+1}^{n+1/2}\right] = \frac{\left[I_{Nz+1}^{n}\right] + \left[I_{Nz+1}^{n+1}\right]}{2} \tag{26}$$

Using (23) and (26) in (25) gives

$$\begin{aligned}\left[V_{Nz+1}^{n+1}\right] = \Big(&[F]\,[G]\left[V_{Nz+1}^{n}\right] + 2\,[F]\,[A]\left[I_{Nz}^{n+1/2}\right] \\ &- [F]\,[A]\left(U + \frac{\alpha\,[J]\left[R'_{\text{lump}}\right][C_{\text{L}}]}{\Delta t}\right)\left[I_{Nz+1}^{n}\right]\Big)\end{aligned} \tag{27}$$

where

$$[F] = \left(U + \frac{[A]\,[J]\,[C_{\text{L}}]}{\Delta t} + \frac{\beta\,[A]\,[J]}{[R_{\text{L}}]}\right)^{-1} \tag{28}$$

$$[G] = \left(U + \frac{[A]\,[J]\,[C_{\text{L}}]}{\Delta t}\right) \tag{29}$$

The far-end boundary variables are solved using (22), (23) and (27).

Equations (11), (13), (19), (22) and (27) are used to evaluate voltage at any time instant and position along the interconnect. Similarly, (9), (14) and (23) are used to compute current. The voltage and current are evaluated alternatively in temporal and spatial domains. These variables are used for transient analysis and determination of the system performance.

### 3.2 Power Modeling for Interconnect System

The power dissipation in DIL model primarily consists of three components, viz. dynamic, static and short-circuit [4]. The DIL system along with these power dissipating components is shown in Fig. 5. The dynamic power dissipation ($P_{\text{dyn}}$) occurs because of charging and discharging of node capacitors. The generalized expression for $P_{\text{dyn}}$ at node $k$ is expressed as [9,18]

$$P_{\text{dyn}} = f C_k V_k^2 \tag{30}$$

where $f$ is frequency and defined as ($f = 1/T_{\text{p}}$) and $T_{\text{p}}$ is the time period of the signal. $C_k$ and $V_k$ represent node capacitance and voltage, respectively. The total average dynamic power dissipation at time instant $n$ is formulated as:

$$P_{\text{dyn}}^{n} = \left[(C_m + C_{\text{d}})\frac{\left(V_0^n\right)^2}{T_{\text{p}}} + (C_{\text{L}})\,\frac{\left(V_{Nz+2}^{n}\right)^2}{T_{\text{p}}} + \sum_{k=2}^{Nz+1}(C_k)\,\frac{\left(V_k^n\right)^2}{T_{\text{p}}}\right] \tag{31}$$

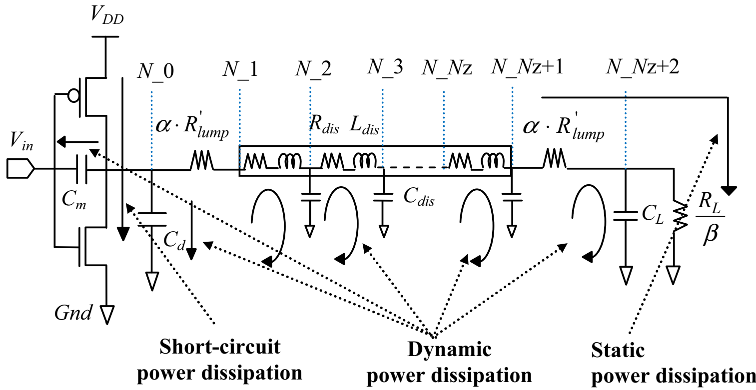


**Fig. 5** Power dissipation in DIL system

The static power dissipation ($P_{\text{stat}}$) is due to ohmic loss across interconnect parasitic resistance and load resistance $R_{\text{L}}$. The total $P_{\text{stat}}$ at time instant $n$ is defined as

$$P_{\text{stat}}^n = \frac{\beta\,(V_{\text{DD}})^2}{2\left[R_{\text{L}} + \beta \cdot Nz \cdot R_{\text{dis}} \cdot \Delta z + 2\beta \cdot \alpha \cdot R'_{\text{lump}} + \beta\left(\frac{V_{\text{DD}} - V_0^n}{I_p^n}\right)\right]} \tag{32}$$

Equation (32) is defined for the case when PMOS transistor of CMOS driver gate is in ON state. As $R_{\text{L}}$ approaches infinity, static power dissipation becomes zero.

Also, during transition period, both NMOS and PMOS transistors remain in ON state between the threshold voltages of NMOS and PMOS transistors. As a result, small current flows from $V_{\text{DD}}$ to ground for fraction of transition period duration which results in short-circuit power dissipation ($P_{\text{sc}}$) in the circuit. $P_{\text{sc}}$ can be defined as fraction ($x$) of total dynamic power dissipation [4,14]. It is given as

$$P_{\text{sc}}^n = x \cdot P_{\text{dyn}}^n \tag{33}$$

where $x$ ranges from 0.1 to 0.2.

## 4 Results and Discussion

In this section, performance of copper and MWCNT interconnects using VMS and CMS schemes is analyzed. The metrics used for performance analyses are propagation delay, energy and crosstalk. The analyses are carried out at 32 nm technology node. The interconnect dimensions are computed as per ITRS and CNIA [6,15]. $R_{\text{dis}}$, $C_{\text{dis}}$, $L_{\text{dis}}$ and $R'_{\text{lump}}$ for MWCNT interconnect are 0.95 M Ω/m, 9.41 pF/m, 9.48 µH/m and 79.04 Ω, respectively. The per unit length parameters $R_{\text{dis}}$, $C_{\text{dis}}$ and $L_{\text{dis}}$ for copper interconnect are 3.18 M Ω/m, 21.8 pF/m and 1.48 µH/m, respectively. $R'_{\text{lump}}$ is zero in case of copper interconnect. The load impedances, $R_{\text{L}}$ and $C_{\text{L}}$, are 1KΩ and 0.5 fF, respectively, for CMS scheme. $C_{\text{L}}$ is 1 fF for VMS scheme [1]. $R_{\text{L}}$ in case of VMS

scheme is very high and considered as infinity [1,4,12,37]. Gate length of transistors is 32 nm. Widths of NMOS and PMOS transistors considered are 1 and 2.5 μm, respectively [1,18]. For formulation using FDTD, $\Delta z$ for MWCNT and copper are 0.34 and 0.55 mm, respectively. $\Delta t$ is nearly same for both the interconnects and equals to 3.14 ns. The proposed FDTD-based model is validated using Tanner EDA tool, SPICE simulations [35]. The BSIM SPICE level 54 model is considered and taken from predictive technology model (PTM) [30].

### 4.1 Analysis of Copper and MWCNT Interconnects Using CMS Scheme

A comparative analysis is carried out for copper and MWCNT interconnects using CMS scheme and illustrated in Figs. 6 and 7. Propagation delay and power dissipation variation with interconnect lengths are shown in Fig. 6. It is observed from the figure that CMS MWCNT interconnect results in lower propagation delay in the circuit while CMS copper interconnect possesses lesser power dissipation. Hence, there is a trade-off in the performance parameters for CMS copper and MWCNT interconnects. The efficacy between the two has been inferred by analyzing the power_delay_product (PDP). PDP represents the energy consumption in the circuit and is an important figure-of-merit in e-circuits. PDP should be low for high performance applications. The PDP for CMS copper and MWCNT interconnects using proposed model based on FDTD, and SPICE is presented in Fig. 7. It is seen from the figure that PDP is nearly identical in both the cases for interconnect length of 500 μm. However, as the wire length increases, CMS MWCNT interconnect has significantly lesser PDP (nearly 64% lesser) as compared to CMS copper interconnect. Also, from Figs. 6 and 7, it is analyzed that results of the proposed model based on FDTD technique are in close agreement with SPICE results. The maximum error between these is $<3\%$.

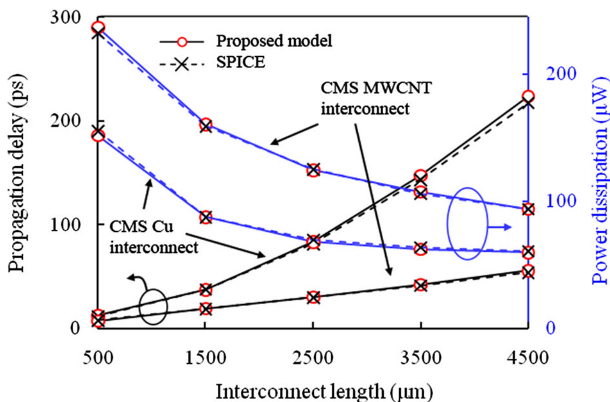


**Fig. 6** Propagation delay and power dissipation in copper and MWCNT interconnects using CMS scheme

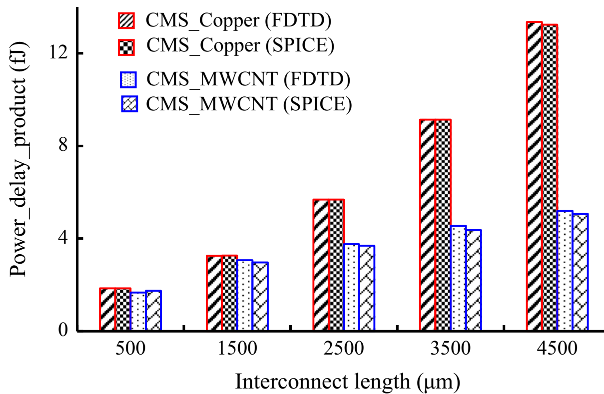


**Fig. 7** Power_delay_product in copper and MWCNT interconnects using CMS scheme

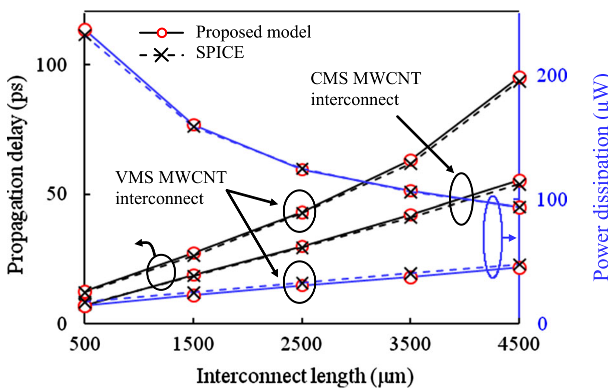


**Fig. 8** Propagation delay and power dissipation in MWCNT interconnect using VMS and CMS schemes

### 4.2 Analysis of MWCNT Interconnect Using VMS and CMS Schemes

Propagation delay and power dissipation are analyzed in MWCNT interconnect for both VMS and CMS schemes. Lower latency and thus higher speed are observed in case of CMS scheme [2, 40]. This is evident from Fig. 8. It is observed from the figure that at interconnect length of 4500 µm, MWCNT interconnect with CMS scheme has about 72% lesser propagation delay as compared to VMS scheme. Owing to smaller impedance termination, voltage swing over interconnects is reduced in CMS scheme. This causes fast charging and discharging of interconnect node capacitances. It is observed from the figure that power dissipation in case of CMS scheme is higher than VMS scheme. Thus, VMS scheme is better for power centric designs. Also, it is seen that the proposed model and SPICE results match closely with each other. The average percentage error between SPICE and analytical models for VMS and CMS schemes is 2.37 and 2.84%, respectively.

### 4.3 Analysis of CMS MWCNT Interconnect Using Resistive Driver and the Proposed CMOS Gate Driver Models

The driver-interconnect-load model in CMS scheme is shown in Fig. 9a. The driver models using CMOS gate and resistive element are represented in Fig. 9b, c, respectively. In resistive driver model, CMOS gate is approximated as resistive ($R_\mathrm{d}$) and capacitive ($C_\mathrm{d}$) elements [19,22,23,31,36]. Resistive driver model has limited accuracy as the nonlinear characteristics of MOS transistors cannot be modeled by lumped resistive and capacitive elements in different operating regions of MOS transistor. The output voltage for CMS MWCNT interconnect using resistive and CMOS gate drivers is shown in Fig. 10. The input is a ramp signal with transition period of 5 ps. The input to resistive driver circuit is opposite to that of CMOS driver input since there is no inversion of input signal in the former case. %Error1 in the figure represents percentage error between CMOS gate driver model and SPICE results, while %Error2 gives percentage error between resistive driver model and SPICE results. It is seen from the figure that the resistive driver model leads to significantly less accurate results. This is palpable from the figure, as average error in case of CMOS driver (%Error1) and

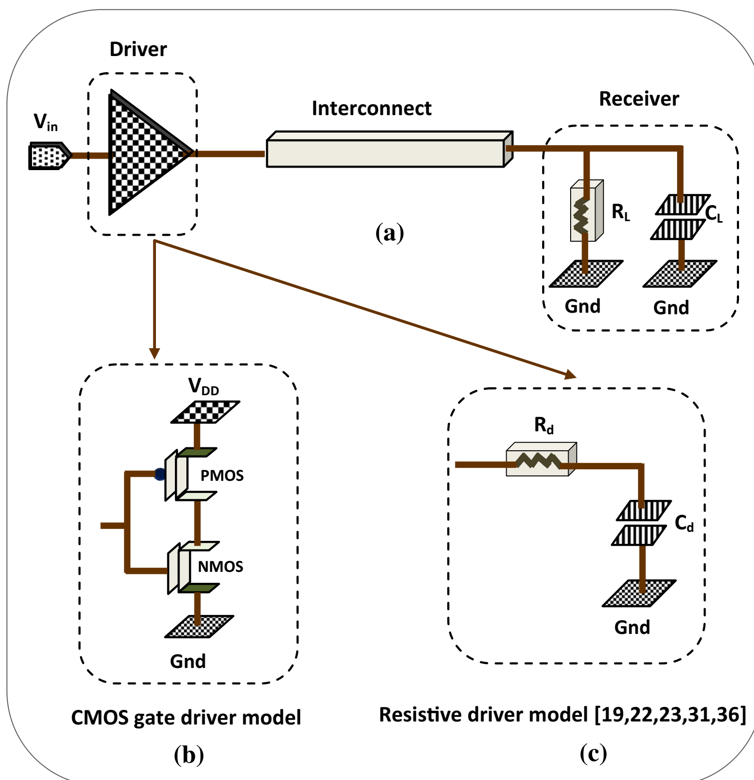


**Fig. 9** **a** Driver-interconnect-load model in CMS scheme. Realization of driver using **b** accurate CMOS gate model **c** approximate resistive model

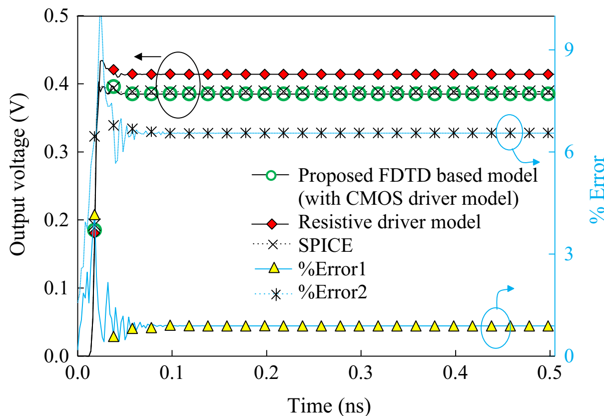


**Fig. 10** Output voltage in MWCNT interconnect using CMS scheme

resistive driver models (%Error2) are 0.94 and 6.49%, respectively. The lower value of %Error1 shows the higher accuracy and efficacy of CMOS gate driver model used in the present work over resistive driver model.

### 4.4 Crosstalk Analysis of MWCNT Interconnect Using CMS Scheme

Coupling between interconnects causes various non-ideal and signal integrity issues such as spurious noise production and enhanced circuit propagation delay. This is termed as crosstalk [13,23]. Crosstalk can be broadly categorized as functional and dynamic [11,19]. In functional crosstalk, input signal to the victim line is quiet. As a result, victim line experiences undershoot or overshoot noise whenever signal on the aggressor line switches, whereas in dynamic crosstalk, input signals to the aggressor and victim lines switch simultaneously either in-phase or out-of-phase with each other. This causes propagation delay and noise in the circuit [1]. Table 1 shows the crosstalk-induced propagation delay in 2-Line coupled MWCNT interconnects using CMS scheme for both in-phase and out-of-phase switching cases. From the table, it is observed that crosstalk-induced delay is lesser for in-phase switching case as compared to out-of-phase switching case. The higher propagation delay in out-of-phase is because of higher Miller capacitance effect [1]. A comparison is also made in between the proposed model using CMOS driver model, resistive driver model and SPICE. It is analyzed that CMOS driver model estimates propagation delay more accurately to SPICE results. The average percentage error between resistive driver model and SPICE for in-phase and out-of-phase cases is 8.54 and 9.52%, respectively. Furthermore, these error values for CMOS driver model and SPICE are 1.25 and 1.78%, respectively.

The transient responses at the victim line (Line 3) for three different cases in 5-Line coupled MWCNT interconnects using CMS scheme are presented in Fig. 11. Figure 11a, b shows that peak overshoot and peak undershoot obtained by the proposed model are 0.47 and 0.08 V, respectively, at 0.05 ns. Figure 11c shows the crosstalk-

**Table 1** Crosstalk-induced propagation delay in coupled MWCNT interconnects using CMS scheme

| Interconnect length (μm) | 2-Line coupled crosstalk-induced propagation delay (ps) | | | | | |
|---|---|---|---|---|---|---|
| | In-phase switching | | | Out-of-phase switching | | |
| | SPICE | Resistive driver model | CMOS driver model (proposed) | SPICE | Resistive driver model | CMOS driver model (proposed) |
| 500 | 10.26 | 9.18 | 10.39 | 22.48 | 19.83 | 23.14 |
| 1500 | 20.70 | 18.83 | 20.39 | 63.77 | 57.12 | 64.72 |
| 2500 | 32.08 | 29.59 | 32.28 | 128.48 | 117.72 | 130.9 |
| 3500 | 44.19 | 41.36 | 43.35 | 213.32 | 198.03 | 216.2 |
| 4500 | 57.36 | 54.24 | 56.77 | 317.88 | 300.33 | 322.6 |
| Avg. % error between model and SPICE results | | 8.54% | 1.25% | | 9.52% | 1.78% |

induced delay of 22.34 ps. For all the three cases, it is observed that the CMOS driver model using the proposed model based on FDTD technique and SPICE results are in very close agreement with each other.

In the present work, carbon nanotube is considered as uniform wire. However, in practical configurations, it is likely that carbon nanotube may not line up perfectly and may possess bends or non-uniformities. The non-uniform copper interconnects have been modeled and analyzed using perturbation technique, virtual straight lines and modeling interconnect parasitics as line-dependent parameters in [8,17,34]. These techniques shall be further explored and implemented for carbon nanotubes as future work of the authors.

## 5 Conclusion

The paper analyzes performance of CMS MWCNT interconnect using FDTD technique. The proposed FDTD-based model can be used for signal integrity analysis of both copper and MWCNT interconnects as well as VMS and CMS schemes. The driver is modeled by CMOS gate and characterized by $n$th power law model. The interconnects are represented by equivalent ESC model. It is analyzed that using CMS scheme, MWCNT interconnect has an upper edge over the conventional copper interconnects in terms of lower propagation delay and lesser PDP. Also, with reference to traditional VMS scheme, CMS scheme is investigated to be better particularly for high speed applications owing to lesser propagation delay in the circuit. Further, it is validated that CMOS driver model using the proposed model has higher precision than the resistive driver model. The crosstalk is analyzed for 2-Line and 5-Line coupled MWCNT interconnects using CMS scheme. For all the cases considered, FDTD technique-based analytical model and SPICE-based simulation results match closely. The proposed model accurately predicts the system response and can be used for

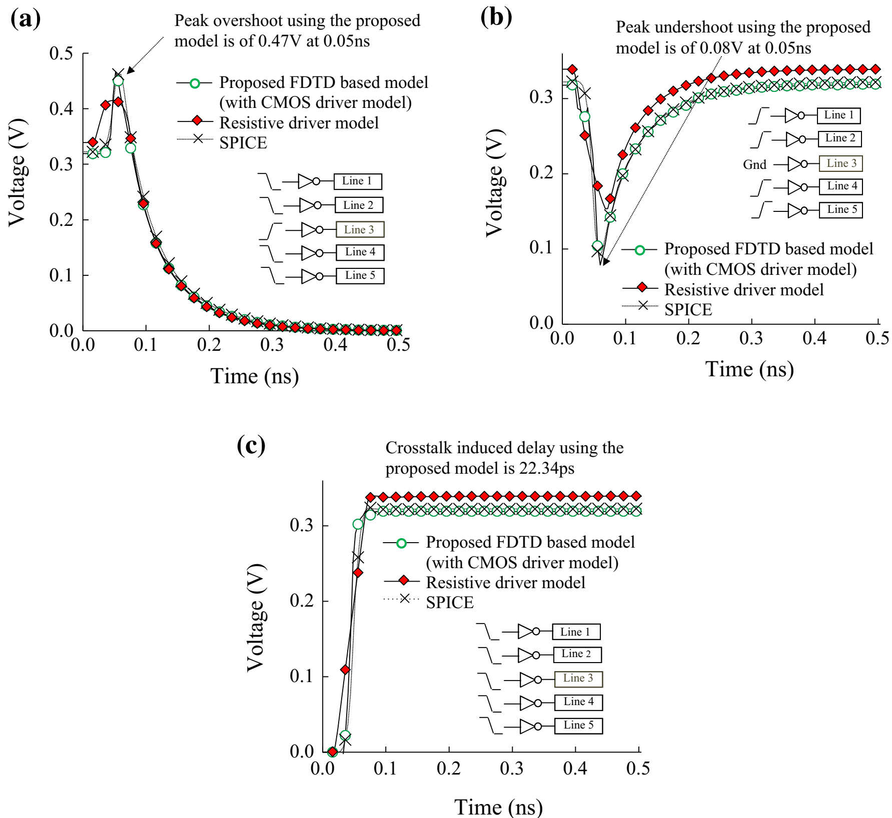


**Fig. 11** Transient response at the victim line (Line 3) in 5-Line CMS MWCNT interconnect for three different switching cases. **a** Dynamic crosstalk (out-of-phase switching case). **b** Functional crosstalk. **c** Dynamic crosstalk (in-phase switching case)

signal integrity analyses of $M$-Line uniform coupled interconnects. The non-uniform MWCNT interconnects can be modeled by incorporating specialized modeling techniques and can be further explored. Subsequently, from the present research work, it is inferred that MWCNT interconnects using CMS scheme are better solution to achieve high performance and efficiency in integrated circuits at nanoscale regime.

## Appendix 1

The parasitic elements of MWCNT interconnect can be defined as:

The lumped resistance ($R_{\text{lump}}$) comprises of quantum resistance ($R_{\text{q}}$) which is due to quantum confinement of carriers along the interconnect dimensions. The contact resistance ($R_{\text{c}}$) is due to imperfect contact between the interconnect and substrate. $R_{\text{c}}$ depends on the fabrication process and varies from 1 to 20 KΩ [10]. $R_{\text{lump}}$ is expressed as [19]

$$R_{\text{lump}} = \left[ \sum_{i=1}^{N} \left( \frac{h}{2e^2 \cdot N_{\text{ch}}^i} + R_{\text{c}}^i \right)^{-1} \right]^{-1} \tag{34}$$

where $h$ is Planck's constant and $e$ represents charge on electron.

$R_{\text{lump}}$ is distributed equally along the two ends of the interconnect as $R'_{\text{lump}}$. It is presented as

$$R'_{\text{lump}} = \frac{R_{\text{lump}}}{2} \tag{35}$$

The distributed resistance ($R_{\text{dis}}$) in the ESC model represents the scattering resistance per unit length (p.u.l.) [22]. It is primarily due to optical and acoustic phonon scattering. $R_{\text{dis}}$ is predominant when interconnect length is greater than electron mean free path [28]. It is defined as [23]

$$R_{\text{dis}} = \sum_{i=1}^{N} \left( \frac{h}{2e^2 \cdot N_{\text{ch}}^i \cdot \lambda_i} \right) \tag{36}$$

where $\lambda_i$ corresponds to effective electron mean free path of $i$th shell and is obtained as [24]

$$\lambda_i = \frac{10^3 d_i}{(T/T_0) - 2} \tag{37}$$

where $T_0$=100 K

The distributed inductance ($L_{\text{dis}}$) comprises of kinetic inductance p.u.l. ($L_{\text{k}}$) and magnetic inductance p.u.l. ($L_{\text{m}}$).

The kinetic inductance p.u.l. per channel ($L_{\text{k/channel}}$) is given as [19]

$$L_{\text{k/channel}} = \left( \frac{h}{2e^2 v_{\text{f}}} \right) \left( \frac{1}{2} \right) \tag{38}$$

where $v_{\text{f}}$ is Fermi velocity.

Using $L_{\text{k/channel}}$, kinetic inductance p.u.l. per shell ($L_{\text{k/shell}}$) is computed.

$$L_{\text{k/shell}}^i = \left( \frac{L_{\text{k/channel}}}{N_{\text{ch}}^i} \right); \quad 1 \le i \le N \tag{39}$$

The p.u.l. mutual shell to shell inductance ($L_{\text{m_shell_shell}}$) is defined as [23]

$$L_{\text{m_shell_shell}}^{i,i+1} = \frac{\mu}{2\pi} \ln \left( \frac{d_{i+1}}{d_i} \right); \quad 1 \le i \le N - 1 \tag{40}$$

The equivalent kinetic inductance p.u.l. of $i$th shell ($L^{i}_{\mathrm{equ}}$) is obtained using recursive expression as [23]

$$L^{i}_{\mathrm{equ}} = \left[ \frac{1}{L^{i-1}_{\mathrm{equ}} + L^{i-1,i}_{\mathrm{m_shell_shell}}} + \frac{1}{L^{i}_{\mathrm{k/shell}}} \right]^{-1}; \quad 2 \le i \le N \tag{41}$$

where

$$L^{1}_{\mathrm{equ}} = L^{1}_{\mathrm{k/shell}} \tag{42}$$

The equivalent kinetic inductance p.u.l. of MWCNT interconnects ($L_{\mathrm{k}}$) is given by:

$$L_{\mathrm{k}} = L^{N}_{\mathrm{equ}} \tag{43}$$

The equivalent magnetic inductance p.u.l. of MWCNT interconnect ($L_{\mathrm{m}}$) is computed as [24].

$$L_{\mathrm{m}} = \frac{\mu}{2\pi} \cosh^{-1}\left(\frac{d_N + 2h_{\mathrm{g}}}{d_N}\right) \tag{44}$$

where $d_N$ is the outermost shell diameter of MWCNT and $h_{\mathrm{g}}$ represents the distance between MWCNT and ground plane.

The equivalent inductance in the ESC model ($L_{\mathrm{dis}}$) is computed as

$$L_{\mathrm{dis}} = L_{\mathrm{k}} + L_{\mathrm{m}} \tag{45}$$

Similarly, distributed capacitance ($C_{\mathrm{dis}}$) of MWCNT in the ESC model is obtained. It comprises of p.u.l. quantum capacitance ($C_{\mathrm{q}}$), and electrostatic capacitance ($C_{\mathrm{e}}$). $C_{\mathrm{dis}}$ is expressed as

$$C_{\mathrm{dis}} = \frac{C_{\mathrm{q}} \cdot C_{\mathrm{e}}}{C_{\mathrm{q}} + C_{\mathrm{e}}} \tag{46}$$

$C_{\mathrm{e}}$ is obtained as [24]

$$C_{\mathrm{e}} = \frac{2\pi\varepsilon}{\cosh^{-1}\left(\frac{d_N + h_{\mathrm{g}}}{d_N}\right)} \tag{47}$$

$C_{\mathrm{q}}$ is obtained by solving recursive formulae given below [23]

$$C^{i}_{\mathrm{equ}} = \left[ \frac{1}{C^{i-1}_{\mathrm{equ}}} + \frac{1}{C^{i-1,i}_{\mathrm{c_shell_shell}}} \right]^{-1} + C^{i}_{\mathrm{q/shell}}; \quad 2 \le i \le N \tag{48}$$

$$C^{1}_{\mathrm{equ}} = C^{1}_{\mathrm{q/shell}} \tag{49}$$

$$C_{\text{q}} = C_{\text{equ}}^{N} \tag{50}$$

where $C_{\text{equ}}^{i}$is the equivalent capacitance of $i$th shell. $C_{\text{q/shell}}$ and $C_{\text{c_shell_shell}}$ are p.u.l. quantum capacitance per shell and coupling capacitance between shells of MWNCT interconnect, respectively [11]. These are defined as [19]

$$C_{\text{q/shell}}^{i} = 2N_{\text{ch}}^{i}\left(\frac{2e^2}{hv_{\text{f}}}\right); \quad 1 \le i \le N \tag{51}$$

$$C_{\text{c_shell_shell}}^{i,i+1} = \frac{2\pi\varepsilon}{\ln\left(d_{i+1}/d_i\right)}; \quad 1 \le i \le N-1 \tag{52}$$

The p.u.l. mutual inductance ($M_{\text{i}}$) and coupling capacitance ($C_{\text{c}}$) between two parallel MWCNT interconnects are given as [11,21,24,31]

$$M_{\text{i}} = \frac{\mu}{2\pi}\left[\ln\left(\frac{l}{h_{\text{c}}} + \sqrt{1 + \left(\frac{l}{h_{\text{c}}}\right)^2}\right) - \sqrt{1 + \left(\frac{h_{\text{c}}}{l}\right)^2} + \frac{h_{\text{c}}}{l}\right] \tag{53}$$

$$C_{\text{c}} = \frac{\pi\varepsilon}{\ln\left(\frac{s_p}{d_N} + \sqrt{\left(\frac{s_p}{d_N}\right)^2 + 1}\right)} \tag{54}$$

where $l$ is the length of interconnect and $s_p$ is the separation between two interconnects. $h_{\text{c}}$ is the center-to-center distance between two interconnects and equals to $(s_p + d_N)$.

## Appendix 2

The parasitic elements for copper interconnects can be defined as [30,39]:

$$R_{\text{dis}} = \frac{\rho}{w \cdot t} \tag{55}$$

$$L_{\text{dis}} = \frac{\mu}{2\pi}\left[\ln\left(\frac{2l}{w+t}\right) + \frac{1}{2} + \frac{0.22\,(w+t)}{l}\right] \tag{56}$$

$$C_{\text{dis}} = \varepsilon\left[\begin{array}{l}\frac{w}{h_{\text{g}}} + 2.22\left(\frac{s_p}{s_p+0.7h_{\text{g}}}\right)^{3.19} \\ +1.17\left(\frac{s_p}{s_p+1.51h_{\text{g}}}\right)^{0.76} \cdot \left(\frac{t}{t+4.53h_{\text{g}}}\right)^{0.12}\end{array}\right] \tag{57}$$

$$M_{\text{i}} = \frac{\mu}{2\pi}\left[\ln\left(\frac{2l}{h_{\text{c}}}\right) - 1 + \frac{h_{\text{c}}}{l}\right] \tag{58}$$

$$C_{\text{c}} = \varepsilon\left[\begin{array}{l}1.14\left(\frac{t}{s_p}\right)\left(\frac{h_{\text{g}}}{h_{\text{g}}+2.06s_p}\right)^{0.09} + 0.74\left(\frac{w}{w+1.59s_p}\right)^{1.14} \\ +1.16\left(\frac{w}{w+1.87s_p}\right)^{0.16} \cdot \left(\frac{h_{\text{g}}}{h_{\text{g}}+0.98s_p}\right)^{1.18}\end{array}\right] \tag{59}$$

where $\rho$ is resistivity of copper material. $w$ and $t$ are width and thickness of the copper interconnect. All other parameters for copper interconnects in (55)–(59) have their

usual meaning as that for MWCNT interconnect. $R'_{\text{lump}}$in the ESC model for copper interconnect is zero.

## Appendix 3

The Telegraph's equations are given as [29]:

$$\frac{\partial [V]}{\partial z} + [L]\frac{\partial [I]}{\partial t} + [R][I] = 0 \tag{60}$$

$$\frac{\partial [I]}{\partial z} + [C]\frac{\partial [V]}{\partial t} = 0 \tag{61}$$

where $[V]$ and $[I]$ are $M \times 1$ voltage and current variables along interconnect and are function of position and time. $[R]$, $[L]$ and $[C]$ are $M \times M$ dimensional p.u.l. interconnect parasitics. These are given as

$$[R] = \text{diag}\left(R^1_{\text{dis}}, R^2_{\text{dis}}, \cdots, R^M_{\text{dis}}\right),$$

$$[L] = \begin{pmatrix} L^1_{\text{dis}} & M_{\text{i}}^{1,2} & M_{\text{i}}^{1,3} & \ldots & M_{\text{i}}^{1,M} \\ M_{\text{i}}^{2,1} & L^2_{\text{dis}} & M_{\text{i}}^{2,3} & \cdots & M_{\text{i}}^{2,M} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ M_{\text{i}}^{M,1} & M_{\text{i}}^{M,2} & M_{\text{i}}^{M,3} & \cdots & L^M_{\text{dis}} \end{pmatrix} \text{ and}$$

$$[C] = \begin{pmatrix} C^1_{\text{dis}} + \sum\limits_{j=2}^{M} C_{\text{c}}^{1,j} & -C_{\text{c}}^{1,2} & -C_{\text{c}}^{1,3} & \ldots & -C_{\text{c}}^{1,M} \\ -C_{\text{c}}^{2,1} & C^2_{\text{dis}} + \sum_{j=1,3}^{M} C_{\text{c}}^{2,j} & -C_{\text{c}}^{2,3} & \cdots & -C_{\text{c}}^{2,M} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ -C_{\text{c}}^{M,1} & -C_{\text{c}}^{M,2} & -C_{\text{c}}^{M,3} & \ldots & C^M_{\text{dis}} + \sum\limits_{j=1}^{M-1} C_{\text{c}}^{M,j} \end{pmatrix} \tag{62}$$

where $R_{\text{dis}}$, $L_{\text{dis}}$ and $C_{\text{dis}}$ are distributed resistance, inductance and capacitance, respectively, of MWCNT/copper interconnect in ESC model. $M_{\text{i}}$ and $C_{\text{c}}$ represent p.u.l. mutual inductance and coupling capacitance between two parallel MWCNT/copper interconnects.

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