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New Protection Technique Against Unidirectional MEUs for FIR Filters

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Abstract As technology shrinks, multiple bits upsets (MBUs) are becoming an important problem in the reliability of digital designs exposed to radiation effects. In this paper, a new technique for the implementation of finite impulse response (FIR) filters is presented that provides protection against single and multi-unidirectional bit upsets (SEUs and MBUs), which have a lower circuit complexity and cost than traditional techniques like N-modular redundancy. Most of previous works has focused on single event upset (SEU), however, in this paper, a coding method based on Berger codes are presented and implemented on FPGA-based FIR filter. As the Berger coding covers all unidirectional faults, the MBUs are also handled in the proposed schemes. The effectiveness of the proposed technique has been evaluated using a dynamic partial reconfiguration-based fault injection platform. The implementation results of the proposed mitigation technique in comparison with traditional TMR method and previous mitigation techniques in the literature represent the effectiveness in terms of protection and implementation cost.

Keywords FIR filter · Berger code checker · Fault · Unidirectional MEUs · Reliability

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1 Introduction

Filters are widely used in digital communication systems for noise canceling, channel equalization, signal separation and etc. Nowadays, the digital communication systems are the essential of all space missions, and therefore, digital filters play an important role in space systems [7]. All in outer space systems are faced with a harsh environment and are exposed to ionizing radiations that cause unwanted effects in microelectronics. Soft error, as most prominent effect, is a major concern for all digital circuit. Furthermore, the shrinking of technology exacerbates the failure probability of space systems. As technology shrinks, the probabilities of multiple bit errors are increased, as MBUs constitute over 50% of the upsets in recent technologies [14].

Unfortunately packing and shielding are ineffective in the presence of SEUs and MBUs since the high energetic particles easily are able to penetrate through the shield packages [15]. In the past decade, various SEU mitigation techniques to detect, mask, or modify the fault effect for FPGAs have been proposed. According to the design, the designers have utilized a type of redundancy in data layer, software layer, hardware layer, and over the time.

In order to mitigate the unwanted effects of soft errors and provide a reliable digital communication system, several design techniques are introduced for filters such as using Hamming codes, parity-based checksum, and reduced precision modular redundancy. In studies, the level of protection is range from detection of erroneous behavior to correction of faulty outputs.

A review of the literature on this topic shows that many of these protection mechanisms rely on redundancy approaches in the normal filter operation which impose a significant area overhead and increase delay time. A key problem with much of the literature regarding to reliable digital systems is the unwanted overhead costs. So, the aforementioned works attempt to introduce novel fault tolerant structures with lower overhead and more fault coverage capability. In addition, in literature, the straightforward Triple Modular Redundancy (TMR), in which three identical circuits with a voter are used to compute the specified function, has commonly employed as a benchmark for comparison. The overhead of the proposed schemes is compared to that of TMR.

In this paper, we aim to propose a new approach to detect unidirectional MEU fault in low pass FIR filter. Unidirectional errors are referred the faulty states that only flip ones into zeroes or only zeroes into ones, such as in asymmetric channels. We have developed a novel fault tolerant architecture for FIR filters based on all unidirectional error detecting (AUED) code. We specially have applied the Berger code encoder and checker in the conventional FIR structure. At first, we have considered the basics idea of applying AUED code in filters structure through the conventional encoder and checkers. With an approximate estimation, we infer that the overhead of conventional structures is unacceptable. Therefore, we have introduced an integrated form for the coder and decoder circuits. The introduced circuit, with a same functionality, provides much lower complexity and area overhead.

The previous studies have tended to focus on single faults rather than MBU faults, while MBUs are increasingly becoming a vital factor by technology shrinking. Few researchers have addressed the problem of MBUs in FIR filters. Furthermore, due

to the fact that the conventional circuits for Berger code encoder and decoder, as a AUED code, impose an unacceptable area overhead, this approach has been neglected. However, in this paper, we have described an interesting solution to mitigate unidirectional MBU faults if FIR filters.

The rest of this paper is organized as follows. In next section, the related works in fault tolerant filters are reviewed. We have presented background information and considered the basics idea of applying AUED code over FIR filters in Sect. 3. In Sect. 4, we focus on the merging of encoders and decoders in a specific circuit. Results and discussions are provided in Sect. 5. Finally, the conclusions of this paper are summarized in Sect. 6.

2 Related Works

There is a considerable amount of literature on the soft error mitigation techniques for modern microcircuits in the radiation environment. Some of them are allocated to FIR filters, and innovative methods are considered to provide protection capability for filters.

As stated in Ref. [12] Triple Modular Redundancy (TMR) and Hamming Codes are the quite straightforward and successful methods for fault mitigation in digital filters. In TMR method, the design is triplicated and voting logic is added to mask errors. To protect FIR filters using Hamming codes an encoder and decoder have been added before and after each register in filter structure. Through the combining of the decoders, the shared decoder method as an enhanced implementation of fault tolerant filter based on Hamming codes have been investigated in Ref. [12].

Ref. [20] by adding a parity bit to each coefficients of adaptive digital filter speeds up the adaptation step (fast adaptation) in faulty condition. It is necessary to mention that adaptive filters by nature recover from soft errors on their coefficients, but an acceptable recovery time is critical for many applications. The proposed method in this research is depended on the operation condition which is generically described as "using the knowledge of the system."

Also, the transform-domain fault tolerant adaptive filters have been proposed [18]. Another system knowledge approach has been applied to simple filter structures [23], in which one special type of FIR filter, the moving average filter, is analyzed. This filter fulfills with a shift operation and the filter needs only adders. For low and average protection requirements, just by a counter or decimated filter error detection capability has been achieved. However, for high protection cases, a two-dimensional parity method is proposed. According to this method, for each input value a 'vertical' parity and for each bit position on the input value a 'vertical' parity is computed. for normal condition, the actual and accumulated parity values are the same, however, in the presence of single faults we face with a discrepancy which provide fault detection capability. Moreover, the partial TMR has been applied over the stored values to correct the error. Also, the FIR protection using system knowledge has been compared with other soft error mitigation techniques like TMR and Hamming codes [22].

A structural dual modular redundancy (DMR), which uses two different implementations of the basic filter operating in parallel, has been proposed in Ref. [21]. Through the distinct error patterns at the filter output the faulty module is detected and error-free result is selected.

Algorithmic soft error-tolerance (ASET) technique [3] that employs uncomplicated estimator of a main DSP unit, M block, has been investigated on for frequency selective finite impulse response (FIR) filtering. This work is extended based on algorithmic noise tolerance (ANT) [2] in which a low-complexity unit, the estimator, computes an approximation for M block output. The Euclidean metric of the main and estimator and also the Hamming distance between two estimator units provide error detection capability.

The use of redundant residue number systems (RNSs) is another technique that has been explored for FIR filter protection [5,17,25]. Based on residue code method, the operands are divided by a given number and the computation is applied on reminders. The residue code has the same arithmetical and logical properties of operand; therefore, a low-complexity computation is exploited for the fault detection purposes. In some cases, to provide error masking capability, a redundant unit has been added in proposed structure [17].

General digital filters that are very similar with convolutional code structure have been adopted to protect from errors in Ref. [26], the parity check positions have been added in the code and a parallel parity channel is developed besides the original structure. Zhen Gao and co-workers [8,9] have developed on a new method to protect parallel filters. Their approach is based on applying ECCs, especially Hamming codes, to the parallel filters outputs. For future works, they also recommend the use of more powerful multibit ECCs, such as Bose–Chaudhuri–Hocquenghem codes, to correct errors on MBUs in filters.

Here we have proposed a new hardening technique for FIR filters to protect against unidirectional MBUs based on the Berger Codes. Through the proposed an efficient scheme for data encoding and decoding, the area, power consumption, and error rate is significantly being reduced. The Berger code is the least redundant separable unidirectional error detecting code that provides an ability to detect all unidirectional errors in the telecommunication channels and arithmetic operations [1].

A unidirectional error is a multiple bit upset so that all errors have same type either $0 \rightarrow 1$ or $1 \rightarrow 0$. According to the Berger code, the binary representation of the number of 0's or 1's in the information part are utilized as the check part. For a data vector with the width of n, the Berger code requires $K = \lceil \log_2(n+1) \rceil$ check bits $C = (c_{K-1}, \ldots, c_1, c_0)$. Berger check prediction (BCP) was used to handle arithmetic and logic operations [13]. In addition, some design methods of Berger code checkers were proposed in the literature [11,19]. In the complicated cases that the Berger codes in the filter structure are intended to a multi-variable issue, for the estimation of faulty state aims, the state space model as illustrated in Ref. [10] can be applied. We aim to develop this coding methods over the communication digital signal processing units, especially FIR filters.

3 Proposed Scheme

A FIR filter equation is described by the following operation [16]:

$$y[n] = \sum_{i=0}^{N} h[i] \cdot x[n-i]$$

where $x[n]$ is the input signal, $y[n]$ is the output and $h[n]$ is the impulse response of the filter. A common structure, the direct form, of n-tap FIR filter is illustrated in Fig. 1, where the input vector $x[n]$ are shifted though the delay registers (D-element), at the same time, the corresponding coefficients $h[n]$ are multiplied in the content of taps and finally the sum of these products yields the filter output $y[n]$. Because the implementation cost of multiplication operation is so large, in some cases a single processing element (PE), multiplier-accumulator was multiplexed among all of the filter taps [4]. As illustrated in Fig. 2 [24], the hardware complexity of this scheme is lower, and therefore the fault detection methods are feasible to be applied, however, the long execution time is a severe drawback.

The new proposed technique is based on the use of Berger code as an effective error detection mechanism. A Berger code version of the FIR filter is obtained by using the Berger code prediction (BCP) units along the basic FIR filters element. The predicted number of 1's in the output of this filter by $N_y[n]$ is equal to the number of 1's of the original filter. So, through a comparator the faulty state is detected. As illustrated in Figs. 3 and 4, besides the main adders and multipliers, we have placed the Adder

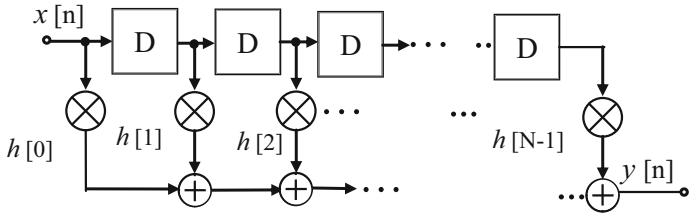

Fig. 1 Direct form FIR digital filter structures (parallel)

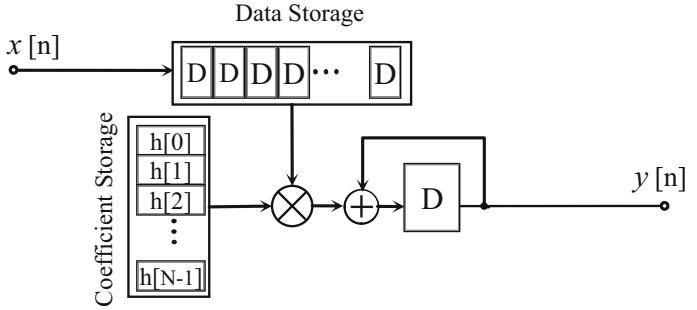

Fig. 2 A single PE architecture for direct form FIR filter structure

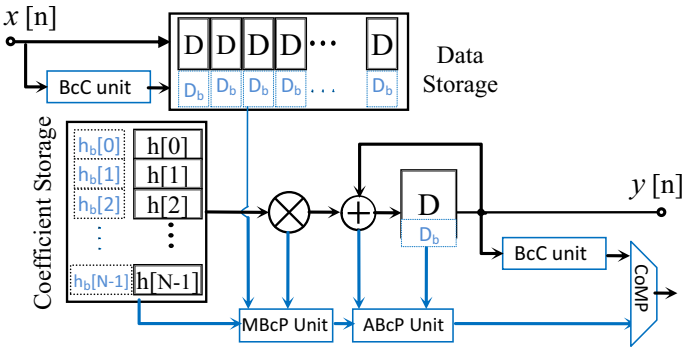

Fig. 3 Proposed coding scheme for single PE FIR filter

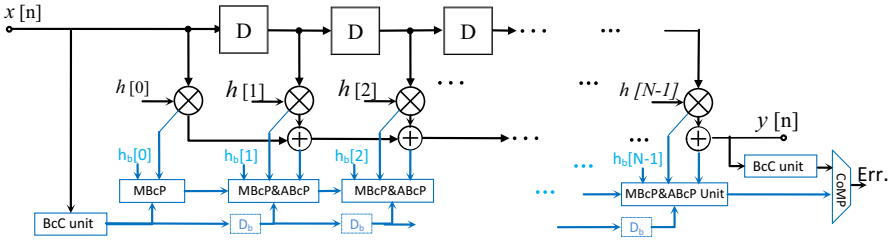

Fig. 4 Proposed coding scheme in general for direct form FIR digital filter

and Multiplier Berger Code Predictor (ABCP) and (MBCP) units. These units, which are detailed in following, predict the Berger check bits of results. To perform this requirement, the number of 1's in the input patters as preliminaries are needed. So, the Berger Code Counter (BCC) unit that calculates the number of 1's has been provided in the proposed scheme. Moreover, the delay element is used over input checker bits to provide the number of 1's for other filter taps. Also, the check bits of the impulse response $h[n]$ have been stored as another input of BCP units. In following subsection, we have detailed the developed Berger check prediction units in the FIR filters.

3.1 BCC Unit

The Berger code counter or encoder unit calculates the sum all the ones in the input time-series $x[n]$. According to Berger code theory, if the information word consists of n bits, $k = \log_2(n+1)$ bits are required as check bits. The check bits can be extracted with a primitive scheme represented in Fig. 5. In this design, the half and semi half adder (H.A and H^2A) units are used. The Semi half adder unit are the same as H.A, with the exception that the Carry bit is unrequited in H^2.A units. The logical details of these blocks are also illustrated in figure. According to this scheme, the number of H.A and H^2.A blocks for n-bit information is equal to Eq. (1). A multi-operand carry save adder (MCSA) similar to the one shown in Ref. [13] is also used here to perform the summation.

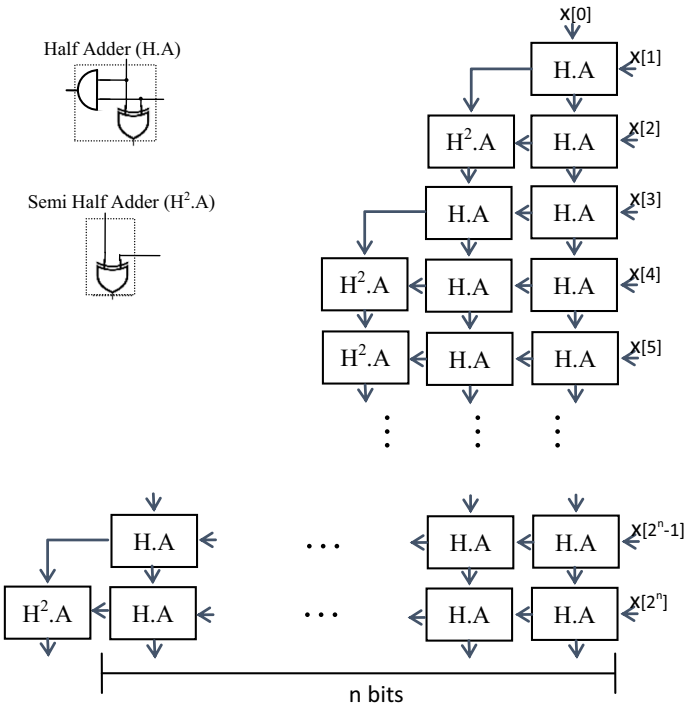

Fig. 5 A primitive scheme for Berger code counter

$$\sum_{i=0}^{m}\left(2^{i}.(i+1)\right)+(2^{m}-n)(k+1), \qquad m=\log_2\lfloor n\rfloor \tag{1}$$

3.2 Adders Berger Code Predictor (ABCP) Unit

The ABCP unit, based on the theorem that is detailed in the following, predicts the Berger check bits over adder results. Consider the addition of two n-bit numbers, $A[n]=(a_n,a_{n-1},\ldots,a_2,a_1)$ and $B[n]=(b_m,\ b_{m-1},\ldots,b_2,b_1)$ are the input patterns of an adder, also let $N[A]$ and $N[B]$ denote the number of 1's in the input patterns, respectively. The decimal representation for i-th bits in adder could be characterized as:

$$a_i+b_i+c_{i-1}=s_i+2c_i \tag{2}$$

s_i, c_i and c_{i-1} indicate the adder result and input/output carry bits for the i-th adder block, respectively. The bit counting over an input pattern is corresponding to adding up the bits in decimal format. So, we are able to develop following equation to find the Berger check bits.

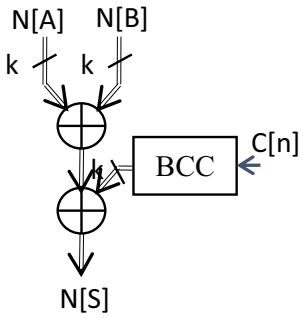

Fig. 6 A primitive scheme for ABCP unit

$$
\begin{aligned}
N[A]+N[B] &= \sum_n a_i + \sum_n b_i = \sum_n [a_i + b_i] \\
&= \sum_n \left[(a_i + b_i) + \overbrace{c_{i-1} - c_{i-1}}^{=0} \right] = \sum_n \left[(a_i + b_i + c_{i-1}) - c_{i-1} \right] \\
&= \sum_n \left[\overbrace{a_i + b_i + c_{i-1}}^{Eq.2} - c_{i-1} \right] = \sum_n \left[(2c_i + s_i) - c_{i-1} \right] \\
&= \sum_n \left[s_i + (2c_i - c_{i-1}) \right] = \sum_n s_i + \sum_n (2c_i - c_{i-1}) \\
&= N[S] + N[C] \qquad (3)
\end{aligned}
$$

In which, the number of 1's in an adder result, $N[S] = \{s_n, s_{n-1}, \ldots, s_2, s_1\}$, could be predicted based on the Berger check bits of the inputs and carry chain, while the input carry c_0 is equal to 0 for all adders and c_n is the output carry, we define the number of 1's in the carry chain as:

$$
\begin{aligned}
N[C] &= \sum_n (2c_i - c_{i-1}) = 2c_n + c_{n-1} + c_{n-2} + \cdots + c_2 + c_1 - c_0 \\
&= \{2c_n, c_{n-1}, c_{n-2}, \ldots, c_2, c_1\}.
\end{aligned}
$$

Figure 6 represents a primitive scheme to realize the adder Berger predictor unit. As illustrated in figure, this unit requires two k-bit adder/subtracter and moreover an BCC unit to compute Berger check bits for carry chain. Also, the adder/subtracter are reduced in order from n to $\log [n+1]$, however the area overhead of BCC unit causes that this scheme imperfect.

3.3 Multiplier Berger Code Predictor (MBCP) Unit

The multiplier architecture is constructed with adders, and therefore the aforementioned Berger checker scheme for adders can be developed over multiplier units

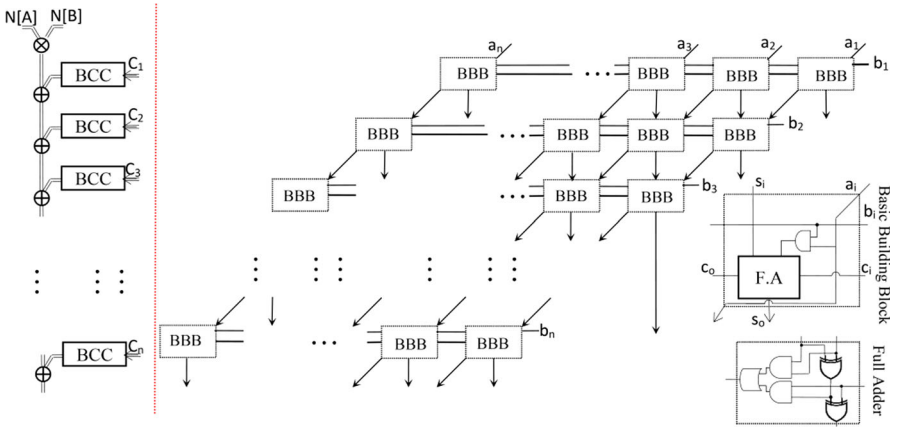

Fig. 7 Multiplier architecture (*right*) and a primitive scheme for MBCP unit

which are used in FIR filters. Multipliers involve computing a set of partial products, $\mathrm{PP}_i = A \times b_i$, and then summing the partial products together. The Berger check bit for partial products, $N[\mathrm{PP}]$, simply can be calculated as Eq. (4). This Equation also represents the summation of check bits of PPs.

$$N[\mathrm{PP}_i] = \begin{cases} 0 & \forall b_i = 0 \\ N[A] & \forall b_i = 1 \end{cases} \Rightarrow \sum_n N[\mathrm{PP}_i] = N[A] \times N[B] \tag{4}$$

Subsequently, the partial produces are added up to produce the final product result. Similarly, to previous subsection, the Berger check bit can be predicted for each stage based on the inputs and carry chain check bits. The check bits are added/subtracted to create the product result Berger bits. For $A[n]$ and $B[n]$, suppose the adder result and carry chain of the i-th stage are denoted by $S_i[n]$ and $C_i[n]$, respectively. The product result check bits, $N[P]$, can be summarized as Eq. (5).

$$\begin{aligned} N[S_i] &= N[\mathrm{PP}_{i-1}] + N[S_{i-1}] - N[C_i] \\ N[P] &= \sum_n N[C_i] + \sum_n N[\mathrm{PP}_i] = N[A] \times N[B] - \sum_n N[C_i] \end{aligned} \tag{5}$$

Similarly, to ABCP unit, the MBCP unit is constructed with size reduced k-bit adders. A primitive scheme to implement MBCP unit is illustrated in Fig. 7. In comparison with basic adders in multiplier architecture, the size of the Berger predictor adders is perfect. However, the overall area overhead which imposed by BCC units aggravates the outcome. In following section, to achieve a reasonable area overhead, we provide a specific method to eliminate primitive schemes of Berger checkers.

4 Integration of Berger Code Checkers

Although the proposed scheme is practical and effective for fault detect purposes, it is imperfect due to the fact that the BCC unit imposes an unacceptable area overhead. To

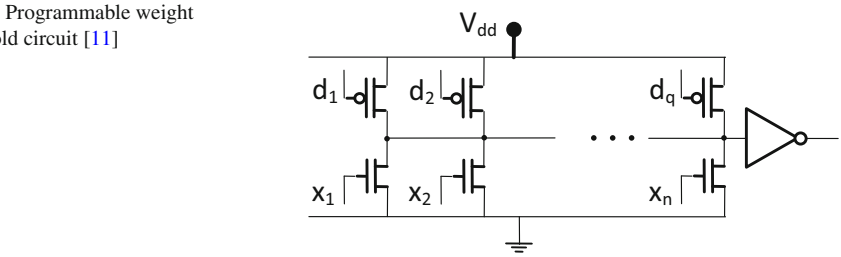

Fig. 8 Programmable weight threshold circuit [11]

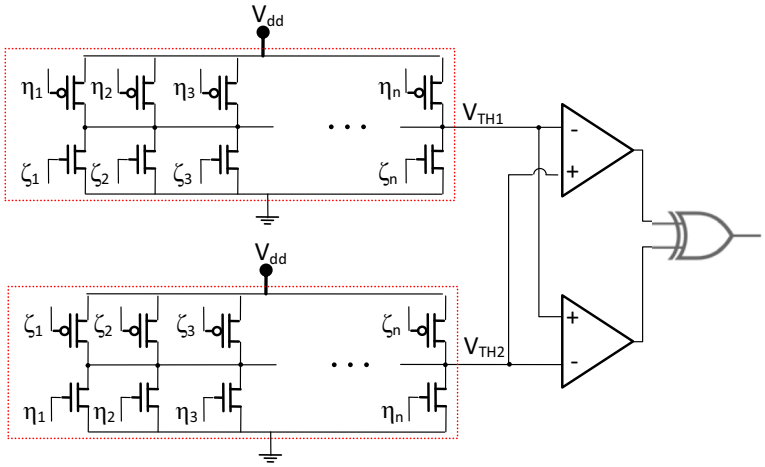

Fig. 9 Integrated Berger code checker unit

solve this issue, we have developed a novel scheme based on the programmable weight threshold circuit (PWTC). The PWTC circuit, initially introduced in Ref. [11], consists of a specific arrangement of CMOS transistors that the operation of the circuit depends on the value of the input (Fig. 8). The aspect ratio W/L of transistors are designed so that the pattern inequity provides the inverter threshold voltage. More details can be found in Ref. [11]. In this paper, we have modified this circuit so that it be feasible for large Berger code checker. In the proposed scheme, integrated Berger code checker unit (IBCC) unit illustrated in Fig. 9, the complicated aspect ratio calculations are resolved. Unlike the PWTC we have utilized two programmable threshold circuits (PTCs), in which the aspect ratio of all transistors is the same. Two latched comparators along with an XOR gate subsequently are placed in the proposed scheme to detect data inequality. The threshold circuit is arranged in complementary form, so that in one's input pattern $Z[n] = \{\zeta_1, \zeta_2, \ldots, \zeta_n\}$ feeds PMOS transistors and in the other one it is connected to NMOS transistors. All NMOS and PMOS transistors are supposed that have the same sizes $W_{\mathrm{nm}}/L_{\mathrm{nm}}$ and $W_{\mathrm{pm}}/L_{\mathrm{pm}}$.

As we illustrated in previous section, in arithmetic operations like addition or multiplication, the Berger code aims to detect the difference in the number of 1's in the two data patterns. We show that the proposed IBCC unit is able to satisfy this requirement. In PTCs, when ζ_{i} or η_{i} is high and equal to V_{dd}, the NMOS transistor is on, while the

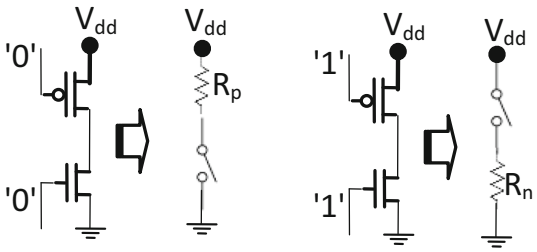

Fig. 10 Programmable weight threshold circuit

PMOS is off. This yields the equivalent circuit that are figured in Fig. 10. When a transistor is 'on' it is equal to a resistor that is indicated by R_n ad R_p. The programmable threshold circuits are driven by V_{dd} through the R_p resistors. The voltage value of PTC unit, V_{TH}, can be found by superposition as the super-imposing of the effects from each of the voltage sources. Equations (6) and (7) represent the total V_{TH} for each top and bottom PTCs, respectively. If we suppose $R_n \approx R_p$, the differential voltage that is applied on comparators can be formulated as Eq. (8). As expected, when number of 1′s in data patterns are the same, $N(\mathrm{Z}) = N(\mathrm{H})$, the applied voltage is equal to 0. An inequality, considered as a faulty state, imposes a differential voltage that is used to detect fault.

$$V_{\mathrm{TH1}} = \frac{N(H)\cdot R_{T_1}}{R_{T_1}+R_p}, \quad R_{T_1} = \left(\frac{R_n}{N(Z)} || \frac{R_p}{N(H)-1}\right) \tag{6}$$

$$V_{\mathrm{TH2}} = \frac{N(H)\cdot R_{T_2}}{R_{T_2}+R_p}, \quad R_{T_2} = \left(\frac{R_n}{N(Z)} || \frac{R_p}{N(Z)-1}\right) \tag{7}$$

$$V_{\mathrm{TH1}} - V_{\mathrm{TH2}} = \frac{2N(H)}{N(H)+N(Z)} - 1 \tag{8}$$

If the number of imbalanced bits, the faulty bits, is denoted by m, the differential voltage verses the number of 1's in information pattern, $N[H]$, can be depicted as Fig. 11. As evident from this figure, the larger the ratio $m/N[H]$, the better differential voltage is provided. While the number of engaged data bits, $N[H]$, are increased, the differential voltage is dropped, for instance $N[H] = 1000$ in millivolt order. Therefore, more sensitive comparator is required. Also the comparators can easily have designed to support microvolt orders, they may demand more challenges in area and power aspects. To resolve this requirement, we provide an independent comparator set for each array of engaged patterns. The data pattern in FIR filter taps, as illustrated in following, could be handled separately. Therefore, the conventional comparators can be applied in the fault tolerant scheme with no trouble. As mentioned, a single tap of filter just consists of one processing element (PE), the multiplication and accumulation, which the multiplier results serve as the adder input. If we suppose the Berger checker are merged for the i-th tap, the multiplier results check bits can be eliminated by the integration of Eqs. (3) and (5) and we have:

$$N[H_i]\times N[X_i] + N[S_{i-1}] = N[S_i] + N[C_i^A] + \sum_n N[C_i^M] \tag{9}$$

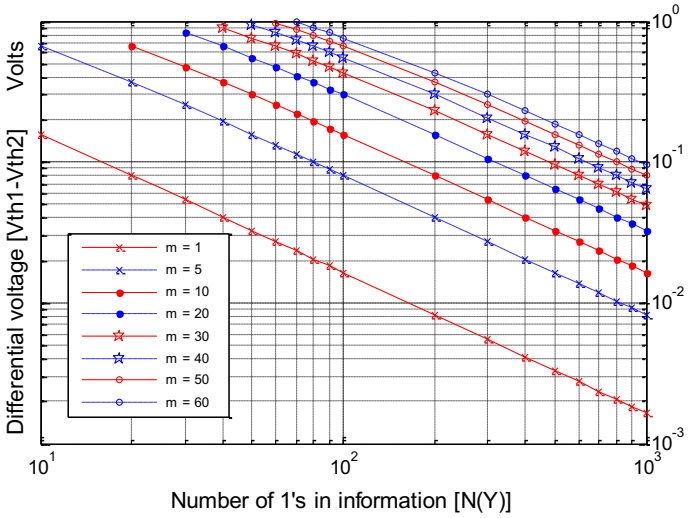

Fig. 11 Differential voltage versus number of 1's $\{V_{\mathrm{dd}} = 3.3v,\ R_n \approx R_p\}$

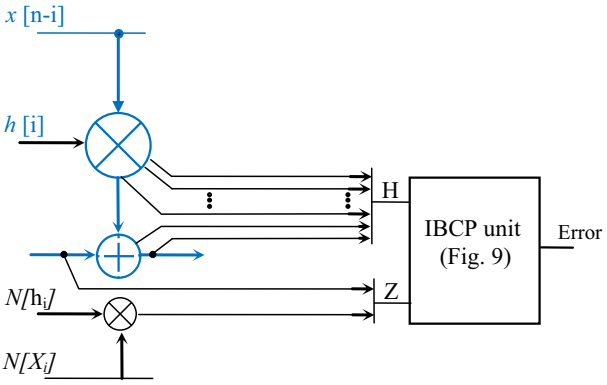

Fig. 12 Single tap integrated Berger code predictor (ST-IBCP)

in which H_i and X_i represents the number of 1's in the impulse response, $h[i]$, in the input pattern, $x[n-i]$, respectively. Also, S_i, C_i^A and C_i^M denote the Berger check bit in the adder result, adder's carry chain and multiplier carry chains correspondingly. A single tap integrated Berger code predictor (ST-IBCP) unit, according to Eq. (9), is illustrated in Fig. 12. In this figure, each PE requires an IBCP unit so that the Z and H length is equal to $n^2 + 2n + 1$. If ST-IBCP units are combined and a multi tap integrated Berger code predictor (MT-IBCP) is used, for a data-path quantization of n bits, when T taps are merged in a MT-IBCP unit, the equivalent $N[H]$ is calculated as:

$$\left(n^2 + 2n + 1\right) \times T + 2n \tag{10}$$

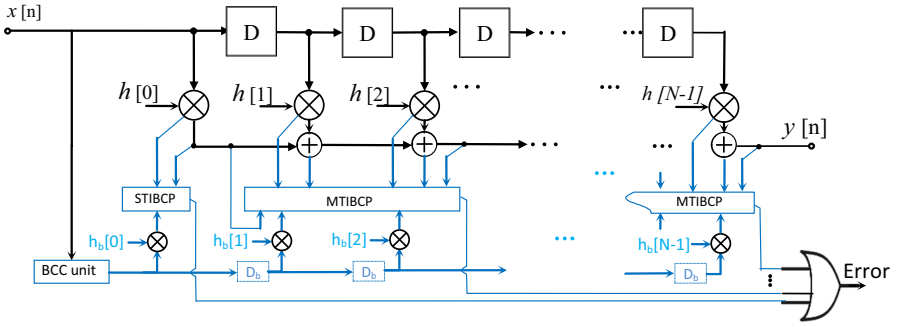

Fig. 13 Proposed integrated Berger coding scheme for direct form FIR digital filter

Figure 13 illustrates fault detection methodology based on integrated Berger predictors. This scheme concludes ST and MT-IBCP units, which their error signals are evaluated by an OR gate. Utilizing the ST or MT IBCPs and the number of merged taps depends on the comparator resolution. Also, it is better to mention that the W/L of all transistors in IBCP unit are the same, however, if the number of 1's in information are applied to threshold circuit instead of raw data, the W/L ratio are arranged as $W/L, 2W/L, 4W/L, \ldots, 2^k W/L$.

5 Evaluation

To evaluate the effectiveness of the proposed scheme, a number of cases are used. The quantized input data and coefficients are selected similar with previous works to compare results. Moreover, Triple Modular Redundancy (TMR), triplicates the design and adds voting logic to mask errors, is a classical fault tolerant solution that is used as the performance criterion for novel structures and the proposed methods are commonly compared with TMR. This method is able to mask single faults, so to provide an equivalent capability in proposed scheme, we have duplicated the original plan and added BC MBU detector and a multiplexer as indicated in Fig. 14. In Fig. 15, we developed the proposed scheme so that it provides 5-NMR ability in the fault mitigation. With an approximately similar fault mitigation level, the proposed technique is compared with conventional approaches and other literature. As detailed in Tables 1, 2 and 3, the results confirm that the proposed scheme can reduce the implementation

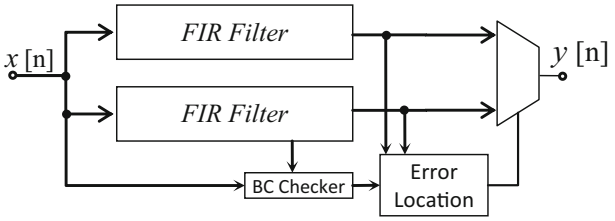

Fig. 14 Unidirectional MBU faults masking scheme based on Berger Code

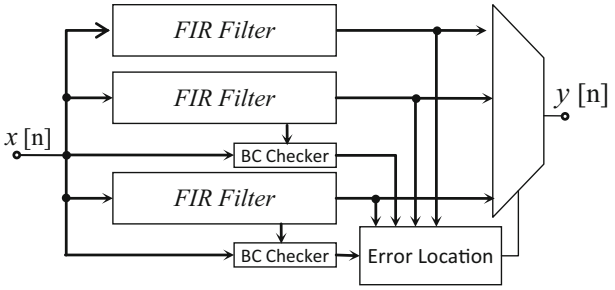

Fig. 15 MUMBU faults masking scheme based on Berger code

Table 1 Resource comparison for 11-orders FIR filter

T = 11-taps n = 16 bits	Logic utilization		Area overhead ratio versus plain		
	Plain	BSDMR	TMR	SDMR [21]	Proposed
Logic	29744	63652	3.03	2.247	2.14
Flip-flops	176	407	3	2.247	2.31

Table 2 Resource comparison for 16-orders FIR filter

T = 16-taps n = 8 bits	Logic utilization		Area overhead ratio versus plain			
	Plain	Proposed	TMR	Method in [6]*	Method in [8]	Proposed
Logic	11392	25440	3.03	2.39	2.11	2.23
Flip-flops	128	320	3	3.25	2.4	2.50

* Extracted from Ref. [8]

Table 3 Resource improvement percentage for 16-orders FIR filter

T = 16-taps n = 8 bits	Logic utilization		Improvement percentage versus TMR	
	TMR	Proposed	Efficient residue [7] (%)*	Proposed (%)
Logic	34216	25440	26.8	25.6
Flip-flops	384	320	−14.2	16.7

* For $m = 7$

cost significantly compared with the TMR. Furthermore, these results show that the IBCP-based FIR filters area overhead correlate fairly well with novel methods of other literature. However, the proposed approach not only identifies the SEU faults, but also it is able to detect all unidirectional MBUs.

Although, we have focused on analyzing the effects of SEUs and MBUs to assess the effectiveness of the scheme to detect errors. The fault injection experiments have been performed and the errors have been randomly inserted in the coefficients, inputs patterns and D registers of the filters. In all cases, single errors and unidirectional MBUs were detected and are masked. According to the filter size, a number of errors

on inputs and for filter coefficients were inserted in the fault simulation tool. This confirms the effectiveness of the scheme to detect and managing all single errors and multi-unidirectional errors in input patterns and coefficients.

6 Conclusion

A new method to implement fault tolerant FIR filters against single and unidirectional MBUs faults has been presented. The proposed scheme exploits the Berger code to implement an effective error detection mechanism. In comparison with previous fault tolerant filters that usually only single faults are detected and masked, in the proposed schemes not only single faults are covered but also, due to the Berger codes inherent specification, all unidirectional are handled. While the implementation results show that the Berger-based schemes impose the same area overhead.

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