

# Low-Power High-Linearity Switching Procedure for Charge-Redistribution SAR ADC

Xingyuan Tong<sup>1</sup> · Yawen Chen<sup>1</sup>

Received: 23 September 2016 / Revised: 16 December 2016 / Accepted: 21 December 2016 /  
Published online: 30 December 2016  
© Springer Science+Business Media New York 2016

**Abstract** An energy-efficient capacitive switching scheme in successive approximation register (SAR) analogue-to-digital converter (ADC) is proposed for biomedical applications. With novel sequence initialization and by reducing the up-switching steps during the A/D conversion, the average switching energy of this proposed procedure is reduced by over 98.7% compared with the conventional architecture after taking the parasitic capacitance into consideration. The number of capacitors in the proposed capacitor array is just 1/4 of that in the conventional switching scheme. Moreover, behavioral simulation performed in MATLAB for the 10-bit SAR ADC shows that the linearity performance of this proposed switching scheme is much better than that of previous architectures.

**Keywords** Analogue-to-digital converter (ADC) · Successive approximation register (SAR) · Switching procedure · Low-power · High-linearity

## 1 Introduction

Due to its high energy efficiency, charge-redistribution successive approximation register (SAR) analogue-to-digital converters (ADCs) have been very popular in biomedical electronics [10, 11, 13]. With the feature size of MOSFETs downscaled to nanometer level, the supply voltage of System-on-Chip (SoC) has been decreased to <1 V [13].

---

✉ Xingyuan Tong  
mayxt@126.com

Yawen Chen  
852897441@qq.com

<sup>1</sup> School of Electronic Engineering, Xi'an University of Posts and Telecommunications, Xi'an 710121, China

This is good for low-power and miniaturized digital circuit design. However, in charge-redistribution SAR ADC, the area of capacitor array cannot dramatically decrease due to the linearity requirement. Moreover, the capacitor array has been the dominant source of power dissipation in SAR ADC [10], especially when the comparator can be designed with a low-power dynamic regenerative latch.

Recently, various switching schemes have been developed to reduce the switching energy of these capacitor arrays in SAR ADCs [2,3,5–7,9,12,14]. In [6], highly energy-efficient switching was performed with obvious energy reduction during the first 3-bit cycles. Unfortunately, this advantage would be weakened by the energy-consuming parasitic capacitance in this architecture. By using down-switching instead of up-switching during the first several bit cycles, the scheme in [7] features better energy efficiency after taking the parasitic capacitance into consideration. However, any discussion of the SAR ADC switching schemes from energy consumption viewpoint would not be complete without considering its linearity performance. It is not easy to achieve good linearity performance by using these two schemes in [6,7]. In this paper, an improved capacitive switching procedure is proposed for low-power SAR ADC. Besides its low power and small size advantages, its linearity performance is also better than that of previous architectures.

## 2 The Proposed Switching Procedure

### 2.1 Proposed Capacitive Switching Scheme

The proposed switching procedure is illustrated with Fig. 1. Taking advantage of top plate sampling method and thanks to the tri-level switching technique, 4-bit conversion can be realized with a 2-bit capacitor array, as shown in Fig. 1. During the sample step,  $V_{ip}$  and  $V_{in}$  are sampled onto the top plates of the capacitor arrays, while the bottom plates of the capacitors are initially loaded with '1/2 1 1.' The bottom plate of the most significant bit (MSB) capacitor connects to  $V_{ref}/2$  and the other bottom plates are set to  $V_{ref}$ . At the end of sample phase, the sampling switches are turned off. The comparator directly compares  $V_{ip}$  and  $V_{in}$ , without any energy consumption of the capacitor array. During the second bit evaluation cycle, the voltage on the higher potential capacitor array will be decreased by  $V_{ref}/2$ , with all the bottom plates of this capacitor array connected to '0 1/2 1/2.' This step generates the 2nd bit, and still does not consume any switching energy. The other capacitor array's connection '1/2 1 1' does not change during the first 2-bit evaluation cycles. Based on the result of the 2nd bit, there will be two different switching methods for generating the 3rd bit. The first one is up-switching the capacitor array that connected to '1/2 1 1' to '1 1 1.' The other one is down-switching from '1/2 1 1' to '1/2 1/2 1/2.' There is still no energy consumption no matter which switching happen. To generate the following bits, only monotonic down-transitions are required. Different from that in [3], the reference range has been halved (from '1' to '1/2' or from '1/2' to '0') during these down-switching steps, resulting in further energy saving.

The input-dependent dynamic offset of the comparator can degrade the ADC performance [7]. Reducing the output common-mode variation of the capacitor array is



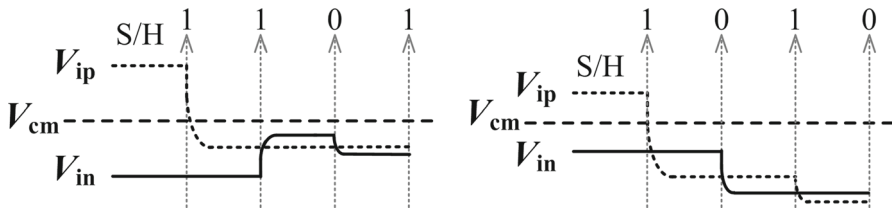


Fig. 2 Output waveform of the capacitor array with this proposed switching method

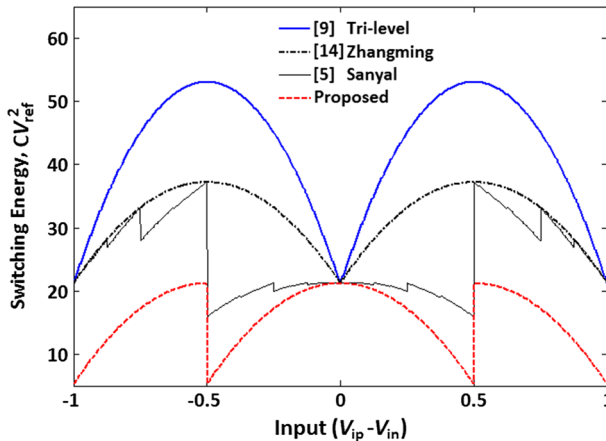


Fig. 3 Switching energy against input

## 2.2 Switching Energy Analysis and Comparison

The behavioral simulation for 10-bit SAR ADCs with different switching schemes was performed in MATLAB. Figure 3 compares the proposed procedure with several other schemes. With novel sequence initialization and by reducing the up-switching steps during the A/D conversion, this proposed SAR ADC switching procedure features very high energy efficiency. The average switching energy is  $15.8 CV_{ref}^2$ , which achieves over 98.8% switching energy reduction, compared with the conventional scheme. The detailed comparison with other switching schemes can be found in Table 1.

## 2.3 Effect of Parasitic Capacitance on Switching Energy

In reality, parasitic capacitance exists between any capacitor plate and substrate. It would be incomplete to analyze the switching energy without discussing parasitic capacitance [6]. Since all the top plates in each capacitor array are connected together, the parasitic capacitors between top plates and substrate can be analyzed as an additional separate capacitor  $C_{pt}$ , which makes the total capacitance of each capacitor array larger than the ideal value, thereby attenuating the output value of each array during conversion. The existence of  $C_{pt}$  can decrease the switching energy of a down-switching step, but will increase the energy of an up-switching one. Moreover, parasitic

**Table 1** Benchmarking with previous works for 10-bit SAR ADC

Switching scheme	Area ( $C$ )	Average energy ( $CV_{\text{ref}}^2$ )	
		$C_{\text{pt}} = C_{\text{pb}} = 0$	$C_{\text{pt}} = 0.1C_t, C_{\text{pb}} = 0.15C$
Conventional [2]	2048	1363.4	1686.1
Cap splitting [2]	2048	852.3	1021.2
Monotonic [3]	1024	255.5	225.2
$V_{\text{cm}}$ based [12]	1024	170.2	209.2
Tri-level [9]	512	42.4	69.0
Zhangming [15]	512	31.9	56.3
Sanyal [5]	512	25.1	50.7
Xingyuan [6]	512	15.8	43.7
Proposed	512	15.8	21.3

capacitance exists between the bottom plate of each capacitor and substrate. It will also consume energy to charge these bottom plate parasitic capacitors. As shown in Fig. 4, when the capacitor array switches its connection to ‘1 1 1’ from ‘1/2 1 1’, though the energy consumption would ideally be 0, it would consume energy to charge the capacitor  $2C_{\text{pb}}$  from ‘1/2’ to ‘1.’ In Fig. 4,  $C_{\text{pb}}$  represents the parasitic capacitance of a unit capacitor between bottom plate and substrate, and  $2C_{\text{pb}}$  is the parasitic capacitance of the capacitor  $2C$  in the array. Obviously, there will be no energy consumption for each bottom plate parasitic capacitor during its monotonic down-switching because only discharge happens.

From the analysis in Sect. 2.1, the switching energy consumed in the first 3-bit cycles is ideally zero, which is similar as that in [6, 7]. To further reduce the switching energy caused by the parasitic capacitance, the number of up-switching steps is dramatically reduced during the conversion. According to the analysis in Sect. 2.3, monotonic down-switching is beneficial to energy reduction. For comparison with [6, 7], and to make the discussion fair, the parasitic capacitance is assumed to be  $C_{\text{pt}} = 10\%C_t$  and  $C_{\text{pb}} = 15\%C$ .  $C_t$  is the total capacitance and  $C$  is the value of unit capacitor in the capacitor array. After taking the parasitic capacitance into consideration, Fig. 5 shows the comparison of the proposed switching scheme with previous architectures. The average switching energy of this proposed scheme is  $21.3 CV_{\text{ref}}^2$ , which is just 1.3% of that in the conventional architecture. Moreover, compared with [6] ( $43.7CV_{\text{ref}}^2$ ) and [7] ( $26.2CV_{\text{ref}}^2$ ), this proposed switching procedure achieves 51.3 and 18.7% switching energy reduction, respectively. Table 1 compares the switching energy of several different schemes for 10-bit SAR ADCs, before and after taking the parasitic capacitance into consideration.

### 3 Linearity Analysis and Comparison

As discussed in Sect. 2, switching energy of a capacitor array in SAR ADC is directly proportional to the value of unit capacitance. Generally, the minimum possible value

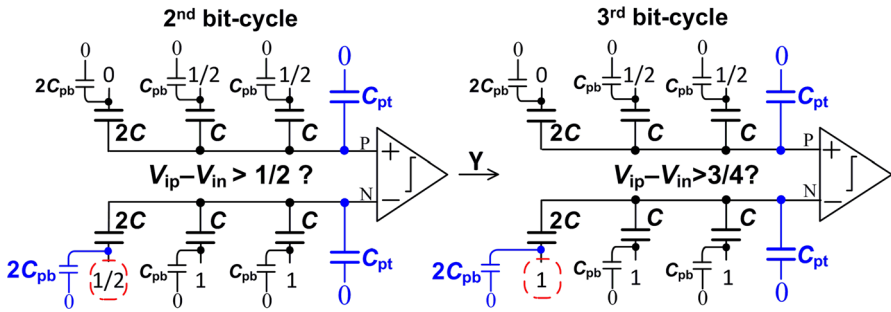


Fig. 4 Analysis of parasitic capacitance in the proposed procedure

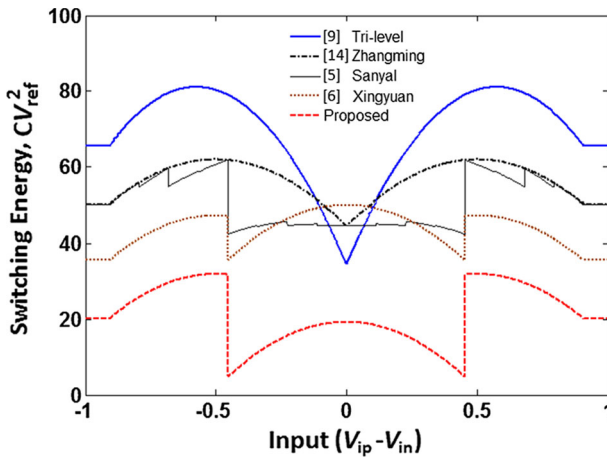


Fig. 5 Switching energy against input (with parasitic capacitance)

of a unit capacitor can be determined by  $KT/C$  noise, the capacitor matching performance, design rules and parasitic capacitance [4]. To make a fair discussion and comparison, it is assumed that the design rules and parasitic capacitances are not specific to any switching schemes. For medium- and high-resolution SAR ADCs, the reliable minimum unit capacitance is primarily determined by the capacitor matching performance [8]. The mismatch between any two capacitors in the capacitor array can directly affect the linearity performance of SAR ADCs, such as differential nonlinearity (DNL) and integral nonlinearity (INL). Therefore, it would not be fair to compare different SAR ADC switching schemes from switching energy perspective without having a discussion on linearity.

### 3.1 Linearity Analysis

Linearity of charge-redistribution SAR ADCs is related to the capacitor switching scheme and is mainly determined by the capacitor mismatch [8]. Ideally, the capacitors

in each capacitor array are binary weighted with

$$C_i = 2^i C, \quad i = 0, \dots, N - 2. \quad (1)$$

The capacitance variation associated with unit capacitor is assumed to be Gaussian distributed, with the normal variance  $\sigma_0^2$ , where  $\sigma_0$  is the standard deviation of unit capacitor. It is easy to verify that the variation of the error associated with capacitor  $C_i$  can be expressed as  $2^i \sigma_0^2$ .

To analyze the linearity caused by the capacitor variation, we assume that each capacitor is composed of its nominal value and its error term. Then, the output voltage,  $V_{\text{DAC}}$ , of the capacitor array for a given code  $d$  would have a deviation caused by the capacitance variation. As a result, DNL and INL can be derived theoretically to measure this deviation. DNL, by definition, can be expressed as follows:

$$\text{DNL}(d) = [V_{\text{DAC}}(d) - V_{\text{DAC}}(d - 1)] - \text{1LSB} \quad (2)$$

To determine INL, a best-fit curve,  $V_{\text{DAC,fit}}$  is introduced that passes through the end points of the  $V_{\text{DAC}}$  curve. Then, INL at the given code  $d$  can be defined as the difference between  $V_{\text{DAC}}(d)$  and  $V_{\text{DAC,fit}}(d)$ .

$$\text{INL}(d) = V_{\text{DAC}}(d) - V_{\text{DAC,fit}}(d) \quad (3)$$

According to (2) and (3), we can further get the variance of DNL and INL.

$$\begin{aligned} \text{Var}(\text{DNL}) &= \text{E}(\text{DNL}^2) - \text{E}^2(\text{DNL}) \\ \text{Var}(\text{INL}) &= \text{E}(\text{INL}^2) - \text{E}^2(\text{INL}) \end{aligned} \quad (4)$$

For the proposed switching scheme, according to the analysis in Sect. 2.1, the maximum INL is expected to occur at the 1/2, 1/4, or 3/4 of the full input range. At the middle of the input range, both these two capacitor arrays are connected to [1/2, 1, 1, ..., 1]. The output voltage of the capacitor array  $V_{\text{DAC}}$  can be expressed as follows:

$$\begin{aligned} V_{\text{DAC}} &= \frac{\left[ \sum_{i=1}^{k-2} (2^{i-1} C + \delta_{p,i}) + C + \delta_{p,0} \right] B_p^T}{2^{k-2} C + \sum_{i=0}^{k-2} \delta_{p,i}} \\ &\quad \frac{\left[ \sum_{i=1}^{k-2} (2^{i-1} C + \delta_{n,i}) + C + \delta_{n,0} \right] B_n^T}{2^{k-2} C + \sum_{i=0}^{k-2} \delta_{n,i}} \end{aligned} \quad (5)$$

The vectors  $B_p$  and  $B_n$  are used to represent the input of the capacitor array. At the middle of the input range,  $B_p = B_n = [1/2, 1, 1, \dots, 1]$ . Since the mean of the error term,  $\sum_{i=0}^{k-2} \delta_i$ , in the denominator should statistically equal to 0, it will be neglected during the calculation.  $k$  represents the ADC resolution. Similarly, the maximum DNL that occurs at the middle of the input range can be derived with  $B_{p,d} = B_{n,d} = [1/2, 1, 1, \dots, 1]$ ,  $B_{p,d-1} = [1/2, 0, 0, \dots, 1/2]$ , and  $B_{n,d-1} =$

**Table 2** Linearity comparison for 10-bit SAR ADC With  $\sigma_0/C = 3\%$ 

Switching scheme	Max deviation of DNL (LSB)	Max deviation of INL (LSB)
Conventional [2]	0.68	0.34
Monotonic [3]	0.48	0.48
Xingyuan [6,7]	0.76	0.68
Proposed	0.48	0.34

$[0, 1/2, 1/2, \dots, 1/2]$ . The maximum standard deviation values for the INL and DNL of the proposed scheme can be calculated as follows:

$$E \left[ \delta_{\max, \text{INL}}^2 \right] \approx \frac{9}{4} \frac{2^{k-4} \sigma_0^2}{C^2} \quad (6)$$

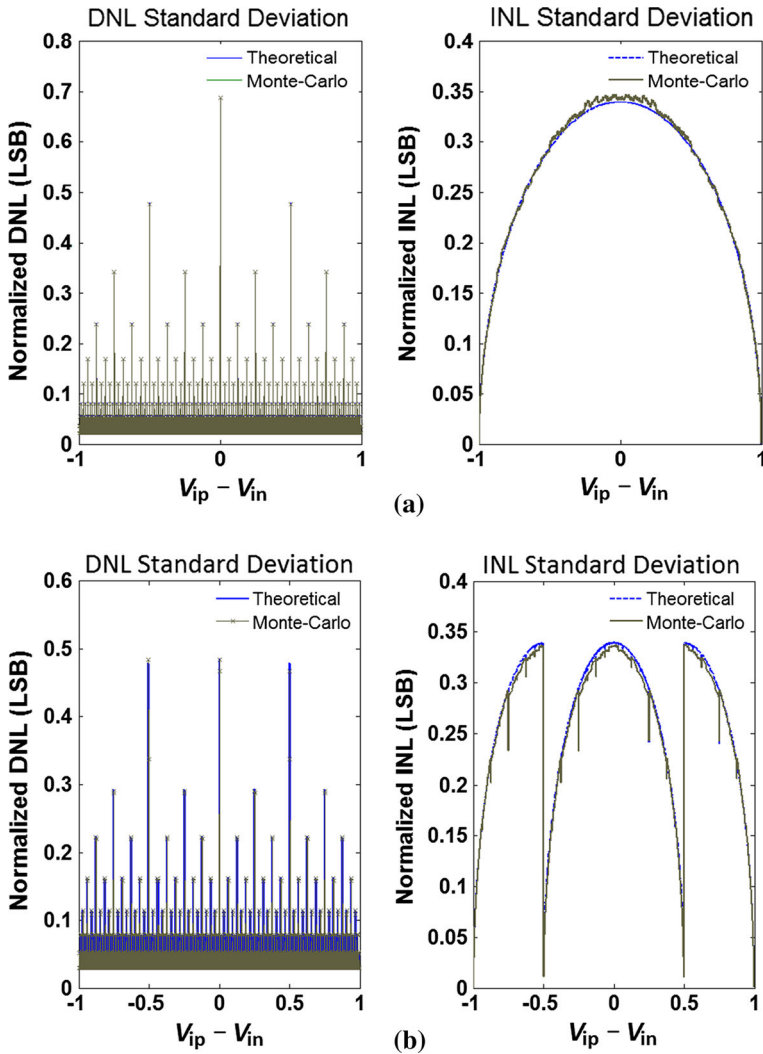
$$E \left[ \delta_{\max, \text{DNL}}^2 \right] \approx \frac{2^{k-1} \sigma_0^2}{C^2} \quad (7)$$

### 3.2 Linearity Simulation

In order to analyze the statistical linearity metrics of this proposed switching procedure, according to the analysis in Sect. 3.1, a theoretical model is constructed mathematically with MATLAB. About this theoretical model, we take the unit capacitor error of  $\sigma_0/C = 3\%$  into consideration, and calculate INL and DNL theoretically at each output code. To make the simulation results more convincing, we also constructed behavioral model with Monte Carlo concept. The principle of the behavioral model is similar as that in [1]. The capacitance variation associated with unit capacitor  $C$  is assumed to be Gaussian distributed. Then, the capacitance of each capacitor can be composed with its normal value and its variance. 2048 Monte Carlo runs were performed with a unit capacitor error of  $\sigma_0/C = 3\%$ . The simulation results for 10-bit capacitor array with proposed switching procedure from theoretical model and Monte Carlo model matched very well. It can be shown from Fig. 6 that the maximum standard deviations of DNL and INL in this proposed switching procedure were smaller than that in the conventional scheme. This means that the proposed switching scheme is less sensitive to the capacitor mismatch, compared with the conventional switching method.

Simulation for 10-bit models with several other switching schemes was also performed for comparison, which can be found in Table 2. Modeling with both theoretical method and Monte Carlo concept were performed for 10-bit SAR ADCs, with unit capacitor error of  $\sigma_0/C = 3\%$ . According to the simulation results in Table 2, this proposed switching scheme has the least standard deviations for both DNL and INL. The linearity advantage of this proposed switching procedure is due to the fact that only voltage shifts occur in the first two conversion steps, so there is no relative difference of the capacitor bottom plate switching in the capacitor arrays.





**Fig. 6** Standard deviation of DNL and INL **a** for the conventional switching scheme and **b** for the proposed switching procedure

### 4 Conclusion

An energy-efficient and high-linearity capacitor switching scheme had been proposed for charge-redistribution SAR ADC. Thanks to the novel sequence initialization, reduction of up-switching steps and tri-level switching method, the average switching energy is reduced by 98.7% after taking parasitic capacitance into consideration, compared with the conventional architecture. The number of unit capacitors in the proposed capacitor array is also reduced to 1/4 of that in the conventional scheme. Moreover, linearity analysis has also performed by MATLAB modeling with both theoretical and

Monte Carlo methods. It has been shown that this proposed switching procedure is less sensitive to capacitor mismatch, making it more suitable in biomedical applications.

**Acknowledgements** We would like to thank Yang Zhang in Xi'an University of Posts and Telecommunications for helpful discussions. This work was supported in part by the National Natural Science Foundation of China (Nos. 61204029, 61674122), the Natural Science Foundation of Shaanxi in China (No. 2014JQ8332) and the Special Scientific Research Foundation of Shaanxi Education Department in China (No. 16JK1705).

## References

1. S. Brenna, A. Bonetti, A. Bonfanti, A.L. Lacaita, An efficient tool for the assisted design of SAR ADCs capacitive DACs. *Integr. VLSI J.* **53**, 88 (2016)
2. B.P. Ginsburg, A.P. Chandrakasan, An energy-efficient charge recycling approach for a SAR converter with capacitive DAC, in *IEEE International Symposium on Circuits and Systems* (2005), p. 184
3. C.C. Liu, S.J. Chang, G.Y. Huang, Y.Z. Lin, A 10-bit 50-Ms/s SAR ADC with a monotonic capacitor switching procedure. *IEEE J. Solid-State Circuits* **45**, 731 (2010)
4. M. Saberi, R. Lotfi, K. Mafinezhad, A. Serdijn, Analysis of power consumption and linearity in capacitive digital-to-analog converters used in successive approximation ADCs. *IEEE Trans. Circuits Syst. I Regul. Pap.* **58**, 1736 (2011)
5. A. Sanyal, N. Sun, SAR ADC architecture with 98% reduction in switching scheme for SAR ADC. *Electron. Lett.* **49**, 248 (2013)
6. X. Tong, M. Ghovanloo, An energy-efficient switching scheme in SAR ADC for biomedical electronics. *Electron. Lett.* **51**, 676 (2015)
7. X. Tong, Y. Zhang, 98.8% switching energy reduction in SAR ADC for bioelectronics application. *Electronics Letters* **51**, 1052 (2015)
8. X. Yue, Determining the reliable minimum unit capacitance for the DAC capacitor array of SAR ADCs. *Microelectron. J.* **44**, 473 (2013)
9. C. Yuan, Y. Lam, Low-energy and area-efficient tri-level switching scheme for SAR ADC. *Electron. Lett.* **48**, 482 (2012)
10. D. Zhang, A. Bhide, A. Alvandpour, A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13- $\mu$ m CMOS for medical implant devices. *IEEE J. Solid-State Circuits* **47**, 1585 (2012)
11. X. Zou, W. Liew, L. Yao, Y. Lian, A 1V 22 $\mu$ W 32-channel implantable EEG recording IC. *ISSCC Dig. Tech. Papers* (2010), p. 126
12. Y. Zhu, C.-H. Chan, U.F. Chio, S.W. Sin, S.-P. U, R.P. Martins, F. Maloberti, A 10-bit 100-MS/s reference-free SAR ADC in 90nm CMOS. *IEEE J. Solid-State Circuits* **45**, 1111 (2010)
13. Z. Zhu, W. Bai, A 0.5-V 1.3- $\mu$ W analog front-end CMOS circuit. *IEEE Trans. Circuits Syst. II Exp. Briefs* **63**, 523 (2016)
14. Z. Zhu, Y. Xiao, X.L. Song,  $V_{cm}$ -based monotonic capacitor switching scheme for SAR ADC. *Electron. Lett.* **49**, 327 (2013)
15. Z. Zhu, Z. Qiu, M. Liu, R. Ding, A 6-to-10-bit 0.5V-to-0.9V reconfigurable 2MS/s power scalable SAR ADC in 0.18 $\mu$ m CMOS. *IEEE Trans. Circuits Syst. I Regul. Pap.* **62**, 689 (2015)