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Current Starving the SRAM Cell: A Strategy to Improve Cell Stability and Power

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Abstract In SRAM cell design, the energy consumption and cell stability are the major performance indices which need to be improved. Several techniques reported earlier attempt to improve either of the stability or the energy consumption. In this paper, a scheme is proposed which uses current starving on conventional SRAM cell to improve cell stability and also to reduce energy consumption. Unlike separating the read and write port of the SRAM cell in most of the techniques proposed earlier, this technique results more ideal voltage transfer characteristic of the cross-coupled inverter leading to larger noise margin. It also reduces the dynamic energy consumption through short circuit current reduction during state transition. The proposed technique is compared with NC-SRAM [3], IWLVC-SRAM [18], 10T-SRAM [16] and a conventional 6T-SRAM cell. The read and retention stability of the current starving SRAM (CS-SRAM) cell increases by 31 and 41%, respectively, with respect to the 6T-RAM cell. These two SNMs are also significantly higher than the other compared cells. The proposed technique consumes 22% lesser energy in comparison with the 6T-SRAM. The energy consumption is also reduced in comparison with the other compared cells. The compared cells are designed both in CMOS process and in FinFET technology

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(20 nm PTM library). The performance enhancement of the proposed cell maintains same trend in both technologies.

Keywords Read and retention SNM · WNM · Process variation · Current starving · FinFET · Short circuit current

1 Introduction

The difference between supply voltage and transistor threshold voltage has come down to a very small level in modern SoC design. As a result, the stability has come down to a problematic zone and hence becomes an important matter of concern [22]. For SRAM cell, this stability problem is even more significant as it is design with minimum feature size. Also the scaling of transistor into the sub 100 nm region further degrades the stability of the SRAM cell. Hence, maintaining desired stability of SRAM cell during supply voltage scaling and transistor size scaling is of utmost necessity in SRAM cell design. The desire to embed more and more functionality in to the embedded system demands the energy consumption also to be reduced as much as possible.

Several techniques have been employed to increase the stability of the SRAM cell. Liu et al. [10] have proposed a 9T-SRAM cell which separates the bit lines from the internal nodes during read operation to increase the read stability. Lin et al. [8] have proposed another 9T-SRAM cell to improve cell stability by separating read and write port of the cell. Verma et al. [23] have proposed an 8T SRAM cell which uses a buffered read mechanism to separate read and write port to overcome read instability. A single-ended pass-gate-based 10T SRAM cell is proposed by Noguchi et al. [15]. In this cell, the data stored are first buffered by an inverter and then transferred to the read bit line through a pass gate. In these above reported works, the basic idea is to separate the internal storage node from the pre-charged bit line during read operation which increases their read stability.

Elakkumanan et al. [3] have proposed an 8T-SRAM cell (NC-SRAM) targeting energy reduction by lowering gate leakage current. The source voltage of the driver NMOS of NC-SRAM cell is connected to a positive ground potential during standby mode and to a normal ground potential during active mode, using two additional pass transistors and an extra voltage source. Though the positive ground potential helps in reduction of leakage current, but the frequent switching activity of additional pass transistors used in this design, during each active operation and the frequent sifting of the driver NMOS source potential from normal ground level to the positive ground level and again back to the normal ground level, leads to a major energy overhead. This may nullify the energy gain by leakage reduction. Despite the use of eight transistors, this cell does not take any action to increase the cell stability. Razavipour et al. [18] have proposed a 9T-SRAM cell (IWLVC-SRAM) targeting energy reduction. They modified the NC-SRAM cell with an extra PMOS in the word line path which increases the access transistors' gate voltage during standby mode. Thus the leakage of the gate transistor is reduced during standby mode. The extra PMOS in the word line not only increases area overhead but also increases cell delay. Despite the use of nine transistors, this cell also does not take care of stability of the cell. A high stable SRAM cell is

proposed by Abhijit Sil et al. [21] which uses extra two transistors so that the internal data node does not come in the read path, thus avoiding read noise insertion. Since it uses single-ended read process, differential sensing of data is not possible with this cell which increases the read delay. The energy consumption during read operation is also increased because of the full swing of the read bit line from V_{DD} to 0. The write ability of this cell is also a major challenge since it uses a single-ended write process instead of the double-ended write process. A 7T-SRAM cell is proposed by Forshad Moradi et al. [11] for low power application. It uses an extra NMOS to nullify the erroneous increase in the data node during read operation. The noise inserted to the data node weakens the additional NMOS, thus, nullifying the inserted noise. But the additional NMOS weakens the read path significantly. Since the cell uses a single-ended read process, differential data sensing is not possible. Thus, the full bit line swing through the weak read path makes the read process significantly slow. This cell does not implement any energy reduction technique to reduce energy consumption. A 10T-SRAM cell is proposed by Prasad et al. [16] which targets for both energy reduction and stability enhancement. It uses a diode-connected NMOS to reduces the effective operating voltage, which reduces the dynamic energy consumption. To compensate the stability reduction due to lowering the operating voltage, it uses two extra PMOS in between the pull-up and pull-down transistors of the cross-coupled inverter. The cell consumes huge area because of the large number of transistors used. Discharging of bit line during read operation takes significantly more time as the read path contains four transistors. Hence the read process becomes much slower. An ultra-low standby power SRAM cell is proposed by Hanson et al. [5] to minimize standby power. This cell uses two PMOSs and two NMOSs in series in the pull-up and pull-down path of the cross-coupled inverter pair. The use of the read buffer circuit in this cell eliminates the read noise insertion problem. But the use of fourteen transistors makes the area overhead significantly high.

In this work, we propose a current starving SRAM cell (CS-SRAM) which targets both stability improvement as well as energy reduction. It increases the cell stability by increasing the stability of the cross-coupled inverter pair. It also temporarily decreases the effective operating voltage across the cross-coupled inverter pair during write operation which reduces it's short circuit current flow and hence the energy consumption. Since the NC-SRAM cell [3] and IWLVC-SRAM cell [18] targets the energy reduction by the help of additional transistors, they are chosen for comparison with our proposed cell. The 10T-SRAM cell [16] targets both the energy consumption and stability like the proposed CS-SRAM cell. Hence, this cell is also chosen for comparison with the CS-SRAM cell.

The proposed current starving technique has the following novelties and advantages.

1. It uses a current starving technique to make the VTC of the cross-coupled inverter pair more ideal in nature. This improves both the retention and read SNM of the proposed technique thus making the cell more stable.
2. Dynamic energy consumption is reduced by the reduction of short circuit current during state transition.
3. The write ability of the proposed technique is better with respect that of the other compared cells.

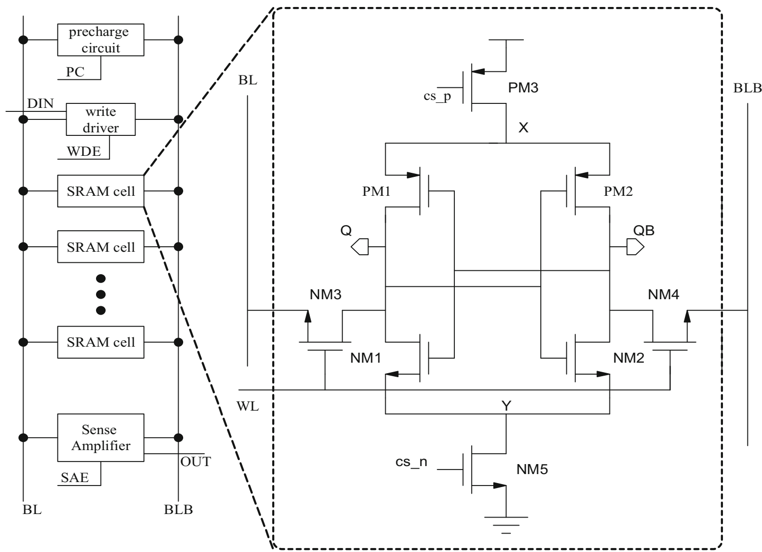


Fig. 1 Proposed CS-SRAM cell topology

4. The performance improvement of the proposed technique is also validated at a deeply miniaturized dimension by using 20 nm Predictive Technology Model's library.

The stability, energy consumption, write ability, delays, and area occupancy of the proposed CS-SRAM cell is compared with those of the NC-SRAM cell [3], IWLVC-SRAM cell [18], 10T-SRAM cell [16] and also with those of a conventional 6T-SRAM cell. The remaining portion of the paper is described as follows. The proposed CS-SRAM cell and its design consideration are described in Sects. 2 and 3, respectively. The performance analysis is presented in Sect. 4. In Sect. 4.5 the physical design considerations are analyzed. Finally, the conclusion of the work is presented in Sect. 5.

2 Current Starving SRAM Cell: The Proposed Strategy

The current starving technique is applied to SRAM cell and shown in Fig. 1. NM1-NM4 and PM1-PM2 form a 6T-SRAM cell. The source of NM1 and NM2 is connected to ground through a current starving NMOS NM5. The gate of NM5 is connected to a control voltage to limit the current starving effect of NM5. Similarly, the source of PM1 and PM2 is connected to V_{DD} through PM3. The PM3 is supplied a controlled gate voltage. The proposed current starving technique takes care of two major aspects. It enhances the cell stability and reduces dynamic energy consumption.

2.1 Stability Enhancement

When a SRAM cell stores any particular state, one of the internal node stores a '1' and the other node stores a '0.' It is desirable that any spurious increase in the 0-node voltage should not cross the switching threshold voltage of the other cross-coupled inverter

as it can flip the stored data. Static noise margin (SNM) [1,20] is the performance index of the SRAM cell to measure the limits up to how much the 0-node voltage can increase without affecting the stored data. To achieve the SNM of the SRAM cell, the VTC (voltage transfer characteristic) of one of the cross-coupled inverter and the inverted VTC of the other inverter are plotted on the same plot. Two largest possible squares are drawn in two lobes of the butterfly diagram. The side of the smaller square is taken as the SNM of SRAM cell [2,4]. Clearly, the SNM can be increased by making the VTC of the inverter more ideal in nature. This idea is employed in the proposed CS-SRAM cell to improve stability.

Conventionally cell ratio was the only parameter in designers' hand to improve cell stability [6]. But though increased cell ratio increases stability, it decreases the write ability. The proposed technique does not solely depend on cell ratio for stability enhancement. Rather the effect of NM5 makes sharp transition of the VTC of the cross-coupled inverter pair. The change in control voltage cs-n and cs-p changes the position of VTC transition. So the designers have two extra control parameters in their hand to increase the stability of the SRAM cell.

In Fig. 1 NM1-PM1 constitutes inverter-1 and NM2-PM2 constitutes inverter-2. Typically the control voltage cs-n is set higher than V_{th} of NM5 so that NM5 will be completely switched on. As NMOS is a good conductor of '0' the 'Y' node is not affected by the presence of NM5 throughout the hold mode. Hence, the data stored at 'Q' node are also unaffected by the presence of NM5. The NM5 just give a resistance in the path from 'QB' node to GND. Now suppose 'Q' and 'QB' node stores '0' and '1,' respectively. Let during read operation, the pre-charged bit line 'BL' inserts some noise voltage to the 'Q' node which raises the 'Q' node potential. This spurious increase in the 'Q' node potential will partially switch on NM2. Had it been a conventional 6T-SRAM cell the 'QB' node would immediately start to fall as it would have got a direct path to GND. This effect would have got a positive feedback from inverter-1. But the current starving NMOS (NM5), in the proposed technique, provides resistance in the path from 'QB' node to GND. Because of this additional resistance in the 'QB'-GND path, NM2 needs to be switched on more strongly, to allow same amount of current as the 6T-SRAM cell, to flow from 'QB' to GND. This needs the noise value at 'Q' to be high enough to degrade 'QB.' Hence, the reduction of 'QB' does not start with a small noise value as in case of the 6T-SRAM cell. This can be visualize from Fig. 12 where the VTC of the SRAM cells are drawn to find out their SNM. From Fig. 12c it can be found that the 'QB' starts to drop from a very low 'Q' value for 6T-SRAM cell, whereas the Fig. 12a shows that the 'QB' starts to drop when the 'Q' value is around $V_{\text{DD}}/2$. Hence, VTC curve of the inverter pair of the proposed CS-SRAM cell is more ideal in nature which leads to increase in its stability.

2.2 Dynamic Energy Reduction

A major component of the dynamic energy consumption of SRAM cell is the short circuit energy during state transition of the cell. As shown in Fig. 2 both the pull-up and pull-down transistors conduct in the interval t1 to t2 during the state transition which leads a short circuit current to flow from V_{DD} to GND. This short circuit current can be

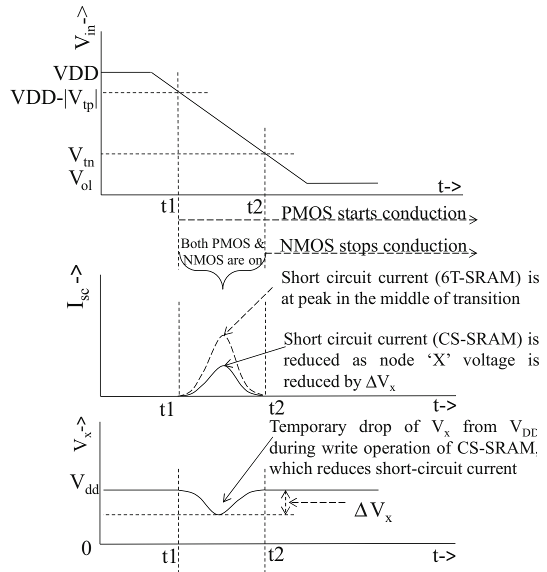


Fig. 2 Short circuit current during state transition

reduced by lowering the effective operating voltage, temporarily during the transition period. The proposed technique follows this idea to reduce its short circuit current. The proposed CS-SRAM cell uses a control transistor PM3 which provides a stacking effect to the cross-coupled inverter pair. It uses another control transistor between the cross-coupled inverter pair and ground. Unlike the NC-SRAM and IWLVC-SRAM compared here, the CS-SRAM does not require any switching activity for these control transistors during each active operation. Hence there is no significant energy overhead because of these two control transistors. The control transistor PM3 provides a stacking effect to the 'X' node. So, when one of the bit lines is pulled down by the write driver during write operation, the 'X' node is also pulled down. But this effect is temporary, since with the state transition, the 'X' node gets connected to the other bit line which is clamped at V_{DD}. So, 'X' node again charges upto V_{DD}. Thus, the 'X' node voltage is dipped temporarily only during state transition when the short circuit current is prominent. In a similar manner, the 'Y' node voltage also gets a temporary glitch during the state transition. The temporary dip of 'X' node and glitch of 'Y' node, results from the stacking effect of control transistors, reduces the effective operating voltage across the cross-coupled inverter pair. But this reduction is only during the state transition, thus the other performances such as read speed and stability are not affected by this phenomenon.

3 Current Starving SRAM: Design Considerations

As explained in Sect. 2.1, the resistance of NM5 increases the amount of noise insertion needed at 'Q,' to degrade 'QB' node. Hence, the VTC of the cross-coupled inverter starts to drop at a higher 'Q' value for high resistivity of NM5. Since the resistivity

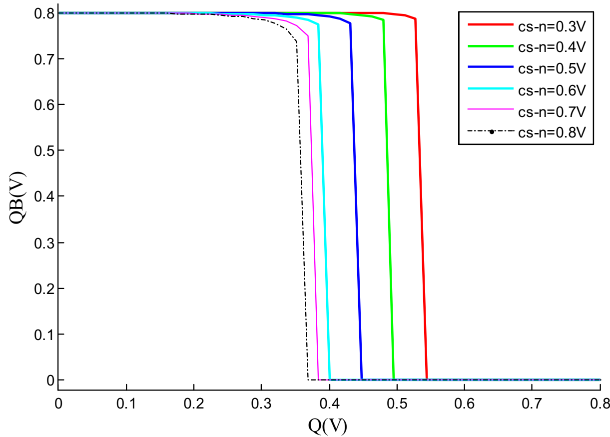


Fig. 3 Change of VTC with respect to control voltage cs-n

Table 1 Retention stability matrix (V)

cs-p (V)	cs-n (V)							
	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8
0	0.18	0.21	0.26	0.30	*0.35*	*0.37*	*0.36*	*0.35*
0.1	0.18	0.21	0.26	0.30	*0.35*	*0.37*	*0.37*	*0.35*
0.2	0.18	0.21	0.26	0.30	*0.35*	*0.37*	*0.36*	*0.35*
0.3	0.18	0.21	0.26	0.30	*0.35*	*0.37*	0.35	0.34
0.4	0.18	0.21	0.26	0.30	*0.36*	*0.37*	0.34	0.32
0.5	0.17	0.21	0.27	0.33	*0.37*	0.29	0.26	0.22
0.6	0.15	0.24	0.35	0.22	0.11	0.10	0.10	0.10
0.7	0.01	0.01	0.00	0.00	0.00	0.00	0.00	0.00

of NM5 decreases with increase in cs_n voltage, the transition point of VTC curve moves toward left with increase in cs-n voltage. This is illustrated in Fig. 3. It can be clearly marked from Fig. 3 that the transition point of the VTC curve moves leftward with increase in the cs-n voltage. Similarly when the cs-p increases, the resistivity of PM3 increases which weakens the power supply to the cross-coupled inverter. Thus, the 'QB' node starts degrading with relatively low amount of noise at 'Q' node. Thus, the transition point of the VTC moves leftward with increase in cs-p voltage.

The cs-n and cs-p value pair for which the transition of VTC occurs as close as possible to the $V_{DD}/2$ point is to be found out which will make the VTC more ideal in nature and hence, the size of the possible embedded square in the VTC lobe will be maximum, leading to a higher SNM value. The best cs-p and cs-n voltage pair which maximizes the retention SNM can be found from the retention stability matrix stated in Table 1. Similarly the read stability matrix stated in Table 2 shows the change of read SNM of the proposed cell with respect to the change of cs-n and cs-p voltage. The change of read and retention SNM with respect to cs-n and cs-p voltage is also

Table 2 Read stability matrix (V)

cs-p (V)	cs-n (V)							
	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8
0	0.02	0.04	0.07	0.10	*0.12*	*0.13*	*0.12*	*0.12*
0.1	0.02	0.04	0.07	0.10	*0.12*	*0.13*	*0.12*	0.11
0.2	0.02	0.04	0.07	0.10	*0.12*	*0.12*	*0.12*	0.11
0.3	0.02	0.04	0.07	0.10	*0.12*	*0.12*	0.11	0.10
0.4	0.02	0.04	0.07	0.10	0.11	0.10	0.10	0.09
0.5	0.00	0.04	0.06	0.07	0.07	0.04	0.03	0.02
0.6	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
0.7	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00

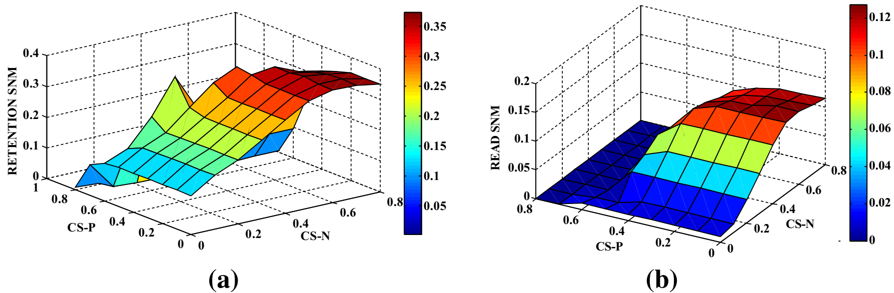


Fig. 4 Change of **a** retention SNM **b** read SNM in Volt with respect to change in cs-n and cs-p voltage

depicted in Fig. 4a, b, respectively. In the retention stability matrix, the SNM values which are >0.35 V are italicized. Similarly, in the read stability matrix the read SNM >0.12 V are italicized. Intersecting retention and read stability matrix, we can find a range of cs-n and cs-p voltage for which both read and retention SNM are improved. From this range of cs-n and cs-p values, we chose the cs-n and cs-p voltage which also reduces the energy consumption. We chose a lower cs-n value and a higher cs-p value from the above obtained range of cs-n and cs-p, to reduce energy consumption. The cs-n and cs-p values are taken as 0.5 and 0.2 V, respectively. Figure 5a, b shows the voltage reference circuits to generate the reference voltage cs-n and cs-p, respectively.

Using gpdk-90 nm CMOS technology library [16], the array of current starving SRAM cell was designed. To ensure a disturbance free read operation, the resistance of the pull-down transistor should be less than that of the access transistor [17]. So the width of access transistor, pull-up transistor and PM3 are set to 120 nm. The width of pull-down transistors is set to 240 nm and that of NM5 is set to as 180 nm.

4 Performance Analysis of the Proposed Cell

The SRAM cell array with current starving technique was simulated using Spectre at the Cadence analog design environment at room temperature (27 °C) using a power supply of 0.8 V. The simulation is performed at 1 GHz and analyzed. The signals

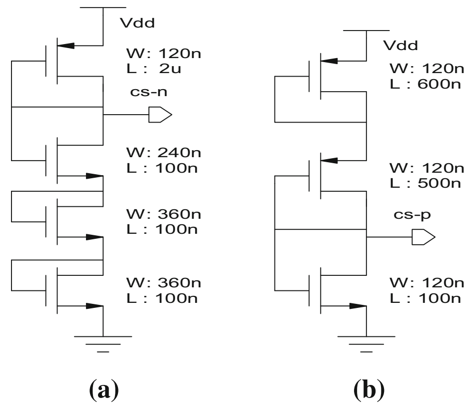


Fig. 5 Voltage reference circuit for **a** cs-n and **b** cs-p signal generation

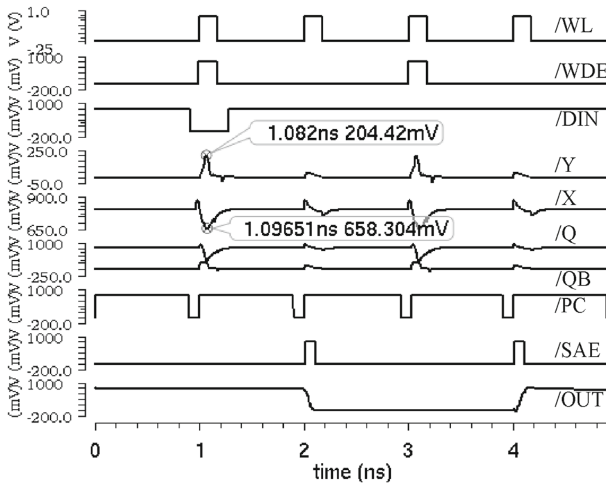


Fig. 6 Transient analysis of CS-SRAM cell at 1 GHz operation

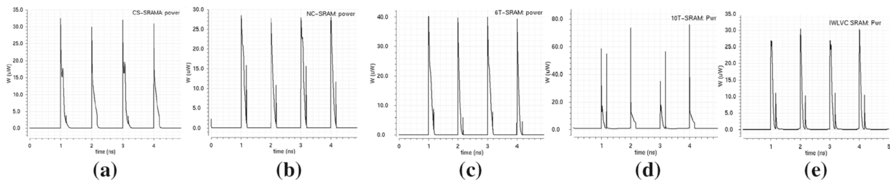


Fig. 7 Power consumption of different SRAM cells during 1 GHz access **a** CS-SRAM cell **b** NC-SRAM cell **c** 6T-SRAM cell **d** 10T-SRAM cell **e** IWLVC-SRAM cell

associated with the accessed cell, during transient analysis, are depicted in Fig. 6. The figure shows that at 1ns, ‘0’ is written to the cell and it is readout at 2ns. So the ‘OUT’ signal goes low at 2 ns. Again at 3 ns, ‘1’ is written to the cell and it is readout at 4 ns which raises the ‘OUT’ signal at 4 ns.

During the write operation, the data to be written are given to ‘DIN’ line. Then the ‘write driver enable’ (WDE) signal is activated which is followed by the activation of ‘word line’ (WL) signal. When the ‘WDE’ is activated, one of the bit lines goes high and the other goes low, depending on the data at ‘DIN.’ Then the ‘WL’ is activated which allow the bit lines to overwrite the data stored in the cell. The ‘Q’ and ‘QB’ node values are flipped, which can be marked from Fig. 6. During read operation, first the precharge circuit is enabled by deserting ‘PC’ signal and the bit lines are pre-charged to V_{DD} and then the WL is activated. Depending on the data stored, one of the bit lines starts discharging. Once the difference between the bit line pair is sufficient to be sensed, the sense-amplifier [9] is enabled by asserting the ‘SAE’ signal. Then the data is read to the ‘OUT’ signal.

A simulation window of 4 ns is chosen from 1 to 5 ns for power analysis. The power consumption for this interval is shown in Fig. 7a. The total dynamic energy consumption is estimated by integrating power consumption during read and write operations within this interval. Similarly the total static energy consumption is estimated by integrating power consumptions during stable intervals between write and read operations. The other compared SRAM cells are simulated in similar manner, and their dynamic and static energy consumptions are also calculated. This energy consumption of the discussed cells are compared and presented in Table 3. The energy comparison is also depicted in Fig. 8. The power consumption of the NC-SRAM cell, 6T-SRAM cell, 10T-SRAM cell and IWLVC-SRAM cell is depicted in Fig. 7b–e, respectively. The energy reduction, stability enhancement, write ability and speed of operation of the proposed technique is described below.

4.1 Energy Reduction

It can be noted from Table 3 that the energy consumption of the proposed CS-SRAM cell is much less in comparison with the other SRAM cells. The reason can be explained as follows. Consider the ‘Q’ node of CS-SRAM (Fig. 1) stores ‘1.’ So, PM1 and NM2 are on. To write a ‘0’ to ‘Q’ node, ‘BL’ has to be pulled down to ‘0’ and ‘BLB’ is clamped at V_{DD}. The ‘X’ node of CS-SRAM cell is not clamped at V_{DD}, and it gets a stacking effect by the control transistor PM3. Since ‘X’ node is not directly connected to V_{DD} and PM1 is switched on initially, the ‘X’ node gets influenced by ‘BL’ and follows it. So, the ‘X’ node starts to reduce a little extent. But when the cell starts switching, PM2 starts conduction and hence, the ‘X’ node is connected to ‘BLB’ which is set to V_{DD}. Thus, ‘X’ node again charges to V_{DD}. Similarly, the ‘Y’ node gets a stacking effect from the control transistor NM5. If ‘Q’ is considered to store ‘1,’ then, NM2 is switched on initially. Hence, the ‘Y’ node is influenced by the pre-charged ‘BLB.’ So the ‘Y’ node voltage is raised. But with state transition, NM1 starts conduction, connecting the ‘Y’ node to ‘BL’ which is set at a low potential. So, the ‘Y’ node is voltage drops immediately to ‘0.’ Hence the ‘Y’ node gets a glitch during the state transition. The temporary dip of ‘X’ node voltage and the glitch of ‘Y’ node voltage during state transition, which is caused by the current starving transistors, reduce the effective operating voltage across the cross-coupled inverter pair. Thus, the short circuit current of the cell is reduced which reduces the dynamic

Table 3 Energy consumption of different SRAM cells (90 nm CMOS technology) during 1 GHz operation

SRAM cells	Operations							
	Energy consumption (aJ) during dynamic operations				Total dynamic energy (aJ) $= A + B + C + D = (E)$	Total static energy (aJ) (F)	Total energy $(aJ) = E + F$	Decrement w.r.t. 6T-SRAM cell (%)
	0-Write (A)	0-Read (B)	1-Write (C)	1-Read (D)				
This work	2073	1835	2069	1746	7723	19.76	7742.76	22.24
NC-SRAM [3]	2607	2025	2509	1885	9026	18.90	9044.90	9.16
10T-SRAM [16]	2091	1883	2027	1834	7835	741.21	8576.21	13.87
IWLVC-SRAM [18]	2613	1939	2519	1842	8913	92.73	9005.73	9.55
6T-SRAM	3027	1980	2998	1917	9922	35.65	9957.65	–

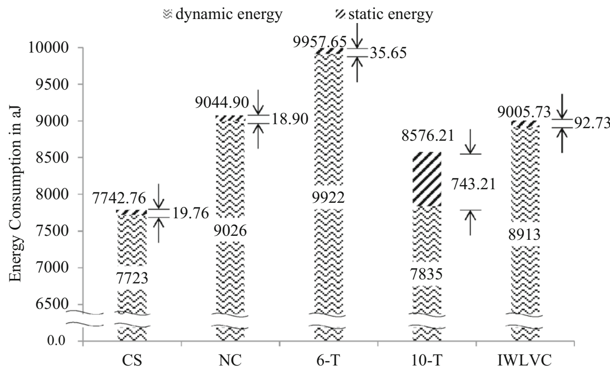


Fig. 8 Energy consumption of SRAM cells during 1 GHz operation

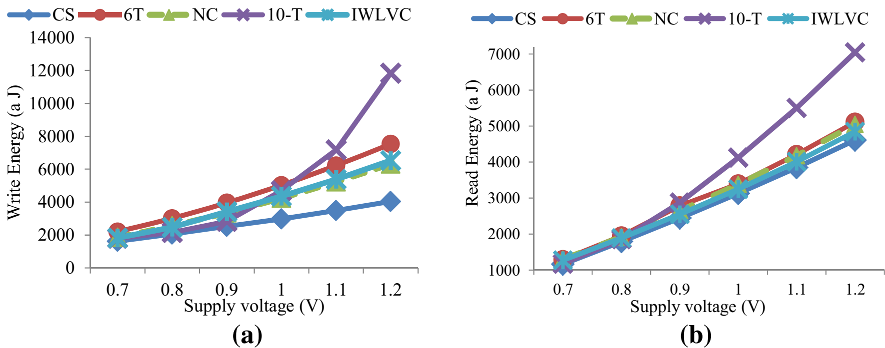


Fig. 9 Energy consumption of SRAM cells designed using CMOS technology (90 nm) during **a** write operation and **b** read operation

energy consumption. Figure 6 shows that the 'X' node voltage drops to 658 mV and the 'Y' node voltage rises to 204 mV during the middle of the state transition.

Figure 9a, b compares the write and read energy consumption, respectively, for the discussed cells at different supply voltages. The write energy of the proposed CS-SRAM is decreased by 26 and 46% from the 6T-SRAM, at a supply voltage of 0.7 and 1.2 V, respectively. Similarly, the energy consumption during read operation of the proposed technique is decreased by 9.7% from the 6T-SRAM both at 0.7 and 1.2 V supply voltage. The leakage current of the CS-SRAM cell is also reduced due to the impact of the current starving transistors. The leakage current of the discussed cells is compared and shown in Fig. 10. It shows that the leakage current of the CS-SRAM cell is significantly lesser than that of the other SRAM cells.

The additional voltage reference circuits used in the proposed technique to supply the control voltage (cs_n and cs_p) consume very little power in comparison with the total power consumption of the SRAM block and other peripherals. The two voltage reference circuits designed using 90 nm CMOS technologies consume an average of 245.7 nW power, whereas the average total power consumption of proposed technique is 9.013 μW and that of the conventional 6T-SRAM is 11.705 μW.

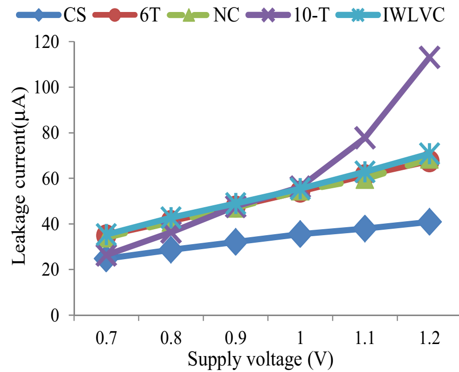
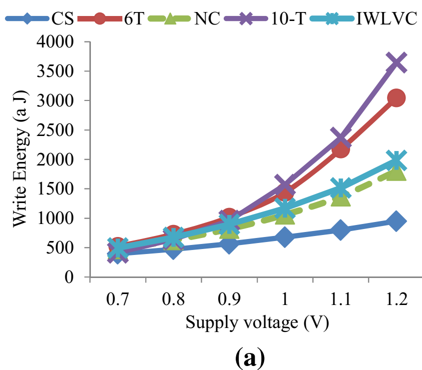


Fig. 10 Leakage current comparison of the SRAM cells designed using CMOS technology (90 nm)



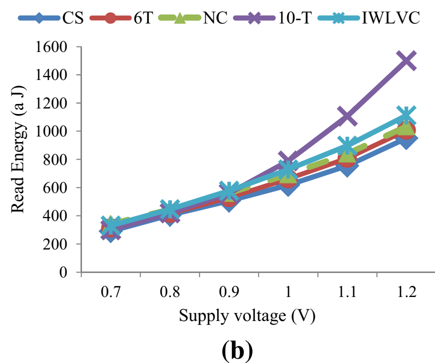


Fig. 11 Energy consumption of SRAM cells designed using FinFET (20 nm) during **a** write operation and **b** read operation

The performance enhancement through miniaturization of devices is in suspicions due to the interference of severe short channel effects. Hence, designers are switching to a new device structure like double-gate MOSFET (FinFET). To observe the performance improvement of the proposed technique in the miniaturized dimension, the compared cell arrays are also designed using Predictive Technology Model's 20 nm library. Figure 11 compares the write and read energy consumption of the discussed cells; those are designed using PTM 20 nm library. It shows that the reduction of read energy and write energy consumption in 20 nm design is maintaining almost similar trend to that in the 90 nm design.

4.2 Stability Enhancement

The retention and read stability of the CS-SRAM, NC-SRAM and 6T-SRAM, 10T-SRAM and IWLVC-SRAM cell are estimated from Fig. 12a–e, respectively. The VTC of one of the cross-coupled inverter and the inverted VTC of the other inverter are drawn simultaneously. The side of the largest possible square drawn in the VTC lobes is considered as the retention SNM of the SRAM cell. The read SNM is measured by keeping the setup similar to that during read operation. The retention SNM of these

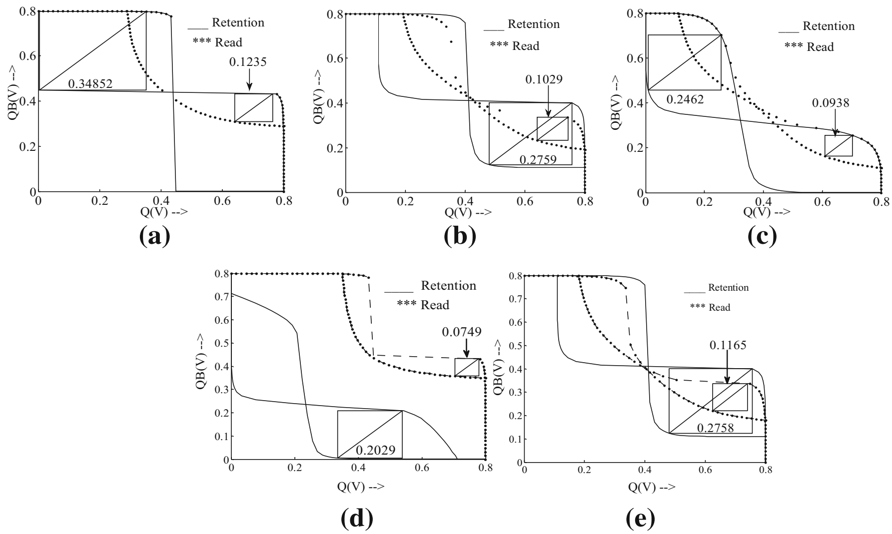


Fig. 12 The read and retention SNM of the compared SRAM cells designed using CMOS 90 nm technology **a** CS-SRAM cell **b** NC-SRAM cell **c** 6T-SRAM cell **d** 10T-SRAM cell **e** IWLVC-SRAM cell

SRAM cells is 348.5, 275.9, 246.2, 202.9 and 275.8 mV, respectively. Figure 12a shows that the VTC of CS-SRAM cell starts to drop when the ‘Q’ value is approximately $V_{DD}/2$, whereas from Fig. 12c we can find that the VTC starts to drop much before ‘Q’ approaches $V_{DD}/2$. So, the square that can be embedded in the lobes of the VTC is much larger in case of the CS-SRAM cell in comparison to that in 6T-SRAM cell and hence its SNM is larger. From Fig. 12b, e, it is found that the VTC of NC-SRAM and IWLVC-SRAM cell is ideal in nature. But since these two cells use a positive ground potential during standby mode, their V_{OL} remains at that positive ground potential and does not drop to 0. Hence, the size of the square embedded in the VTC lobe, for the NC-SRAM cell and IWLVC-SRAM cell, is smaller than that in the CS-SRAM cell and so is their SNM. The 10T-SRAM cell uses a diode-connected NMOS which permanently reduces the effective power supply to the cross-coupled inverter pair. Thus, the VTC curve of the 10T-SRAM cell starts from a lower value ($V_{DD} - V_{th}$) instead of V_{DD}, which can be found from Fig. 12d. Thus, a relatively smaller square can be embedded into the VTC lobe which reduces its stability. The read SNM of the CS-SRAM cell is also better than the others. As the 6T-SRAM cell does not have any stability improvement technique, it offers a low SNM value. Since the functionality of NC-SRAM cell is similar to that of 6T-SRAM cell during read operation, so its read SNM is also similar to that of 6T-SRAM cell. The IWLVC-SRAM cell uses a PMOS in its word line path which weakens the access transistor, so its SNM is slightly better than that of the NC-SRAM cell. The use of optimum cs-n and cs-p value estimated in Sect. 3.1 maximizes the read SNM of the CS-SRAM cell.

The read and retention stability are also measured, for the compared cells designed using 20 nm technology FinFETs and shown in Fig. 13. It is found that the stability enhancement of the proposed method remains intact in the 20 nm FinFET technology also. The read and retention SNM of the compared cells are presented in Table 4.

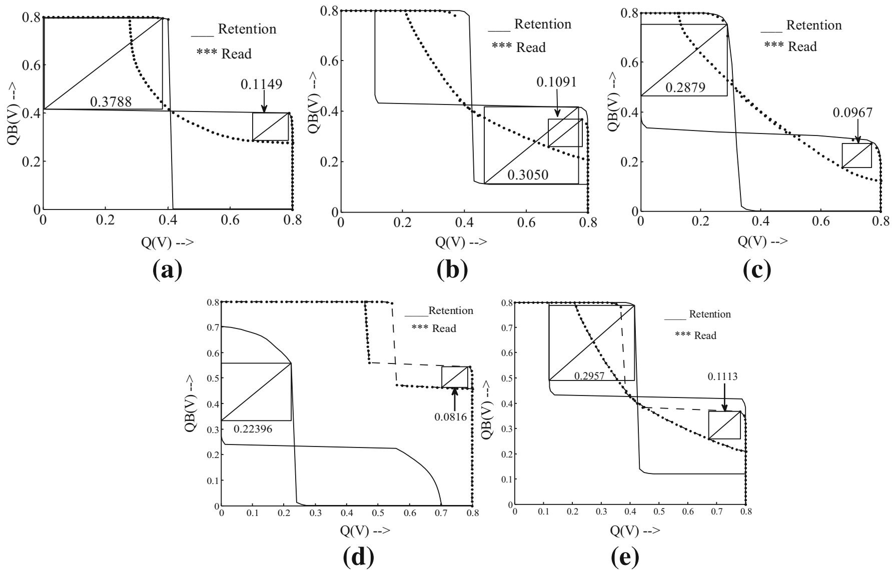


Fig. 13 The read and retention SNM of the compared SRAM cells designed using 20 nm FinFET technology **a** CS-SRAM cell **b** NC-SRAM cell **c** 6T-SRAM cell **d** 10T-SRAM cell **e** IWLVC-SRAM cell

Table 4 Stability comparison matrix

Technology	SRAM cells	Stability	
		Retention SNM (mV)	Read SNM (mV)
CMOS (90nm)	This work	348.5	123.5
	NC-SRAM [3]	275.5	102.9
	6T-SRAM	246.2	93.8
	10T-SRAM [16]	202.9	74.9
	IWLVC-SRAM [18]	275.8	116.5
FinFET (20nm)	This work	378.8	114.9
	NC-SRAM [3]	305.0	109.1
	6T-SRAM	287.9	96.7
	10T-SRAM [16]	223.9	81.6
	IWLVC-SRAM [18]	295.7	111.3

A systematic fluctuation of oxide-thickness, doping concentration, and oxide-capacitance leads to threshold voltage fluctuation which changes the device characteristic [14, 19]. This can deteriorate the noise margin of the SRAM cell. A statistical analysis is performed using a Monte Carlo simulation to know the stability variation which results from the fluctuation of V_{th}, channel length (L) and channel width (W) as a result of process variation. Assuming the threshold voltage to distribute in a Gaussian manner having 3σ variation of 10 % from the nominal value, the Monte Carlo simulation is performed with 500 instances of simulations. From this the worst

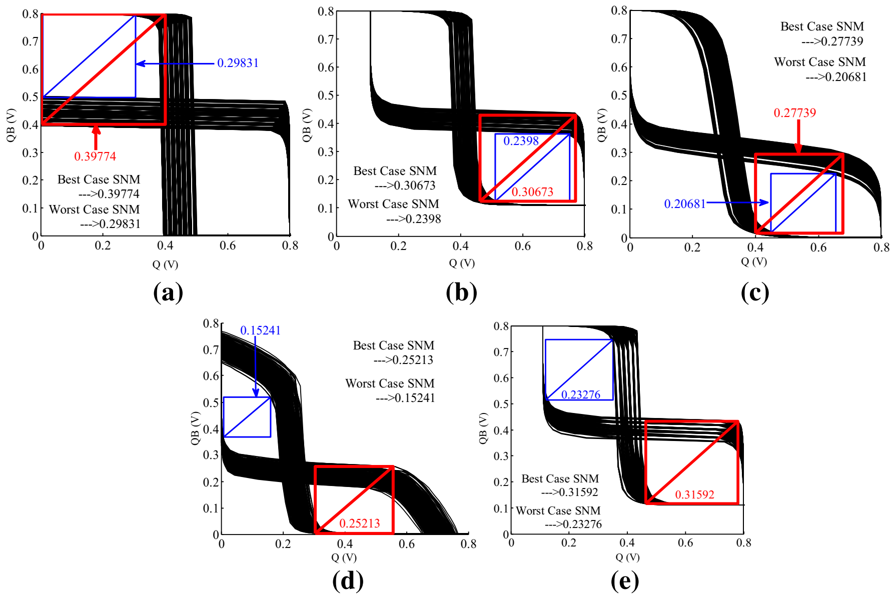


Fig. 14 The best and worst case retention SNM during Monte Carlo simulation **a** CS-SRAM cell **b** NC-SRAM cell **c** 6T-SRAM cell **d** 10T-SRAM cell **e** IWLVC-SRAM cell

and best case SNM are measured and shown in Figs. 14 and 15, respectively. The statistical distribution of the read SNM and retention SNM of the discussed cells is shown in Fig. 16a, b, respectively. It shows that the mean retention SNM of CS-SRAM, NC-SRAM, 6T-SRAM, 10T-SRAM and IWLVC-SRAM cell is 347, 273, 246, 200.3 and 265 mV, respectively, with standard deviation of 20.40, 12.05, 10.50, 13.56 and 39.1 mV, respectively. So, the mean retention SNM of CS-SRAM increases by 41.05 % from that of 6T -SRAM cell. Similarly, the mean read SNM of CS-SRAM, NC-SRAM, 6T-SRAM, 10T-SRAM and IWLVC-SRAM cell is 134, 118, 91.9, 89.1 and 115 mV, respectively, with standard deviation of 27.40, 24.10, 19.4, 20.2 and 24.3 mV, respectively. The read SNM of CS-SRAM is increased by 45.5 % from that of 6T-SRAM cell.

To observe how the stability enhancement of the proposed cell is affected at the different process corners, temperature and supply voltage variation, the read and retention SNM of the compared cells is also measured in different PVT condition and depicted in Figs. 17 and 18, respectively. The peripheral circuits are also taken into consideration during PVT analysis. It shows that both the read SNM and retention SNM of the proposed cell are significantly higher than the other compared cells in all PVT conditions.

4.3 Performance Enhancement in Terms of Write Margin

Write SNM is a well-known parameter to measure the write ability of a SRAM cell. A SRAM cell with higher WSNM is highly writable [24]. To check the write ability of the compared cells, their write SNM are measured and depicted in Fig. 19a–e. The write

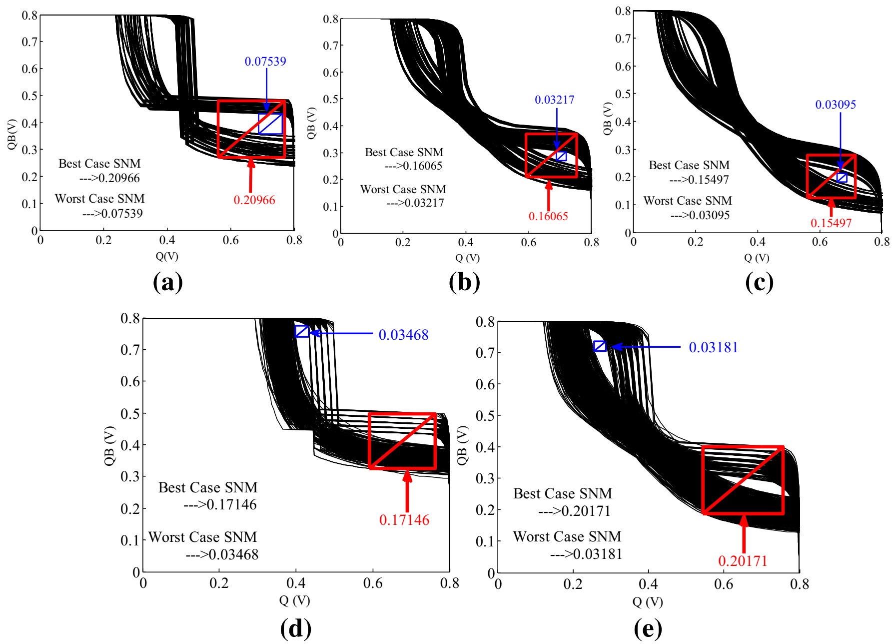


Fig. 15 The best and worst case read SNM during Monte Carlo simulation **a** CS-SRAM cell **b** NC-SRAM cell **c** 6T-SRAM cell **d** 10T-SRAM cell **e** IWLVC-SRAM cell

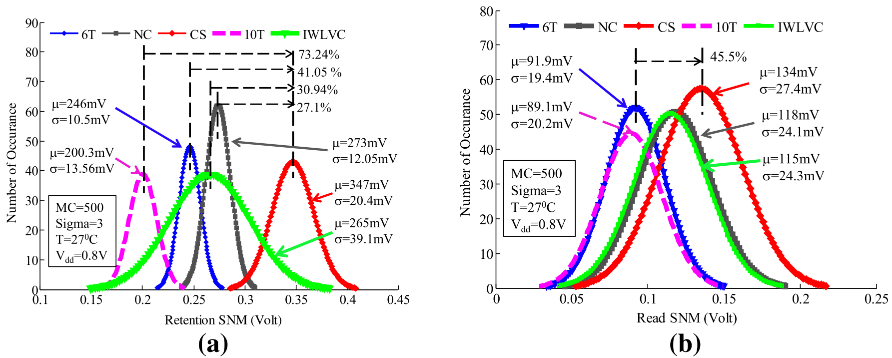


Fig. 16 Statistical distribution of **a** Retention SNM **b** read SNM of the compared SRAM cells designed using 90 nm technology

SNM of the CS-SRAM cell is 392.5 mV, whereas that of NC-SRAM, 6T-SRAM, 10T-SRAM and IWLVC-SRAM cell is 341.5, 297.7, 384.1 and 324.59 mV, respectively. The write ability of the proposed CS-SRAM cell is 31.8 % more than that of 6T-SRAM cell. The reason can be explained as below.

Had it been a conventional 6T-SRAM cell, the 'X' node (Fig. 1) would be fixed at V_{DD}. So the 'Q' node would have got a strong supply from the 'X' node. But in the proposed CS-SRAM cell the 'X' node voltage gets a dip during write operation which is shown in Fig. 6. Hence, during write operation, the 'Q' node does not get a very

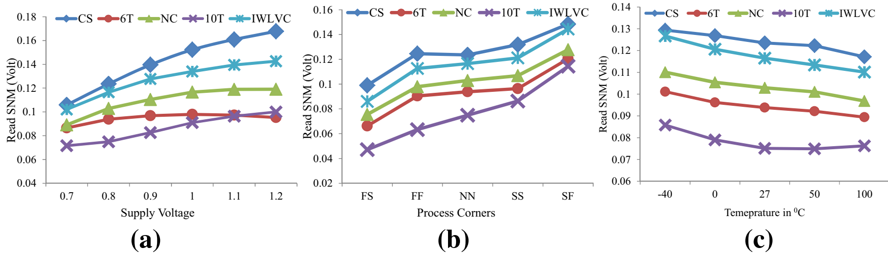


Fig. 17 Read SNM of different SRAM cells (CMOS 90 nm technology) at different **a** supply voltages **b** process corners **c** temperatures

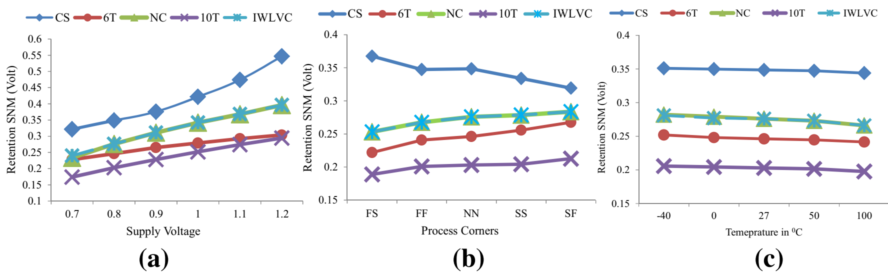


Fig. 18 Retention SNM of different SRAM cells (CMOS 90 nm technology) at different **a** supply voltages **b** process corners **c** temperatures

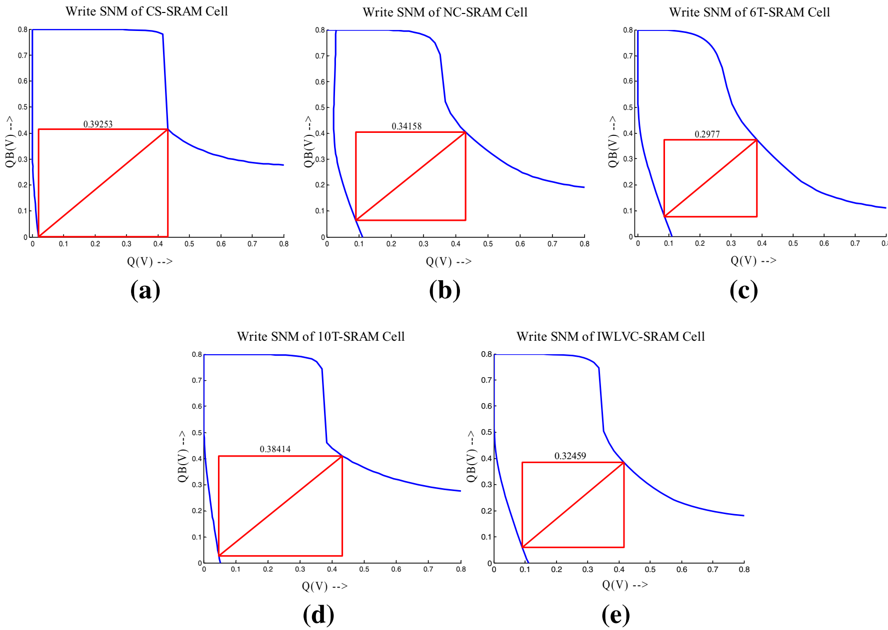


Fig. 19 The WSNM of the SRAM cells under comparison designed using 90 nm CMOS technology **a** CS-SRAM cell **b** NC-SRAM cell **c** 6T-SRAM cell **d** 10T-SRAM cell **e** IWLVC-SRAM cell

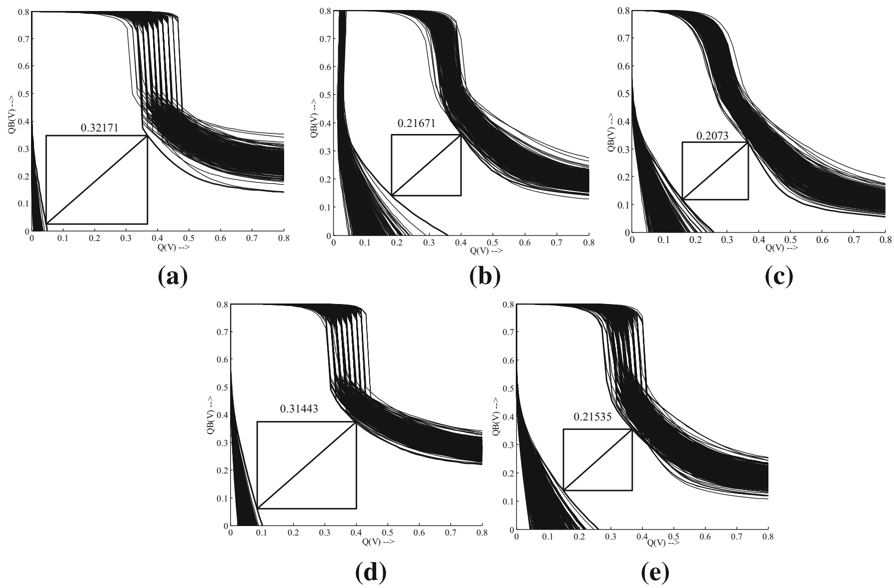


Fig. 20 The WSNM of the cells under comparison, designed using 90 nm CMOS technology under process variation **a** CS-SRAM cell **b** NC-SRAM cell **c** 6T-SRAM cell **d** 10T-SRAM cell **e** IWLVC-SRAM cell

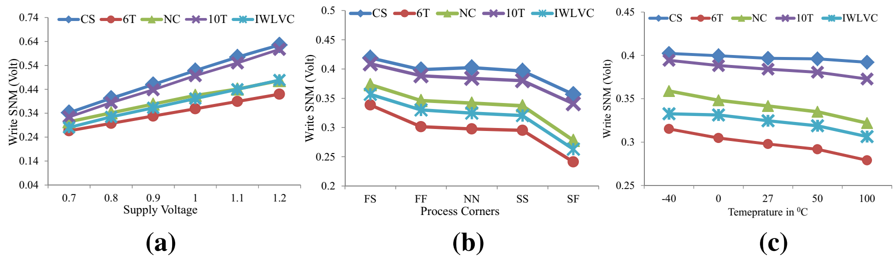


Fig. 21 Write SNM of different SRAM cells (CMOS 90 nm technology) at different **a** supply voltage **b** process corner **c** temperature

strong supply from 'X' node compare to the case of 6T-SRAM cell. Hence, 'Q' node can discharge quickly. As a result, the write ability of the CS-SRAM cell increases with respect to 6T-SRAM cell.

To know how the write ability is affected under process variation, we have also estimated the write SNM of the cells under comparison using Monte Carlo analysis and shown in Fig. 20. It is found that the write SNM of the proposed cell is better than the other cells also under process variation.

To observe how the write ability of the proposed cell is affected at the different process corners, temperature and supply voltage variation, write SNM of the cells is also measured in different PVT condition and depicted in Fig. 21. It shows that the write SNM of the proposed cell is better than the other cells under comparison in all PVT conditions

4.4 Speed Comparison

The speed of operation of the compared cells is analyzed by measuring the read and write speed. The delay between 50 % of WL and the 50 % of rising QB is taken as the delay for write ‘0’ operation. Figure 22 shows the measurement of delay during a 0-write. Similarly, the delay for write ‘1’ is also calculated. The read ‘0’ and read ‘1’ delays are calculated by measuring the time taken by ‘BL’ and ‘BLB,’ respectively, to discharge by 20 % of the supply voltage. The delay analysis is carried out for the SRAM cells designed using 90 nm CMOS technology library. It is found that the read delay of the proposed scheme is better than all the other cells under comparison except the 6T-SRAM cell. Table 5 states the write and read delays of the compared SRAM cells. The read delay of the 6T-SRAM cell is the least. This is due to its simple structure having only two transistors in its read path. Since the proposed cell has one extra transistor in its read path, it increases the read delay than the 6T-SRAM cell which is considered as a tradeoff to achieve the significant advantages in terms of energy and stability. However, the delay of the proposed CS-SRAM cell is less in comparison with the NC-SRAM, IWLVC-SRAM cell and the 10T-SRAM cell. This

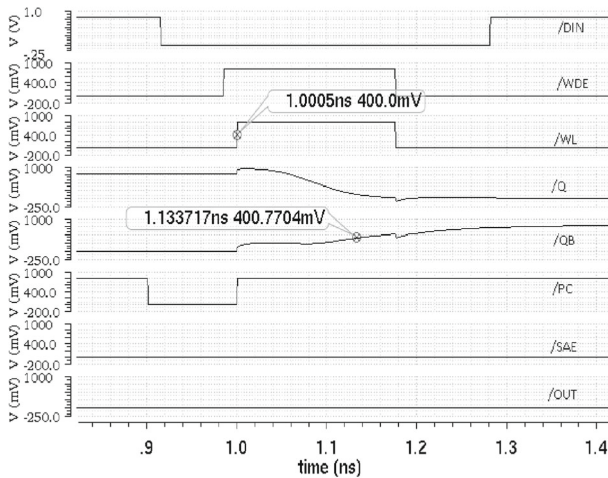


Fig. 22 Setup for calculating delay during writing a ’0’ to the CS-SRAM cell

Table 5 Write and read delays of SRAM Cells (CMOS 90 nm technology) in ps

SRAM cells	Operations			
	0-Write	0-Read	1-Write	1-Read
This work	133.21	68.77	123.30	65.92
NC-SRAM [3]	127.43	71.27	116.35	69.40
10T-SRAM [16]	136.13	119.92	136.28	115.61
IWLVC-SRAM [18]	144.45	81.81	139.46	79.75
6T-SRAM	137.52	53.82	135.52	52.61

Fig. 23 Physical layout of **a** 6T-SRAM cell **b** NC-SRAM cell **c** CS-SRAM cell **d** IWLVC-SRAM cell **e** 10T-SRAM cell

is because though the NC-SRAM cell uses three transistors in its read path, it uses a high V_{th} access transistor which increases its read delay than the CS-SRAM cell. In IWLVC-SRAM cell, the insertion of PMOS in the word line weakens further the read path. Thus, the delay increases further. In the 10T-SRAM cell, the read path consists of four transistors which increase its delays even more. The write delays of all the cells are almost similar. The write delay of the proposed cell is slightly greater than the NC-SRAM cell but it is smaller than that of the other three cells under comparison.

4.5 Physical Considerations of the Proposed Cell-Based Array

Using 90 nm CMOS technology, physical layout of the cell arrays with proposed CS-SRAM cell, and the other SRAM cells under comparison are designed. The cells are

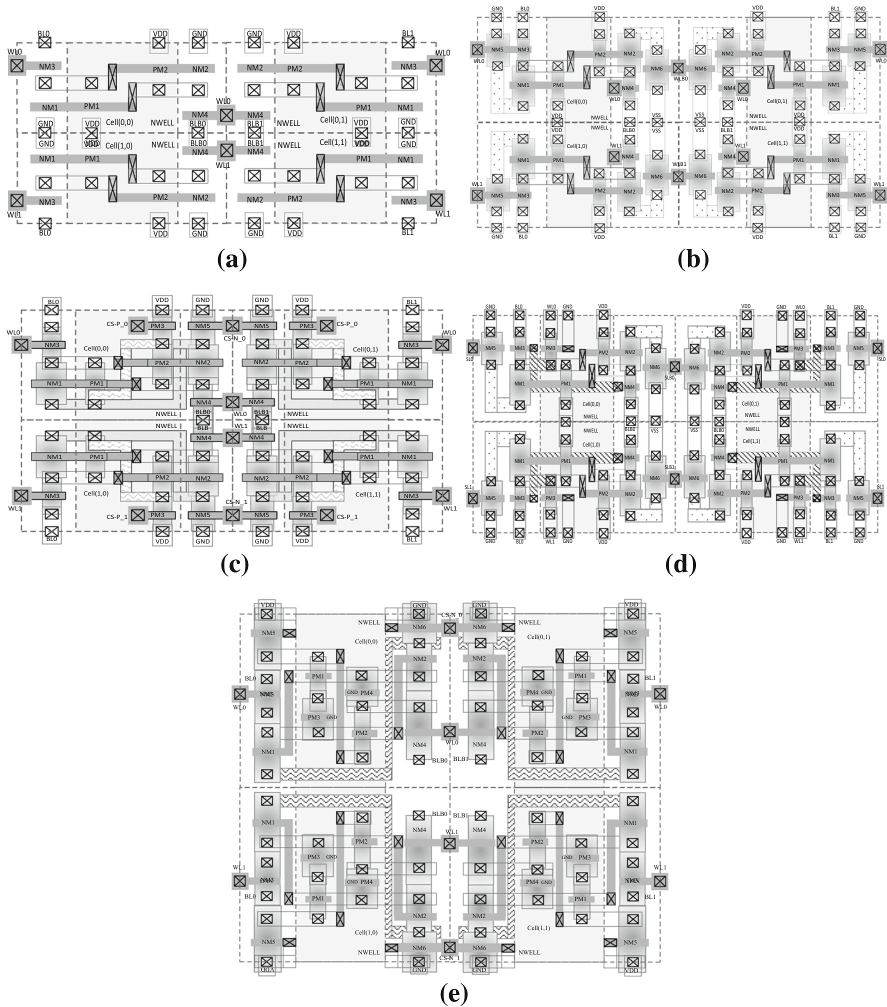


Fig. 24 Architecture of array of **a** 6T-SRAM cell **b** NC-SRAM cell **c** CS-SRAM cell **d** IWLVC-SRAM cell **e** 10T-SRAM cell

designed with utmost care to make it symmetric and compact. It uses an industry standard one directional poly-silicon layer concept [7,12,13,25]. The array of the SRAM cells is designed such that the neighboring cells share the BL, BLB, VDD, GND nodes among each other wherever possible. The physical layout of the 6T-SRAM cell, NC-SRAM cell, CS-SRAM cell, IWLVC-SRAM cell and 10T-SRAM cell is shown in Fig. 23a–e, respectively. A portion of the array, designed using these SRAM cells, is shown in Fig. 24.

From Fig. 24a, it can be found that the cell(1,0) is flipped vertically so that cell(1,0) and cell(0,0) can share the same VDD, GND and BLB node. It is also found that the cell(0,1) is flipped horizontally and it shares its WL node with the cell(0,0). In the

similar manner, all the consecutive cells share the nodes with their neighboring cells. The 17 % increment of the proposed CS-SRAM cell in comparison with the 6T-SRAM cell is well justified by the overwhelming improvement in its stability, write ability and energy consumption. However, the area consumption of the proposed cell is less by 25, 47, 61% than that of the NC-SRAM cell, IWLVC-SRAM cell and 10T-SRAM cell, respectively.

5 Conclusion

The proposed current starving SRAM cell and its array is implemented using gpdk-90 nm CMOS technology library. Its stability, energy consumption and delay are compared with that of NC-SRAM, 10T-SRAM, IWLVC-SRAM and the conventional 6T-SRAM cell. The proposed scheme increases cell stability by making the VTC of the cross-coupled inverter pair more ideal in nature. It reduces the dynamic energy consumption of the cell by reducing its short circuit current during state transition. The retention and read stability in proposed current starving scheme increases by 41 and 31%, respectively, with respect to 6T-RAM cell. These two SNM are also much better than the other SRAM cells under comparison. The proposed scheme consumes 22% lesser energy in comparison with 6T-SRAM cell. The write ability of the proposed cell is 31% higher than that of the 6T-SRAM cell. The stability enhancement, energy reduction and higher write ability could be achieved at a cost of 17% more physical area of the proposed SRAM cell. The performance enhancement of the proposed technique is also validated for a miniaturized device size, using 20 nm FinFET technology. The enhancement in circuit performance remains intact in 20 nm FinFET design.

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