

# The Investigation and Optimisation of Phase-Induced Amplitude Attenuation in the Injection-Locked Ring Oscillators-Based Receiver

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**Abstract** In this paper, the injection-locked oscillator (ILO)-based receiver is investigated. The key design considerations of the ILO including the phase difference between the input and output signals and its impact on the ILO-based receiver are analysed in detail. Different strategies for both the narrow and wide-band applications are discussed and simulated. As a design example, a 2.4 GHz ILO-based receiver is implemented using a standard 40 nm CMOS technology, where a three-stage inverter-based ILO is optimised to maintain a good balance among working range, sensitivity and power consumption, etc. Measurement results show that the proposed receiver is able to demodulate an input signal at a 2.4 GHz carrier frequency with the data rate up to 1 Mbps while consuming  $<300 \mu\text{W}$  power. It is suitable for short-range communication system such as chip-scale data link.

**Keywords** Injection locking · Nano-scale CMOS · OOK receiver

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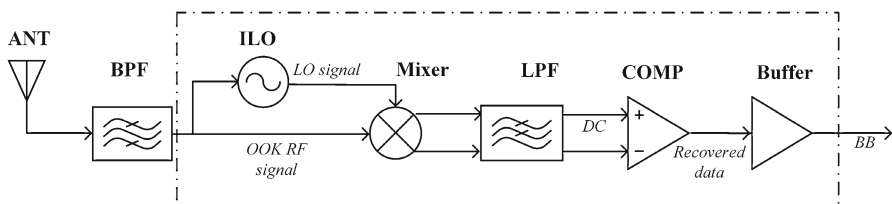
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## 1 Introduction

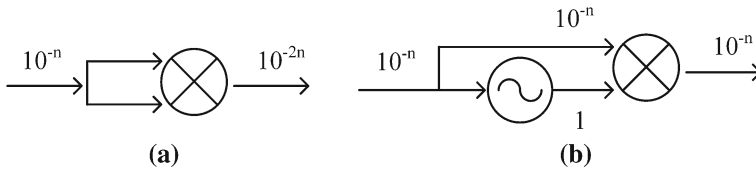
The wireless communication has been experiencing a tremendous progress in recent decades. As one of the key building blocks in such a system, low-cost CMOS radio-frequency (RF) receivers with low power consumption and small silicon area are always highly desired [1, 3, 4, 6, 8, 10, 12, 15, 16]. The ILO-based receiver has been celebrated as a promising candidate where energy efficiency is the key consideration [9, 14]. Conventionally, a low power receiver is achievable by using an oscillator-less topology where the input RF signal is amplified and demodulated with a low-noise amplifier followed by an envelope detector [17]. However, to obtain a better sensitivity, a phase-locked loop (PLL)-based local oscillator is preferred although the PLL is one of the most power-consuming blocks in the whole receiver. As shown in Fig. 1, an ILO-based receiver makes it possible to eliminate power-consuming PLL or low-noise amplifier (LNA) where the ILO is used to track the input carrier frequency and generate a considerably large output signal level. To maintain an ultra-low power consumption, many reported receivers are based on a single RF path without I/Q signals. In such architecture, however, the phase difference between RF signal and oscillator's output signal may significantly degrade the amplitude of the output IF signal, and deteriorate the SNR of the receiver consequently. This makes the ILO-based receiver less attractive. Based on this requirement, this paper investigates the key design issues including the working range, phase shifts in the ILO-based receiver. Then, the optimization from circuit to systems level is carried out, followed by the silicon verification of a 2.4 GHz receiver implemented using a standard 40 nm CMOS technology. Measurement results suggest that it is possible to obtain a good balance among all these design considerations based on certain system requirements.

## 2 Design Considerations

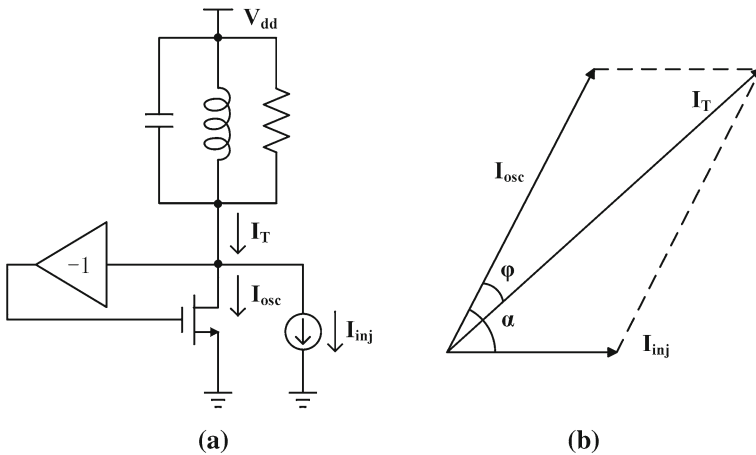
The comparison between the ILO-based receiver and conventional self-demodulator has been carried out in [10]. As shown in Fig. 2, for an input signal level of  $10^{-n}$  (e.g. antenna impedance of 50 Ohm, input power of  $-60$  dBm), the envelope detection or self-demodulation, as shown in Fig. 2a, the mixer produces an output power of  $10^{-2n}$ . As shown in Fig. 2b, by using an injection-locked oscillator, which tracks the envelope of input RF signal and generates an output signal locked to carrier frequency, the output of the mixer is now in the order of  $10^{-n}$ . Thanks to this enhanced ILO's output, the sensitivity is significantly improved.



**Fig. 1** Architecture of the proposed receiver



**Fig. 2** Model of self-demodulation and injection-locked oscillator-based demodulation



**Fig. 3** **a** Model of an injection-locked oscillator, **b** phasor representation of the injected and resulted currents

The first key consideration of the ILO-based receiver is the working range which is mainly limited by the oscillator. The ILO is only able to track the input signal within a certain frequency range. When the input frequency is out of the locking range, it may only generate a fixed output frequency. This locking range determines the total working range of the receiver, which should be properly planned in a communication system. Moreover, even the ILO is locked to the input signal, phase shifts between the input and output of the ILO still exist. The IF signal (output of the mixer) may be degraded considerably, or even be cancelled out. The optimisation of this phase shift is therefore highly desired in the single-path ILO receiver.

These two design considerations can be analysed theoretically. The model of an injection-locked oscillator is shown in Fig. 3a, where an oscillator has a self-resonant frequency of  $\omega_0$  and an oscillating current of  $I_{osc}$ . Due to the external injection current,  $I_{inj}$ , the oscillator is locked at  $\omega_1$ . A phasor representation of currents is shown in Fig. 3b, where  $\alpha$  is the phase difference between injected and oscillating current and  $\varphi$  represents the phase shift.

From the consideration of data rate, a wide bandwidth is usually preferred. It is therefore of great importance to discuss the way to extend the locking range of the oscillator, which determines the working range of an ILO-based receiver. Simultaneously, other considerations such as the phase shift of ILO, sensitivity, etc., should be taken into account. Since the target working frequency of this work is at GHz, which is

suitable at this range, the ring oscillator core is discussed in this work. In an injection-locked ring oscillator, according to [2], the locking range is directly proportional to the injection current amplitude, and it is inversely proportional to the amplitude of ring oscillator's output voltage. It suggests the possibility to achieve a wider locking range only if the injected signal is enhanced.

In such an injection system, a phase shift always exists between the input and output of the oscillator. The locking range and first-harmonic injection locking as well as phase noise in CMOS ring oscillators are analysed and discussed in [10, 11]. It is assumed that the phase change is linear to the shift of operating frequency, which can be expressed as

$$\frac{d\varphi}{d\omega} = A \quad (1)$$

where  $A$  is a constant, we have

$$\varphi = A (\omega - \omega_0) \quad (2)$$

Therefore,

$$\Delta\omega = \frac{d\alpha}{dt} = \omega - \omega_1 \quad (3)$$

By applying the Law of Sines, we obtain

$$\varphi \approx \sin \varphi = -\frac{I_{inj}}{I_T} \cdot \sin \alpha \approx -\frac{I_{inj}}{I_{osc}} \cdot \sin \alpha \quad (4)$$

Therefore,

$$\varphi = A (\omega - \omega_0) = A [(\omega - \omega_1) - (\omega_0 - \omega_1)] = A (\Delta\omega - \Delta\omega_0) \quad (5)$$

From (4) and (5), we have

$$-\frac{I_{inj}}{I_{osc}} \cdot \sin \alpha = A (\Delta\omega - \Delta\omega_0) = A \left( \frac{d\alpha}{dt} - \Delta\omega_0 \right) \quad (6)$$

Assume

$$B = \frac{I_{inj}}{A \cdot I_{osc}} \quad (7)$$

From (6), we have

$$\frac{d\alpha}{dt} = -B \cdot \sin \alpha + \Delta\omega_0 = \omega - \omega_1 \quad (8)$$

$$-B \cdot \sin \alpha = \omega - \omega_1 - \Delta\omega_0 = \omega - \omega_1 - \omega_0 + \omega_1 = \omega - \omega_0 \quad (9)$$

Therefore,

$$\omega = -B \cdot \sin \alpha + \omega_0 = -\frac{I_{inj}}{A \cdot I_{osc}} \cdot \sin \alpha + \omega_0 \quad (10)$$

Finally, it is obtained as

$$\omega - \omega_0 = -\frac{I_{inj}}{A \cdot I_{osc}} \cdot \sin \alpha \quad (11)$$

For a single tuned circuit,

$$\tan \varphi = \frac{\omega - \omega_0}{\omega_0} \cdot 2Q \quad (12)$$

For a small angle,

$$\varphi \approx \tan \varphi = \frac{\omega - \omega_0}{\omega_0} \cdot 2Q \quad (13)$$

Therefore,

$$A = \frac{d\varphi}{d\omega} = \frac{2Q}{\omega_0} \quad (14)$$

$$B = \frac{\omega_0 \cdot I_{inj}}{2Q \cdot I_{osc}} \quad (15)$$

Finally, it is obtained as

$$\frac{d\alpha}{dt} = -\frac{\omega_0 \cdot I_{inj}}{2Q \cdot I_{osc}} \cdot \sin \alpha + \Delta\omega_0 \quad (16)$$

When the oscillator works at  $\omega_1$ ,

$$\Delta\omega = \omega - \omega_1 = 0 \quad (17)$$

In this case,  $\frac{d\alpha}{dt} = 0$ , therefore,

$$\sin \alpha = 2Q \cdot \frac{\Delta\omega_0 \cdot I_{osc}}{\omega_0 \cdot I_{inj}} \quad (18)$$

$$\varphi = A(\omega - \omega_0) = A(\omega_1 - \omega_0) = -A \cdot \Delta\omega_0 = -\frac{2Q \cdot \Delta\omega_0}{\omega_0} \quad (19)$$

So the phase difference between the input and output of the oscillator can be expressed as

$$\beta = \alpha - \varphi \approx \alpha \quad (20)$$

From these equations, there is a phase difference between the input and output of the oscillator, which consequently impacts the amplitude of the output of the mixer. This varies at different frequency shift, oscillating current, injection current, and quality factor of the oscillator, which are closely related with circuit parameters.

### 3 Optimisation of the ILO Receiver

The optimisation of the ILO-based receiver has been important topic in literatures. To achieve a low-voltage operation, an AC-coupled ILO that generates four quarter-rate clock phases is used in the receiver [9]. By using an automatic frequency control

module to adjust the centre frequency of the oscillator, a frequency-sweeping injection-locked oscillator is realised in a self-demodulator [10]. To enhance the sub-harmonic injection strength, an 8<sup>th</sup> sub-harmonic injection-locked oscillator (SILO) is used in the receiver for mm-wave beamforming applications [14]. In these receivers, the key considerations such as the phase shift have not been considered from a system perspective. Especially considering the emerging nano-scale CMOS technology as well as the low-power short-range communications, it is necessary to investigate a new design strategy such as the designs based on ring oscillator-based ILO.

From the above-mentioned general theory of injection locking, the locking range and phase shift are heavily dependent on circuit parameters. So it is necessary to conclude a design strategy based on a certain circuit topology. LC oscillator is widely used in wireless communications for its high operating frequency and excellent phase noise performance. However, LC tank at GHz ranges means a large silicon area, which makes it less suitable for large-scale integration. In this work, for example, with regarding to the wide implementation of nano-scale CMOS, which is able to work at GHz range with low power consumption in nowadays RF system, the ring-oscillator-based ILO is used.

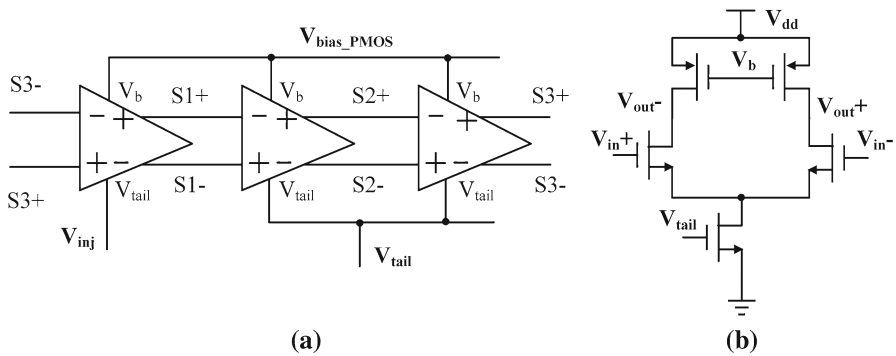
Figure 4 shows the topology of the ILO, which contains three stages of differential inverters. For high-speed inverters, the power dissipation is dominated by the dynamic dissipation resulting from charging and discharging of capacitances. In typical CMOS circuits, the dynamic dissipation  $P_{\text{dyn}}$  is given by [13]:

$$P_{\text{dyn}} = C_L V_{\text{DD}}^2 f_{0 \rightarrow 1} \quad (21)$$

$f_{0 \rightarrow 1}$  represents the frequency of energy-consuming transitions,  $C_L$  represents the total loading capacitance,  $V_{\text{DD}}$  represents the supply voltage. The power consumption of inverters in this work mainly depends on the sizes of the transistors. The design strategy of power consumption in the ring oscillator is to use smaller transistor sizes as long as the other performances can be reached.

The equivalent resistance of the load PMOS is tunable by the biasing voltage,  $V_{\text{bias\_PMOS}}$ . The input signal is injected to the ring oscillator through the tail transistor of the first stage. By properly sizing of the transistors and optimising the biasing condition, the oscillator is able to operate at a wide range with a low power consumption. The adjustable parameters include the W/L of tail NMOS, NMOS, and PMOS transistors in the inverter, the biasing voltage of the tail NMOS and loading PMOS transistors. The ILO, designed using a standard 40 nm CMOS technology, is able to cover certain work range defined by the communication systems, e.g. 2.4 GHz ISM band. The optimisation of the ILO is carried out as follows.

Step1: Determine the self-resonant frequency of the oscillator,  $f_0$ . Firstly, the size of transistor should be adjusted to meet this basic requirement. To ensure a smaller area and lower power consumption, the channel length of all the transistors (L) in Fig. 4b should be the smallest, such as 40 nm in this case. The power consumption and self-resonant frequency are mainly determined by the tail transistor. As the W/L of the tail transistor decreases, the power consumption reduces, and the self-resonant frequency varies. It is possible to find an optimised transistor size when the target operating frequency is reached, while the power consumption is minimised.



**Fig. 4** Topology of the ILO (a) and top view (b) the cell

Secondly, it is necessary to find the total working range of the oscillator to cover the entire operating frequencies of the receiver. In this work, without applying an input RF signal, we should firstly set a proper DC biasing voltage for the NMOS transistor, e.g. 0.6 V, then sweep the biasing voltage of for PMOS. At the working range of 0.5–0.7 V, e.g. the oscillator has an output frequency ranges from 3.4 to 0.23 GHz in simulation. In this design, when the DC biasing voltage of NMOS transistor decreases, power consumption of the ILO can be further reduced.

After the optimisation of the loading of the inverter, the working condition of the NMOS tail transistor can be properly adjusted. Without applying an input RF signal, set a proper biasing voltage for the PMOS, e.g. 0.6 V, then sweep the DC biasing voltage of NMOS transistor. In the suitable biasing range of 0.4–0.8 V, the oscillator has an output frequency range from 1.29 to 0.89 GHz with an output amplitude range from 0.24 to 0.91 V. The simulated output frequencies and amplitudes of the oscillator under these conditions are summarised in Fig. 5, which indicates the major functionality of the NMOS biasing voltage is the control of the output amplitude, instead of the operating frequency. The output frequency doesn't change considerably versus the DC biasing of NMOS biasing condition.

These simulations suggest that the target operating frequency of the oscillator can be reached by proper sizing of transistor and adjusting of DC biasing voltage.

Step2: Optimise the total operating range (locking range) of the oscillator. The biasing voltage of PMOS is mainly determined by the target operating frequency as mentioned above. The locking range is mainly reached by the optimisation of biasing voltage and device size of the NMOS transistor. The target operating frequency of the oscillator is regarded as a prior consideration when optimising the size of transistor. Then, the W/L of the NMOS transistor can be properly reduced to acquire lower consumption. The biasing of the NMOS transistor should be optimised as follows: If a large biasing current of the NMOS transistor is applied, the oscillator becomes less sensible to the injected current. Otherwise, the oscillator is more sensible to the injection current, which is preferred for frequency tuning. This indicates a balance between the locking range and sensitivity of input signal is possible. The ILO designed to have a very wide range may exhibit a lower sensitivity. This can be verified in simulations among different combinations of MOS transistors and biasing condition.

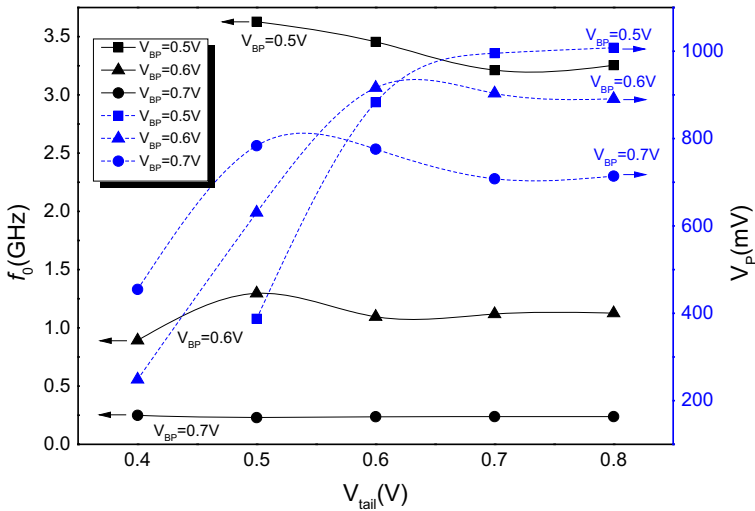


Fig. 5 Output frequency and amplitude when  $V_{BP} = 0.5, 0.6$  and  $0.7$

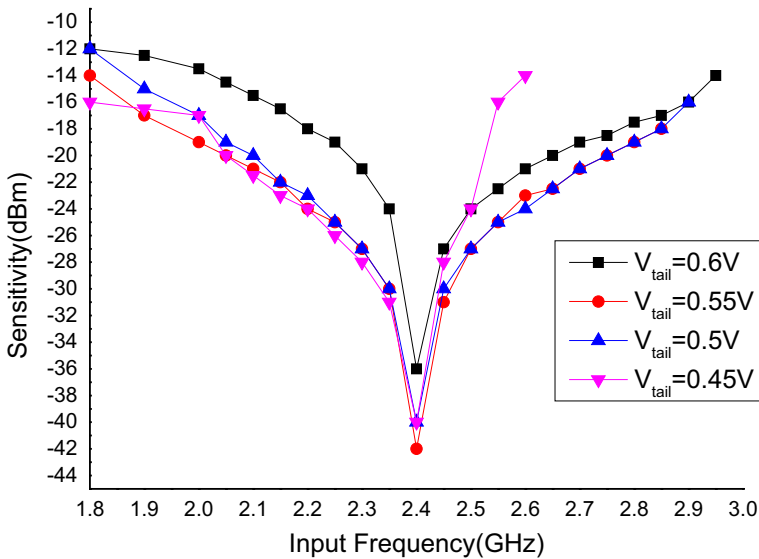


Fig. 6 Input sensitivity versus input frequency at different  $V_{tail}$

In this work, for example, we can set the target operating frequency, e.g. 2.4 GHz, then sweep the tail biasing voltage. At the working range of 0.45–0.6 V, the simulated power consumption increases from 0.042 to 0.121 mW. The simulated sensitivity and locking range are shown in Fig. 6.

When  $V_{tail}$  is set to be 0.6 V, a maximum locking frequency of 2.95 GHz is achieved but with the poorest sensitivity of  $-36$  dBm. When  $V_{tail}$  is set to be 0.55 V, there is a good sensitivity of  $-42$  dBm with a maximum locking range of 2.85 GHz, which

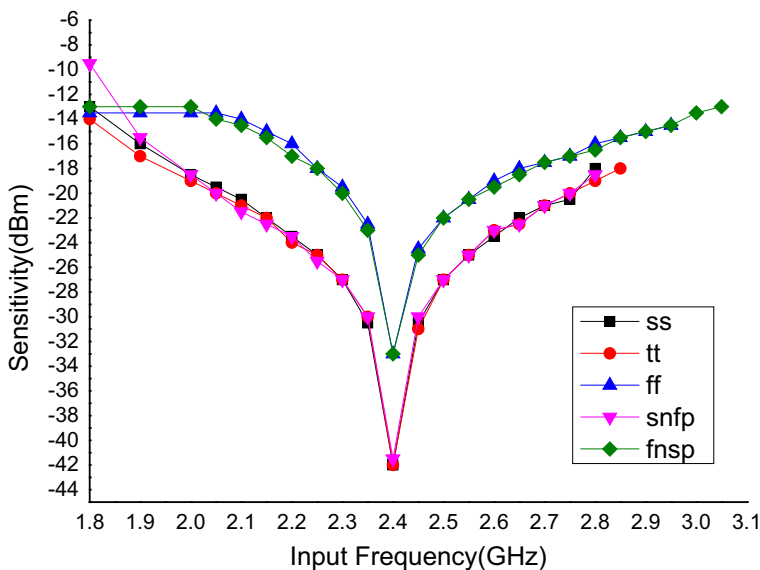


maintains a good balance between sensitivity and locking range. The simulations are based on the typical process corner. The optimised biasing conditions may vary subject to different process corners. More simulated results under process corners are shown in Fig. 7 when  $V_{\text{tail}}$  is set to be 0.55 V. Under corner ff and fnsp, the simulated results show good locking range and poor sensitivity, while the simulated results under corner ss, tt and snfp show better sensitivity but smaller locking range.

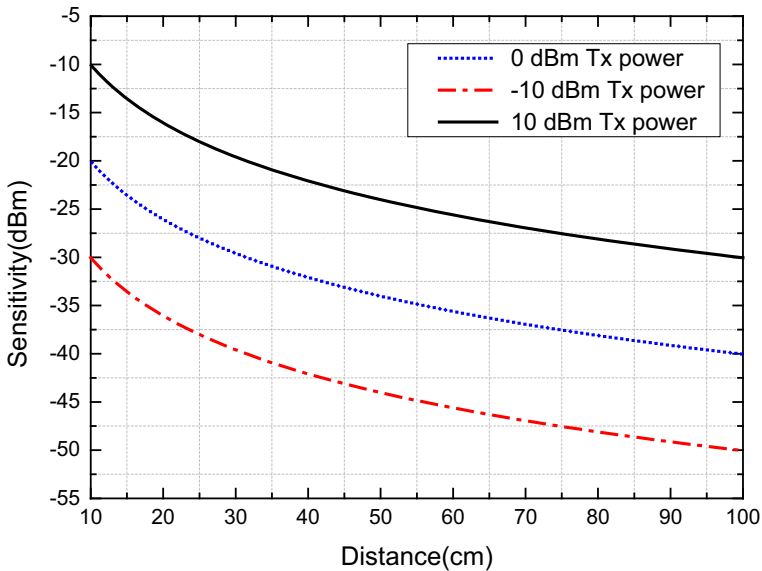
The design consideration of sensitivity is subject to different applications. For short-range low-power applications such as wireless sensor networks or RFID, the required sensitivity of receivers is less stringent [4]. For example, a narrowband wireless transmission with a 2 GHz carrier frequency incurs only about 40dB path loss for a one metre link distance. The range of the wireless link determines the path loss, which together with the transmit power sets the required sensitivity of the receiver according to [7]:

$$\text{Sens}_{\text{RX}} = P_{\text{TX,out}} - 20 \log_{10} \left( \frac{4\pi d}{\lambda} \right) \quad (22)$$

Where  $P_{\text{TX,out}}$  is the output power of the transmitter,  $d$  is the distance of communication,  $\lambda$  is the wave length of the carrier. For a carrier frequency of 2.4 GHz, Fig. 8 shows the requirement of sensitivities in such a system. In this work, the receiver is designed to have a sensitivity of  $-40$  dBm, which is suitable for short-range applications. For the application of other applications such as sub-GHz wireless metering, Bluetooth, etc., a better sensitivity of  $-80$  dBm may be required. The ILO with LC tank or a low-noise amplifier (pre-amplify the RF signals) is hence needed, at the expense of additional silicon area and power consumption.



**Fig. 7** Input sensitivity versus input frequency at different process corners

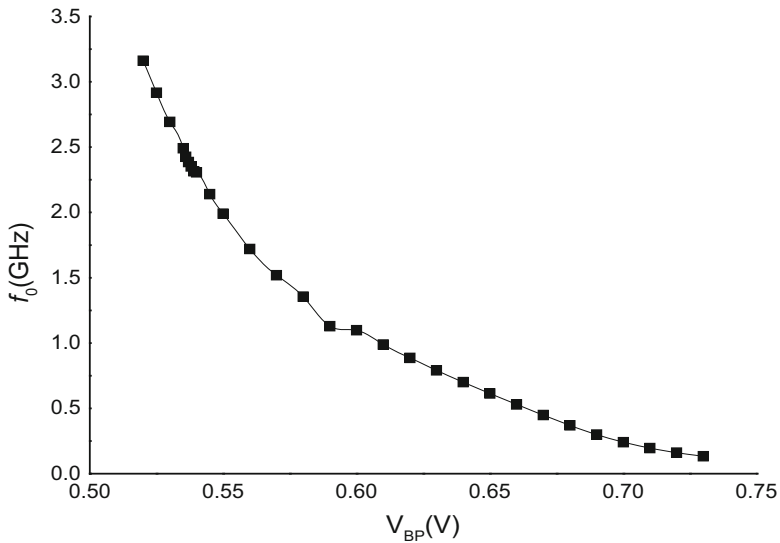


**Fig. 8** Required receiver sensitivity versus communication range

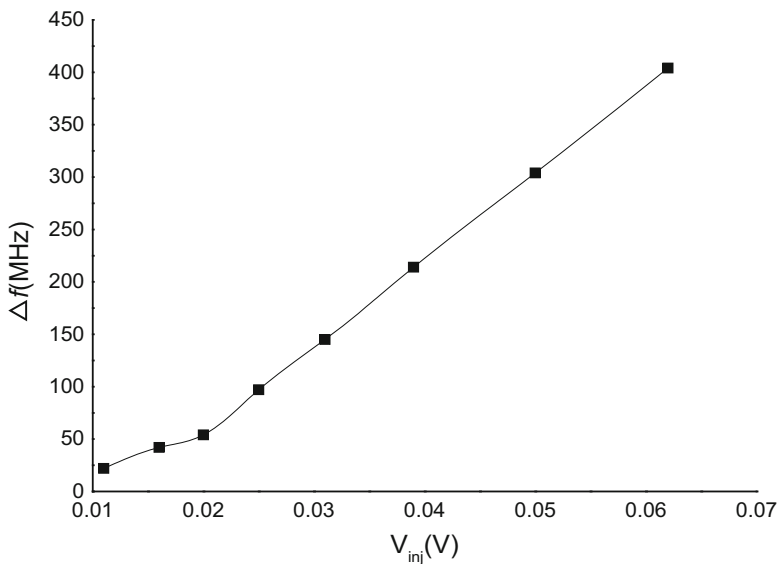
After considering all these factors, the suitable tail biasing voltage should be 0.5–0.55 V to maintain a good balance between locking range and sensitivity. Here the tail biasing voltage can be 0.45 V mainly considering the low power consumption as well as the good sensitivity and proper locking range. If a larger locking range is required, the biasing voltage should be adjusted accordingly. The self-resonant frequency versus PMOS biasing voltage is shown in Fig. 9 at this NMOS biasing condition. Compared with [1, 4–6, 12], the proposed work is able to cover most of the GHz and sub-GHz communications and it can be tuned to other operating frequency ranges by properly adjusting the device size and biasing condition. By optimising the ILO, the wanted locking range, power consumption as well as sensitivity of the receiver can be reached according to the actual need while a high FoM is achieved.

The locking range of an ILO has been well studied in the literature, which is closely related with the self-resonant frequency, quality factor of the core, injection current, and oscillator current. The major way to increase the locking range is to increase the injection current or decrease the quality factor. As shown in Fig. 10, the simulated locking range of the oscillator is almost linearly proportional to the input AC amplitude or injection current, which agrees well with the theory. From the simulation, it is also observed that the quality factor of the ring oscillator is about 2, which is considerably smaller compared with LC tank, making it suitable for wide-range operations.

Similar simulations can be performed to investigate this phase shift in the oscillator. The first step is to investigate the relationship between the phase shift (of input and output signals) and input power of the oscillator. In simulation, the self-resonant frequency is set to be 2.386 GHz while the injected signal has an input frequency of 2.38 GHz. The phase difference keeps decreasing while the input power increases. At the injection AC signal above 0.06 V, there is hardly any change of phase shift. This



**Fig. 9** Self-resonant frequency versus PMOS biasing voltage



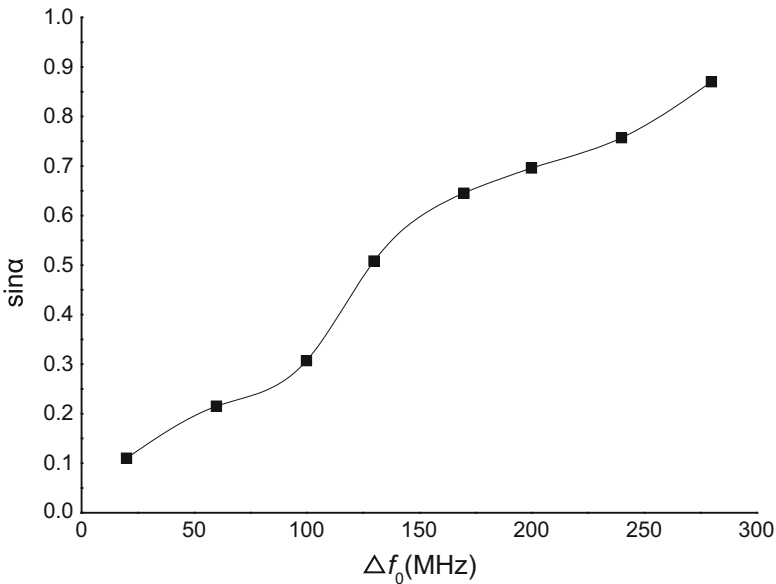
**Fig. 10** Locking range versus input amplitude (at  $f_0 = 2.386$  GHz)

suggests that the input power is a key factor that may greatly impact this phase shift, especially in the cases where the oscillator is working at its extreme conditions. Table 1 summarises the phase shift under these conditions.

A more detail investigation of this effect is carried out as well. The results of phase shift at self-resonant frequency of 2.386 GHz but with different input frequencies are summarised in Fig. 11. It clearly demonstrates the drawback of wideband operation.

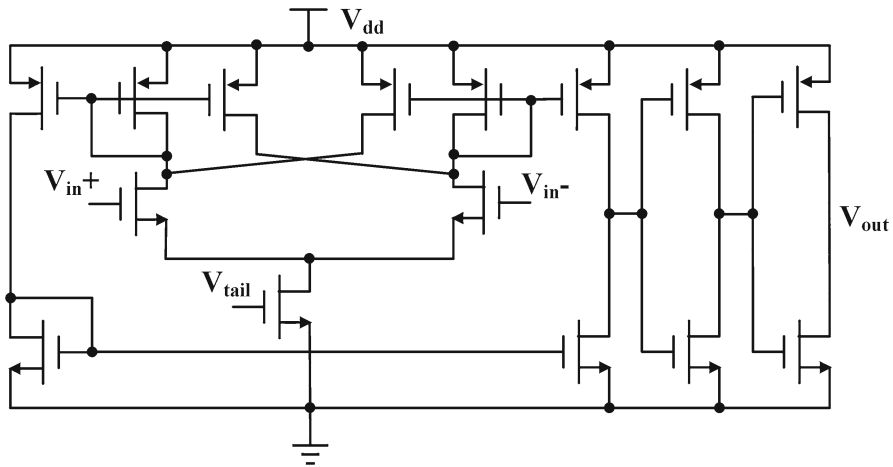
**Table 1** The phase difference at different operating frequencies

	prf (dBm)	$\Delta f_0$ (MHz)	$V_{inj}$ (V)	$t$ (ps)	$\alpha$ ( $^\circ$ )	$\sin\alpha$
1	-35	7	0.011	46.15	39.5	0.636
2	-32	21	0.016	58.59	49.9	0.765
3	-30	36	0.02	57.16	48.3	0.747
4	-28	59	0.025	59.73	50.0	0.766
5	-26	94	0.031	63.49	52.4	0.792
6	-24	143	0.039	76.4	61.7	0.880
7	-22	208	0.05	77.45	60.7	0.872
8	-20	289	0.062	86.49	65.3	0.909

**Fig. 11**  $\Delta f_0$  versus  $\sin\alpha$  (at  $f_0 = 2.386$  GHz)

A large phase difference exists at the operating frequencies far from its self-resonant frequency, which consequently results in a large attenuation at the output amplitude of the mixer.

From these simulations, it is possible to conclude a strategy in designing ILO-based receiver. Even a wide-band operation is highly desired, the ILO is not suitable to be designed to have a large locking range with regarding to the phase shift in the ILO. With different input ranges, the self-resonant frequency should be set to align with input frequency as much as possible by adjusting the biasing condition of the oscillator core. This is achievable if the self-oscillating frequency can be calibrated using auto-frequency control (AFC) to match the input frequency.

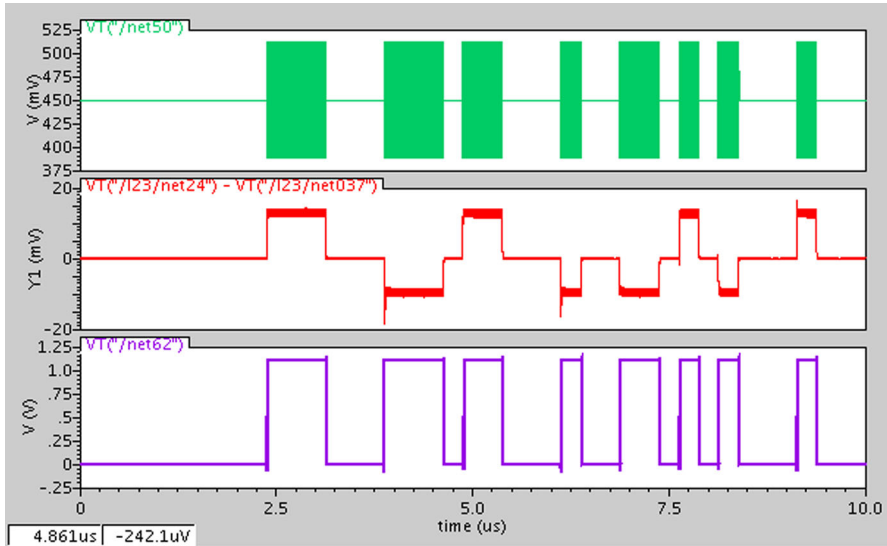


**Fig. 12** Topology of the comparator

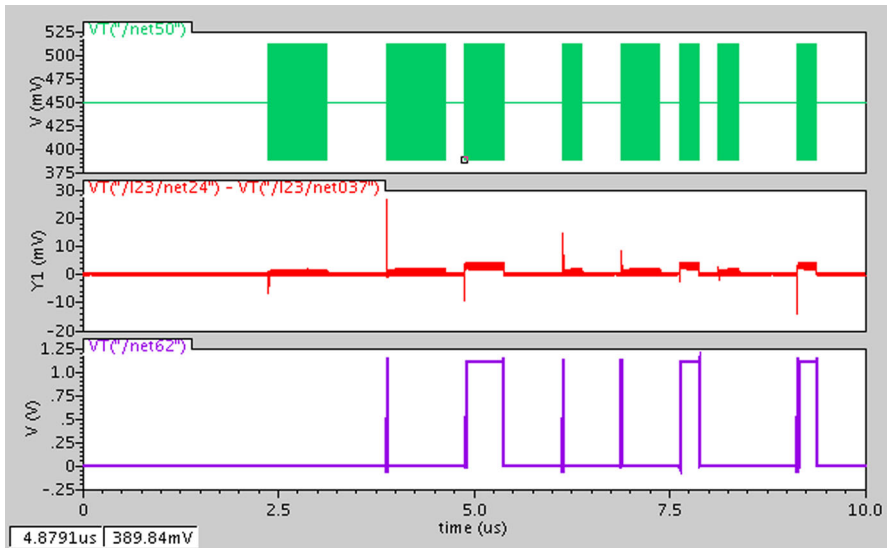
#### 4 Design of a 2.4 GHz Injection-Locked Receiver

Based on above-mentioned design strategies, a 2.4 GHz ILO as well as a demodulator receiver are implemented in a standard 40 nm CMOS technology as a design example. It is designed as follows. The first step is to determine the biasing condition of the PMOS transistor which makes the self-resonant frequency working at around 2.4 GHz, then proper sizing of the transistors and biasing condition for the tail current are performed. Optimisation shows that the ring oscillator is able to work at 2.4 GHz properly with  $<0.2$  mW. Then, a receiver is implemented by adding a mixer, an IF buffer followed by a comparator for data demodulation. These circuits, including a passive single-balanced mixer followed a comparator are shown in Fig. 12. By comparing and amplifying the differential IF signals, the output of the comparator are able to generate rail-to-rail demodulated digital signals.

It is now possible to carry out the investigation of the phase difference in the system simulation. In the simulation setup, the carrier is 2.4 GHz with  $-20$  dBm output power modulated (On-Off-Keying) with 4Mbps random data. The next step is to change the self-resonant frequency to be 2.365 GHz ( $-20$  dBm) with OOK data rate of 4Mbps. As shown in Fig. 13, for an input frequency of 2.37 GHz, the output swing is about 15mV (peak-to-peak). In comparison, if the output frequency is set to be 2.39 GHz, the output amplitude decreases to 7mV. A close look at the signal indicates that the phase difference between the two signals is now  $72^\circ$ , which induces significant degradation of the mixer's output. As shown in Fig. 14, if the input frequency increases to 2.41 GHz, the phase difference reaches  $83^\circ$ . The mixer's output amplitude is now  $<2$  mV, which consequently causes the failure of the comparator and data recovery. It is observed that the phase difference keeps increasing while the injected signal is deviating from the self-resonant frequency of the ILO under the same injection power. The attenuation of the mixer's output will eventually cause the failure of data recovery. This agrees well with the character of an ILO, which requires a stronger injected power at a larger



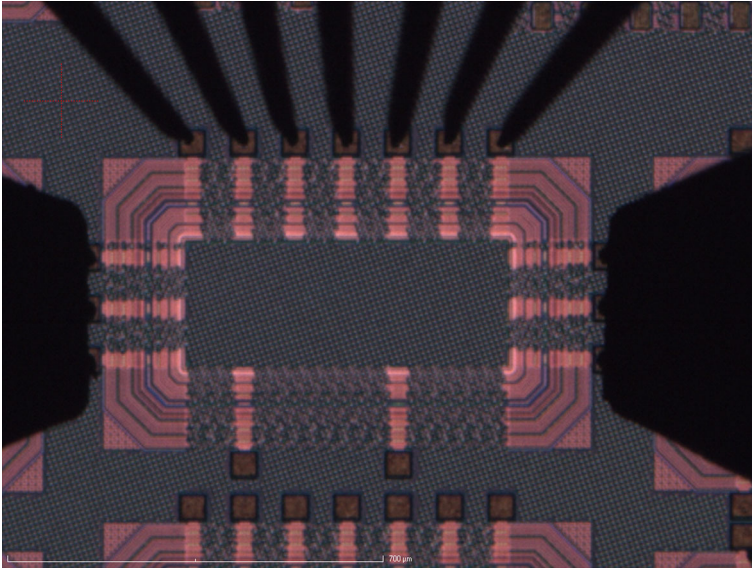
**Fig. 13** Simulated transient results (2.37 GHz carrier 4 Mbps data rate)



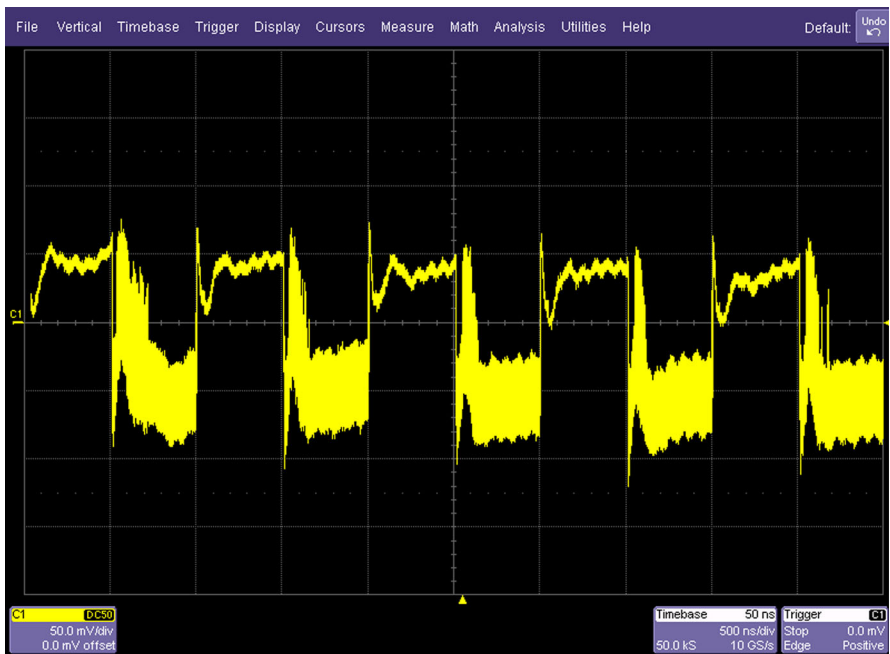
**Fig. 14** Simulated transient results (2.41 GHz carrier 4 Mbps data rate)

frequency offset between the input and output. In real applications, due to the output buffer and loading effects of the following stages, the phase difference can be even larger than that of a separate ILO.

The solutions to this problem should be considered subject to different applications. In a narrow band operation, since the phase difference is considerably small within the locking range, it is not necessary to compensate it as long as the input power is



**Fig. 15** Die photo of the 2.4 GHz receiver



**Fig. 16** Measured input and output of the receiver

**Table 2** Comparison with literatures

Work	Tech. CMOS (nm)	Data rate (Mbps)	Freq. (GHz)	Sens. (dBm)	Power (mW)	FoM (Mbps/mW)
This	40	1	1–2.4	−30	0.3	3.3
[1]	180	0.16	0.9	−18.2	N/A	N/A
[4]	180	1	0.9	−37	0.5–2.5	2
[5]	65	0.5	2.4	−82	0.415	1.2
[6]	90	0.1	2.4	−64	0.051	2
[12]	90	0.1	2	−72	0.052	1.9

within a suitable range under all process corners. If a better sensitivity is desired, a simple push-pull LNA can be added to the system, the system is still of a low power consumption and a small silicon area.

If the system is designed for a wide operating range, the best way is to divide the wide-band into several sub-bands. This can be done by adjusting the biasing condition of the VCO. The importance of this work, is however, the frequency range calibration like an auto-frequency control (AFC) in phase-locked loop. Since the AFC block can be turned off after calibration, no additional power consumption is required.

To demonstrate the possibility of design such a system, a 2.4 GHz receiver is implemented in a standard 40 nm CMOS technology. The receiver is simulated using Cadence Spectre RF under all process corners including possible variations in temperature and supply voltage. Fine-tuning of circuit parameters such as transistor sizes and biasing voltage is performed after the extraction of layout parasitic using Mentor Graphics Calibre PEX. Figure 15 shows the die photo of the proposed receiver. Thanks to its inductor-less topology, the silicon area of the receiver is only 0.09 mm<sup>2</sup>. The input and output of the receivers are placed at the left and right of this test chip by using two GSG pads, while the DC biasing are provided by using an eye-pass DC pad at the top. Measurement is carried out on wafer. The DC basing is done by the eye-pass pads. The signal is generated from ROHDE&SCHAWRZ SMF 100A with a carrier frequency from 1 to 2.4 GHz with on-off-keying (OOK) signal modulated. The input data signal is pseudo-random data with a data rate of 1 Mbps. Figure 16 shows the measured input (OOK signal) and output of the receiver at 2.4 GHz carrier. By tuning biasing of the oscillator, the receiver can work properly with the power level of the input signal as low as −30 dBm. The maximum power consumption is 0.3 mW within the operating range. Table 2 compares the performances of the proposed receivers with those in literatures. Compared with simulation results, the measured receiver exhibits several dB degradation in sensitivity and about 10% less locking range. This is in mainly due to insufficient parasitic extraction of the interconnect and pads. Fortunately, it is possible to fine tune it using DC bias. The measurement results agree reasonably well with the simulations.



## 5 Conclusion

In this paper, the design consideration especially the phase shift of injection-locked oscillator in the receiver is investigated. Simulation results of the key design considerations agree well with the theoretical analysis, which concludes some design strategies. Based on which, an OOK receiver, which maintains a good balance among all these design considerations, is implemented in a standard 40 nm CMOS process. By using an ultra-low power ring oscillator-based injection-locked local oscillator, the receiver is able to work from 2.4 GHz with a data rate as high as 1 Mbps while consuming <0.3 mW power.

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