

# A Dual-Wideband CMOS LNA Using Gain–Bandwidth Product Optimization Technique

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Received: 17 April 2015 / Revised: 12 April 2016 / Accepted: 13 April 2016 /  
Published online: 26 April 2016  
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**Abstract** This paper presents a dual-wideband, common-gate, cascode low-noise amplifier (LNA) using gain–bandwidth product optimization technique. This approach shrinks the aspect ratio of the cascode MOS device, thereby reducing the equivalent parasitic capacitance of the resonator load to optimize the gain–bandwidth product of the LNA. The input impedance of the proposed LNA is analyzed, and the noise factor is well predicted through analytical equations. Measurement results that show well agreement with post-simulation results demonstrate the feasibility of this technique. In low-band mode, experimental results presented a maximum  $|S_{21}|$  of 13.4 dB over a  $-3$ -dB bandwidth of 3.1–4.8 GHz with a minimum noise figure of 4.5 dB. In high-band mode, the proposed LNA achieved a maximum  $|S_{21}|$  of 13.6 dB with a minimum noise figure of 6.2 dB over a  $-3$ -dB bandwidth of 7.3–9.4 GHz. A test chip with a die area of  $0.83 \text{ mm}^2$  was fabricated using a  $0.18 \text{ }\mu\text{m}$  CMOS process. The proposed dual-wideband LNA consumes 9.1 mW, excluding the buffer, from a supply voltage of 1.8 V.

**Keywords** Low-noise amplifier (LNA) · Dual-band · Gain–bandwidth product · Common-gate

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The authors would like to thank the Chung Yuan Christian University for financial support, and thank National Chip Implementation Center (CIC), Hsin-Chu, Taiwan, for chip fabrication and measurement support.

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## 1 Introduction

With the increasing demands for different types of wireless standards integrated in one mobile terminal, the dual-band low-noise amplifiers have recently gained a lot of interest. During the last few years, many methodologies have been proposed for the design of dual-band LNA [1–4, 6, 7, 9–15, 17–22]. One approach is based on a high-value active inductor with a wide tuning range [7, 15]. This approach achieves a good performance with small chip area, however, at the cost of higher power consumption. The second approach involved the use of a notch filter within a wideband LNA to achieve dual-band performance [3, 10, 14, 21, 22]. Unfortunately, this approach also suffers from high power consumption due to the wideband design with an additional notch filter. Another approach involved the use of switched capacitors and switched circuits to realize the dual-band operation [1, 2, 6, 9, 11, 13, 17–20]. This approach, however, still suffered from the trade-off between power consumption, gain, and the bandwidth that was mainly limited by the parasitic capacitance of devices for both bands. As to the bandwidth enhancement of LNA, double loop feedback topology was proposed to obtain wideband performance [12]. However, it is difficult to apply this technique to dual-wideband LNA because it is hard to optimize the component values for both bands simultaneously.

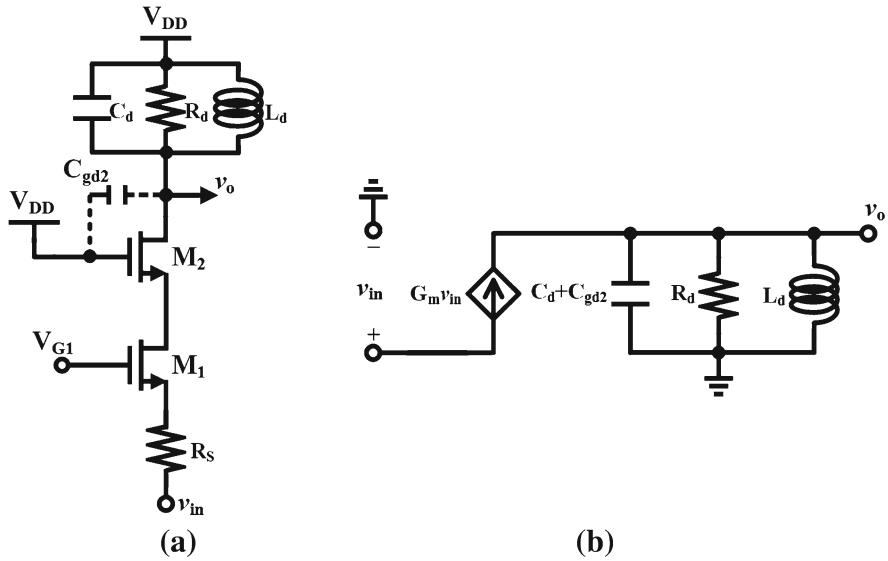
This study employed a switched inductor with common-gate (CG) cascode topology to facilitate the realization of wideband input matching. However, this approach suffered from two drawbacks. The first drawback was the limited  $-3$ -dB bandwidth in the high frequency range due to the parasitic capacitance of MOS devices. The second drawback was a trade-off between the  $-3$ -dB bandwidth and gain. To overcome these drawbacks, this paper proposes a gain–bandwidth product optimization technique that reduces the parasitic capacitance of the cascode MOS device to optimize the gain–bandwidth product of the dual-wideband LNA in the high frequency band.

The remainder of this paper is organized as follows. Section 2 introduces the proposed gain–bandwidth product optimization technique, as well as input impedance matching and noise analysis of the proposed dual-wideband common-gate cascode CMOS LNA. Section 3 presents the simulation and measurement results demonstrating the feasibility of the proposed technique. Section 4 provides conclusions.

## 2 Principles of Circuit Design

### 2.1 Gain–Bandwidth Product Optimization Technique

Figure 1 outlines the typical topology of a common-gate cascode amplifier with single tuned load and the simplified small-signal equivalent circuit, where  $C_d$ ,  $R_d$ , and  $G_m$  are the equivalent capacitance and parasitic parallel resistance of the tank load, and the equivalent transconductance of the common-gate cascode amplifier, respectively. Through simple derivation, we easily obtained the dominant resonant frequency ( $f_{res}$ ),  $-3$ -dB bandwidth (BW), and gain–bandwidth product (GBW), expressed as (1) to (3), respectively [8].



**Fig. 1** **a** Typical topology of common-gate cascode amplifier with single tuned load; **b** Simplified small-signal equivalent circuit of Fig. 1a

$$f_{res} = \frac{1}{\sqrt{L_d (C_d + C_{gd2})}} \tag{1}$$

$$BW = \frac{1}{R_d (C_d + C_{gd2})} \tag{2}$$

$$GBW = \frac{G_m R_d}{R_d (C_d + C_{gd2})} = \frac{G_m}{C_d + C_{gd2}} \tag{3}$$

where

$$G_m = \frac{(g_{m1} + g_{ds1})(g_{m2} + g_{ds2})}{g_{m2} + g_{ds2} + g_{ds1}}$$

Equation (1) clearly shows that the  $L_d(C_d + C_{gd2})$  product must be reduced when the resonant frequency is increased. Thus, most tuned amplifiers operating in the high frequency band adopt only the inductor as the load and utilize the parasitic capacitance of the inductor to replace  $C_d$ . However, at higher frequencies,  $C_d$  also decreases when the load inductance  $L_d$  is decreased. Thus,  $C_{gd2}$  dominates the  $(C_d + C_{gd2})$  term and becomes the factor limiting the bandwidth in the high frequency band. Reducing resistance  $R_d$  would increase the bandwidth; however, this would simultaneously decrease the amplifier gain.

Fortunately, Eq. (3) indicates that the gain–bandwidth product can be improved by decreasing  $C_{gd2}$ . This also means that the gain–bandwidth product can be increased under the same power consumption conditions. Thus, this paper proposes a gain–bandwidth product optimization technique to reduce the width of  $M_2$ , which is

equivalent to reducing parasitic capacitance  $C_{gd2}$  in order to improve the gain–bandwidth product and operation bandwidth of common-gate cascode LNA in the high frequency band.

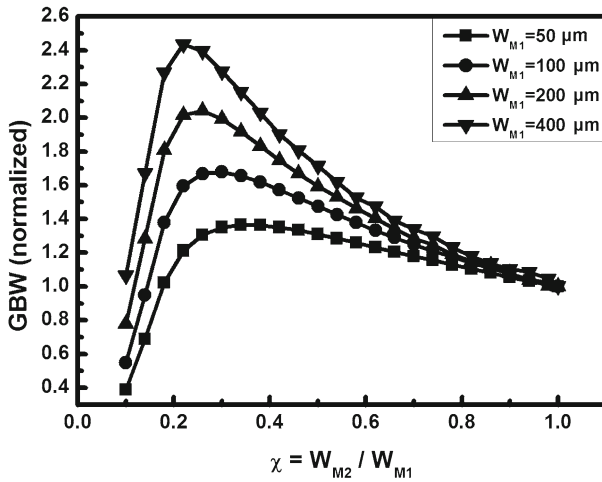
Figure 2 presents the normalized gain–bandwidth product curves versus the ratio of  $W_{M2}$  and  $W_{M1}$ ,  $\chi$ , for  $M_1$  of various widths for most common-gate cascode CMOS LNA designs, in which each curve is normalized to the value of its gain–bandwidth product at  $\chi=1$ . The reason for the maximum value in each GBW curve of Fig. 2 can be explained by expressing the gain–bandwidth product as (4) by rewriting the  $G_m$  and  $C_{gd2}$  of (3) as functions of  $\chi$ .

$$\begin{aligned} \text{GBW} &\approx \frac{g_{m1}}{C_d + C_{gd2}} \\ &\approx \frac{\sqrt{2\mu_n C_{ox} \frac{W_{M1}}{L} I_D \left[ 1 + \lambda \left( V_{DD} - \sqrt{\frac{2I_D L}{\mu_n C_{ox} \chi W_{M1}}} - V_{T2} \right) \right]}}{C_d + \chi C_{gd1}} \end{aligned} \quad (4)$$

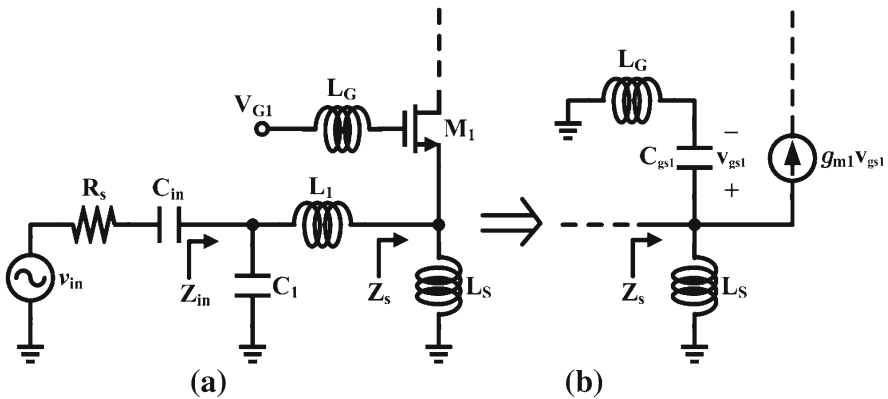
where  $\mu_n C_{ox}$  and  $\lambda$  are the process transconductance parameters and the channel length modulation coefficient of MOSFET devices, respectively.  $W_{M1}/L$  and  $V_{T2}$  are the aspect ratio of  $M_1$  and the threshold voltage of  $M_2$ , respectively. For example, for a given  $W_{M1}$ , when  $\chi$  is close to 1, the  $\chi C_{gd1}$  term dominates the sum in the denominator. As  $\chi$  decreases, the rate of decrease of the denominator is faster than the rate of decrease of the numerator. Thus, the gain–bandwidth product increases. However, as  $\chi$  approaches zero, the denominator is dominated by  $C_d$  and approaches  $C_d$ . Meanwhile, the  $\sqrt{2I_D L/(\mu_n C_{ox} \chi W_{M1})}$  term in the numerator becomes larger, thereby causing the rate of decrease of the numerator to exceed the rate of decrease of the denominator, whereupon the gain–bandwidth product begins decreasing after reaching its maximum value. These results demonstrate the optimum  $\chi$  capable of inducing the maximum gain–bandwidth product. In other words,  $\chi$  can be reduced to the optimum value in Fig. 2, which is equivalent to reducing the  $R_d(C_d + C_{gd2})$  time constant of the resonator load, thereby expanding the bandwidth and optimizing the gain–bandwidth product of the proposed LNA. In addition, when a larger  $W_{M1}$  is selected, a smaller  $\chi$  is required to ensure that the  $\sqrt{2I_D L/(\mu_n C_{ox} \chi W_{M1})}$  term dominates the numerator. This explains why the maximum GBW is achieved at smaller  $\chi$  for curves of larger  $W_{M1}$ .

## 2.2 Input Impedance Matching

Figure 3a presents a schematic diagram of the input impedance matching network and part of the equivalent small-signal circuits of the input impedance matching network of the proposed dual-wideband, common-gate cascode LNA. A source inductor  $L_S$  is used to provide the DC path, and a gate-terminating inductor  $L_G$  is used to compensate the gain attenuation of the common-gate stage in the high frequency range [16]. For the equivalent small-signal circuits shown in Fig. 3b, the input impedance  $Z_s$  can be



**Fig. 2** Normalized gain–bandwidth product curves of Fig. 1 versus the ratio of  $W_{M2}$  and  $W_{M1}$ ,  $\chi$ , for channels of various width of  $M_1$ ,  $W_{M1}$



**Fig. 3** **a** Input matching network of the proposed LNA; **b** part of the small-signal equivalent circuit of the input matching network

expressed as:

$$\begin{aligned}
 Z_s &\approx \frac{1 + s^2 L_G C_{gs1}}{g_{m1} + s C_{gs1}} \parallel s L_S = \frac{s \frac{L_S}{C_{gs1}(L_G + L_S)} (1 + s^2 L_G C_{gs1})}{s^2 + s \frac{g_{m1} L_S}{C_{gs1}(L_G + L_S)} + \frac{1}{C_{gs1}(L_G + L_S)}} \\
 &= \frac{s \frac{L_G L_S}{L_G + L_S} \left( s^2 + \frac{1}{L_G C_{gs1}} \right)}{s^2 + s \frac{\omega_{oi}}{Q_{in}} + \omega_{oi}^2}
 \end{aligned} \tag{5a}$$

where

$$\omega_{oi} = \frac{1}{\sqrt{C_{gs1} (L_G + L_S)}} \tag{5b}$$

$$Q_{in} = \frac{1}{g_{m1}L_S} \sqrt{C_{gs1}(L_G + L_S)} \quad (5c)$$

If the operating frequency meets the condition of (5b), by substituting (5b) into (5a), the input impedance  $Z_s$  can be simplified as:

$$Z_s \approx \frac{L_S}{g_{m1}(L_G + L_S)} \quad (6)$$

For the design cases in this study, impedance  $Z_s$  is lower than  $50 \Omega$  because the transconductance  $g_{m1}$  is designed to be larger than  $20 \text{ mS}$  to meet the high gain requirement. Therefore, we employed an LC ladder resonator to ensure that the input impedance matches  $50 \Omega$ . The input impedance  $Z_{in}$  is expressed as follows:

$$\begin{aligned} Z_{in} &= \frac{1}{Y_{in}} = \frac{1}{sC_1 + \frac{1}{Z_s + sL_1}} \\ &= \frac{Z_s^2 + \omega^2 L_1^2}{Z_s + j\omega [Z_s^2 C_1 - L_1(1 - \omega^2 L_1 C_1)]} \end{aligned} \quad (7)$$

Similarly, the values for  $C_1$  and  $L_1$  can be selected to set the imaginary part of (7) to zero. Thus, the resonant frequency  $\omega_r$  can be tuned to be as close as possible to the operating frequency  $\omega_{oi}$  mentioned in (5b). We can then express the resonant frequency  $\omega_r$  as follows:

$$\omega_r = \frac{\sqrt{L_1 C_1 - (Z_s C_1)^2}}{L_1 C_1} \approx \omega_{oi} = \frac{1}{\sqrt{C_{gs1}(L_G + L_S)}} \quad (8)$$

By substituting (8) into (7), the purely resistive input impedance  $Z_{in}$  can be reformulated as

$$Z_{in} = \frac{g_{m1}L_1(L_G + L_S)}{L_S C_1} \quad (9)$$

By substituting the design parameters of  $g_{m1} = 40.63 \text{ mS}$ ,  $L_G = 482 \text{ pH}$ ,  $L_S = 4.315 \text{ nH}$ ,  $L_1 = 392 \text{ pH}$ , and  $C_1 = 388.5 \text{ fF}$  into (9), we obtain the input impedance  $Z_{in} \approx 45.6 \Omega$ , which is close to  $50 \Omega$ . Figure 4 presents the simulated loci of  $S_{11}$  of the proposed LNA with and without series input capacitor  $C_{in}$  for frequencies ranging from 3 to 11 GHz.

### 2.3 Noise Analysis

Figure 5 outlines the equivalent circuit of common-gate cascode LNA with the input matching network in Fig. 3a for the calculation of noise. It is assumed that the gain of the LNA is large enough when the LNA is operated at a resonant frequency at which

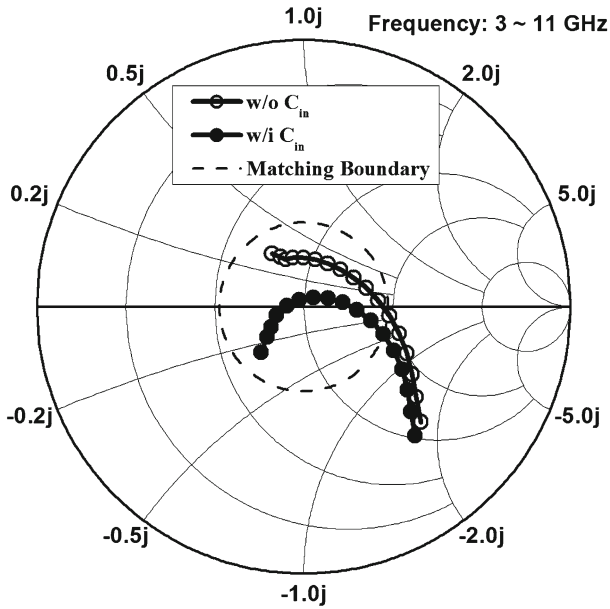


Fig. 4 Loci of  $S_{11}$  of the proposed LNA with and without series input capacitor  $C_{in}$

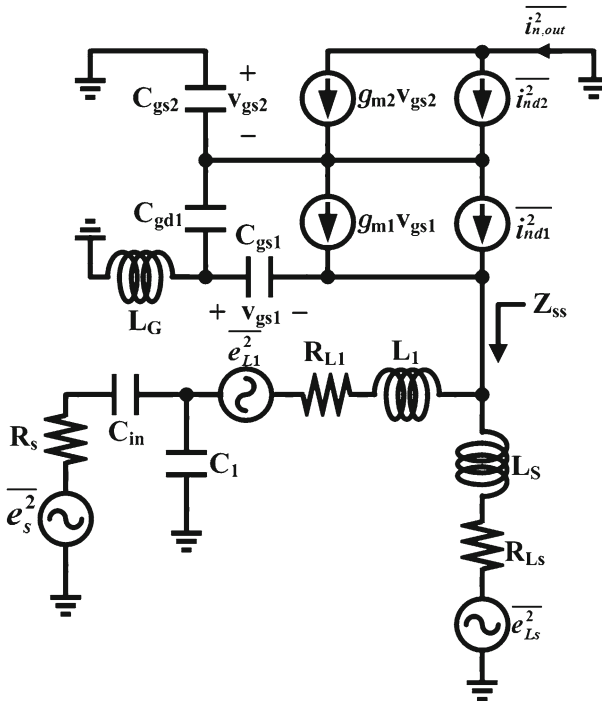
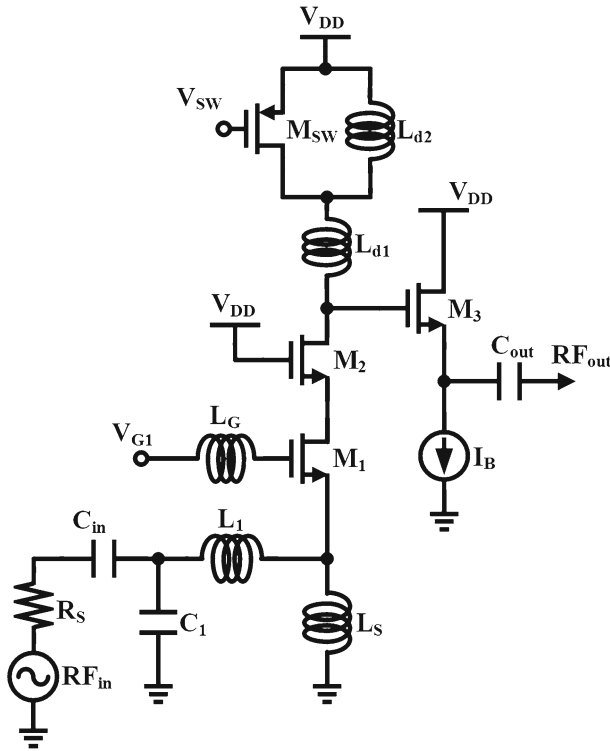


Fig. 5 Equivalent circuit of CG cascode LNA with input matching network for calculation of noise



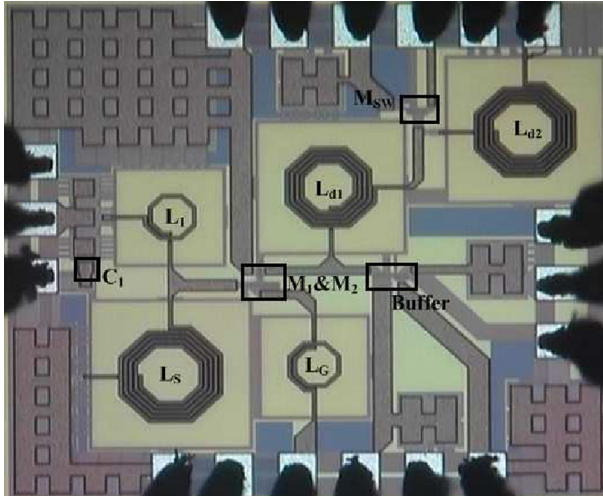
**Fig. 6** Schematic of the proposed dual-wideband common-gate cascode LNA

the noise contribution from the resonator load can be disregarded. Thus, the noise factor can be expressed as follows:

$$\begin{aligned}
 F &= \frac{\overline{|i_{n,out}^2|}}{\overline{|i_{so}^2|}} \\
 &\approx 1 + \frac{\overline{|i_{L1o} + i_{Lso} + i_{nd1o} + i_{nd2o}|^2}}{\overline{|i_{so}^2|}} \\
 &= 1 + \frac{\overline{|i_{L1o}^2|}}{\overline{|i_{so}^2|}} + \frac{\overline{|i_{Lso}^2|}}{\overline{|i_{so}^2|}} + \frac{\overline{|i_{nd1o}^2|}}{\overline{|i_{so}^2|}} + \frac{\overline{|i_{nd2o}^2|}}{\overline{|i_{so}^2|}} \\
 &= 1 + F_{L1} + F_{Ls} + F_{M1} + F_{M2}
 \end{aligned} \tag{10}$$

where  $i_{n,out}$  represents the total noise current in the short-circuited output path originating from noise current components  $i_{so}$ ,  $i_{L1o}$ ,  $i_{Lso}$ ,  $i_{nd1o}$ , and  $i_{nd2o}$ , which are produced by the noise generators  $e_s$ ,  $e_{L1}$ ,  $e_{Ls}$ ,  $i_{nd1}$ , and  $i_{nd2}$ , respectively.  $F_{L1} = \overline{|i_{L1o}^2|}/\overline{|i_{so}^2|}$ ,  $F_{Ls} = \overline{|i_{Lso}^2|}/\overline{|i_{so}^2|}$ ,  $F_{M1} = \overline{|i_{nd1o}^2|}/\overline{|i_{so}^2|}$ , and  $F_{M2} = \overline{|i_{nd2o}^2|}/\overline{|i_{so}^2|}$  represent the





**Fig. 7** Micrograph of the proposed dual-wideband common-gate cascode LNA

corresponding noise factor contributions of  $i_{L1o}$ ,  $i_{Lso}$ ,  $i_{nd1o}$ , and  $i_{nd2o}$  to the LNA, respectively.

Equations (11a)–(11g) present each noise factor in detail, where  $g_{d0}$  is the drain–source conductance at zero  $V_{DS}$ ,  $\alpha$  is the ratio of  $g_m$  to  $g_{d0}$ ,  $\gamma$  is the coefficient of channel noise, and  $Z_{ss}$  is the equivalent impedance observed in the input impedance network from the channel noise source  $i_{nd1}$ .

$$F_{L1} = \frac{R_{L1}}{R_s} \left| \frac{sR_s C_{in} C_1 + C_{in} + C_1}{C_{in}} \right|^2 \tag{11a}$$

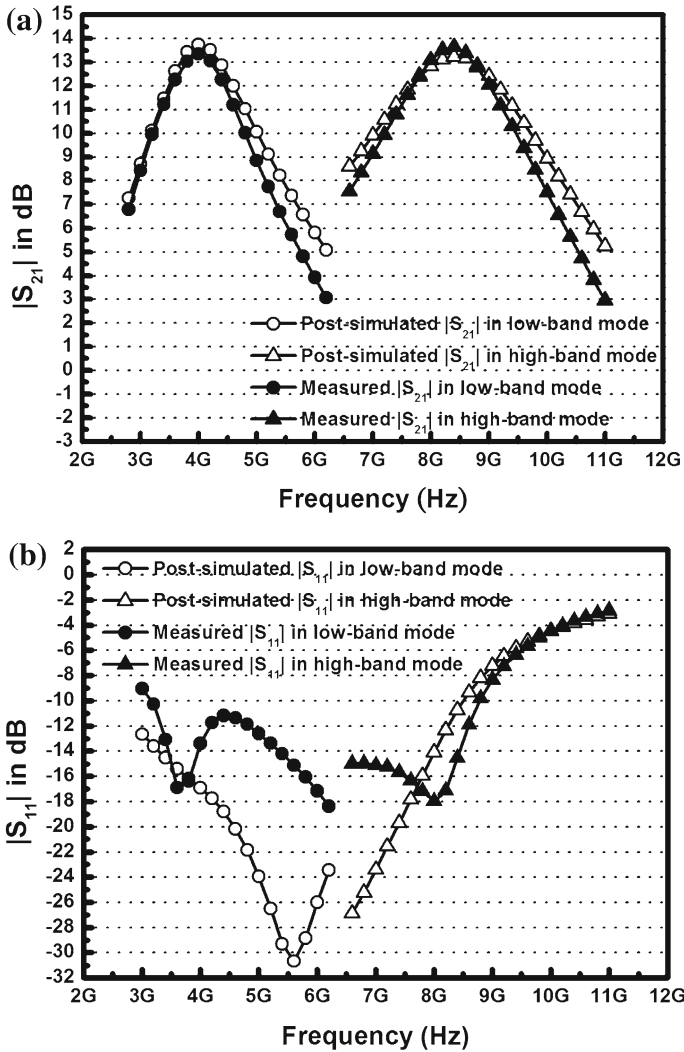
$$F_{Ls} = \frac{R_{Ls}}{R_s} \left| \frac{s^3 R_s L_1 C_{in} C_1 + s^2 L_1 (C_1 + C_{in}) + s R_s C_{in} + 1}{s^2 L_s C_{in}} \right|^2 \tag{11b}$$

$$F_{M1} = \frac{g_{m1} \gamma}{\alpha_1 R_s} \left| \frac{s^2 L_G (C_{gd1} + C_{gs1}) + s C_{gs1} Z_{ss} + 1}{H_o(s)} \right|^2 \tag{11c}$$

$$F_{M2} = \frac{g_{m2} \gamma}{\alpha_2 R_s} \left| \frac{A(s)}{g_{m2} \cdot H_o(s)} \right|^2 \tag{11d}$$

where

$$A(s) = s \{ s^3 L_G C_{gs1} C_{gs2} C_{gd1} Z_{ss} + s^2 L_G [C_{gs1} (C_{gd1} + C_{gs2}) + C_{gs2} C_{gd1} (g_{m1} Z_{ss} + 1)] + s [C_{gs1} Z_{ss} (C_{gd1} + C_{gs2}) + g_{m1} L_G C_{gd1}] + (C_{gd1} + C_{gs2}) (g_{m1} Z_{ss} + 1) \} \tag{11e}$$

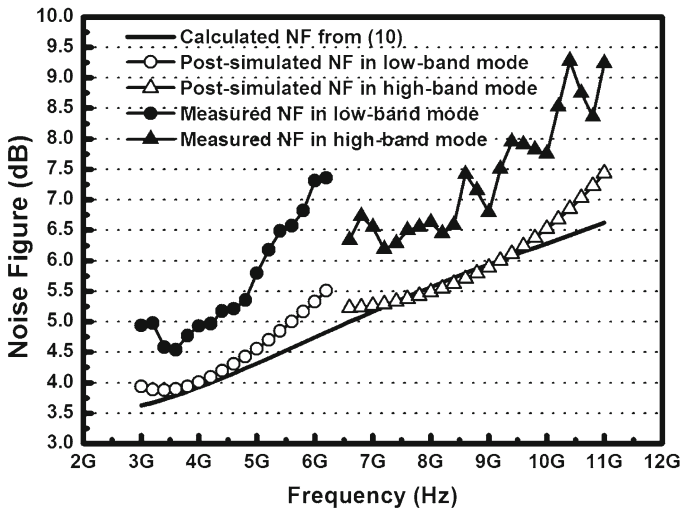


**Fig. 8** Post-simulated and measured **a**  $|S_{21}|$  and **b**  $|S_{11}|$  of the proposed dual-wideband LNA

$$H_o(s) = \frac{s^2 L_S C_{in} (s^3 L_G C_{gd1} C_{gs1} + s^2 g_{m1} L_G C_{gd1} + g_{m1})}{s^3 R_s C_1 C_{in} (L_1 + L_S) + s^2 (L_1 + L_S) (C_{in} + C_1) + s R_s C_{in} + 1} \quad (11f)$$

and

$$Z_{ss} = \frac{s L_S [s^3 R_s L_1 C_1 C_{in} + s^2 L_1 (C_{in} + C_1) + s R_s C_{in} + 1]}{s^3 R_s C_1 C_{in} (L_1 + L_S) + s^2 (L_1 + L_S) (C_{in} + C_1) + s R_s C_{in} + 1} \quad (11g)$$



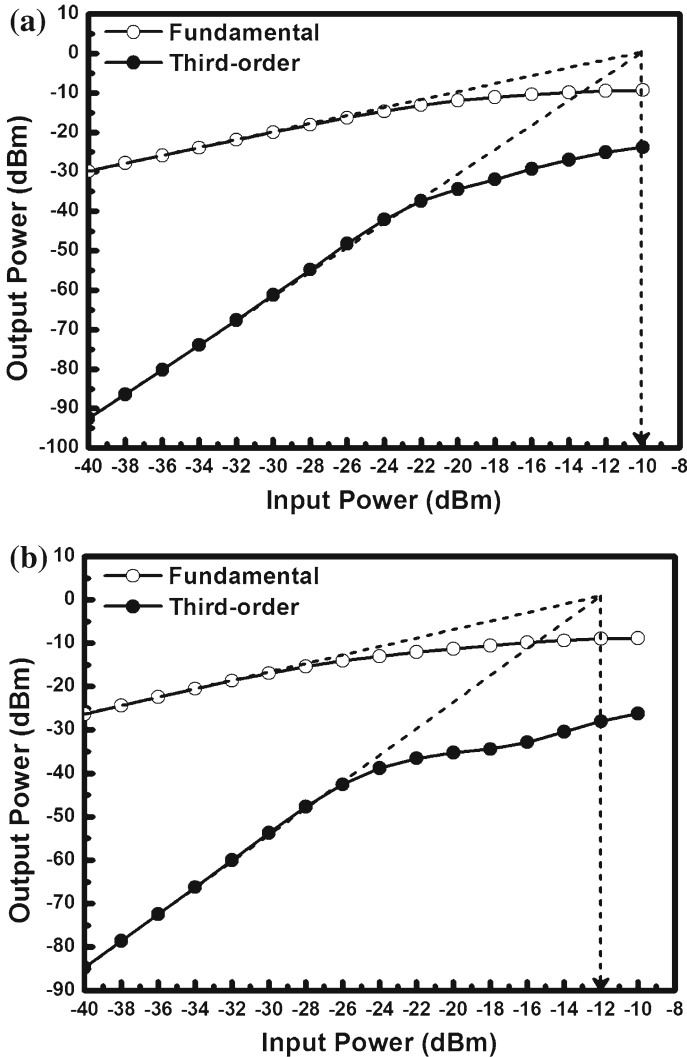
**Fig. 9** Calculated, post-simulated, and measured noise figures of the proposed dual-wideband LNA

## 2.4 Proposed Dual-Wideband Common-Gate Cascode LNA

Figure 6 presents a schematic diagram of the proposed dual-wideband common-gate cascode low-noise amplifier. This dual-wideband LNA is operated between 3.1 and 4.8 GHz in low-band mode and 7.3–9.4 GHz in high-band mode using a band selection switch  $M_{SW}$ . The equivalent parasitic capacitance of the resonator can be reduced by shrinking the size of  $M_2$ . Thus, the proposed dual-wideband LNA is capable of achieving multi-GHz  $-3$ -dB bandwidth when operated in the high frequency range using the proposed gain–bandwidth product optimization technique. The aspect ratio of NMOS  $M_1$  is fine tuned to  $108.8/0.18 \mu\text{m}$  to meet the gain and input matching requirements. Meanwhile, the aspect ratio of NMOS  $M_2$  is set to  $28.8/0.18 \mu\text{m}$ . That is equivalent to  $\chi \approx 0.26$ , which is close to the expected  $\chi$  ratio presented in Fig. 2 with the maximum gain–bandwidth product and expanded bandwidth in the high frequency band. It is worth mentioning that the current consumption of the proposed common-gate cascode LNA shown in Fig. 6 is dominated by the bias condition of  $M_1$ . Therefore, shrinking the width of  $M_2$  will not increase the current consumption of the proposed dual-wideband common-gate cascode LNA. The circuit designers can maximize the gain–bandwidth product of the proposed common-gate cascode LNA by sizing the  $M_2$  transistor and not increasing power consumption.

## 3 Experimental Results

The proposed dual-wideband common-gate cascode LNA was fabricated in a  $0.18 \mu\text{m}$  CMOS process. Figure 7 presents a micrograph of the chip, that occupies  $0.83 \text{ mm}^2$  including pads and bypass capacitors. The testing phase considered on-wafer mea-



**Fig. 10** Measured input-referred third-order intercept point of the proposed dual-wideband LNA with two tone inputs of **a**  $3960 \pm 264$  MHz and **b**  $8184 \pm 264$  MHz

measurements using ground–signal–ground (GSG) and DC probes. Figure 8 presents the post-layout simulated and measured  $|S_{21}|$  and  $|S_{11}|$  of the proposed LNA. The proposed dual-wideband LNA achieved a  $-3$ -dB bandwidth of 3.1–4.8 GHz with a peak gain of 13.4 dB in low-band mode and a  $-3$ -dB bandwidth of 7.3–9.4 GHz with a peak gain of 13.6 dB in high-band mode. Figure 9 presents the calculated, post-simulated, and measured noise figure (NF) of the proposed LNA, where a  $\gamma$  of 2.21 which is a measured average value is adopted for the calculated NF [5]. These results present good agreement between the calculated and simulated  $NF$  at resonant frequencies in

**Table 1** Comparison of recently reported dual-band LNA performances

Reference	−3 dB BW [GHz]	$ S_{11} $ [dB]	$ S_{21} $ Max. [dB]	$NF_{min}$ [dB]	IIP3 [dBm]	Total $P_{diss}$ [mW]	Technology [CMOS]	Die area [mm <sup>2</sup> ]	FoM
[2]	1.67–1.93	< −11	15.0	4.0	6.2@ 1.8 GHz 11@ 2.0 GHz	4.0@ 1 V	90 nm	0.2944	1.03 1.24
[6]	3.1–4.8	< −9.3	6.1	5.0	−4@ 3.96 GHz −7@ 8.18 GHz	24.8@ 1.8 V <sup>b</sup>	0.18 $\mu$ m	N.A.	0.28
[7] <sup>a</sup>	0.7–1.6 2.1–2.7	< −2 < −4	17 20	1.7 2.0	N.A.	19.6@ 1.8 V	0.18 $\mu$ m	0.03	2.30 3.06
[11]	1.8–3.2	< −6.2	10.1	2.9	4@ 2.4 GHz −5@ 5.2 GHz	11.7@ 1.8 V 5.7@ 1.8 V	0.18 $\mu$ m	N.A.	1.22 2.59
[13]	2.0–3.0	< −5	9.4	2.8	−4.3@ 2.45 GHz −5.6@ 6 GHz	2.79@ 1.2 V <sup>c</sup>	0.13 $\mu$ m	0.612	2.25 30.1

**Table 1** continued

Reference	-3dB BW [GHz]	$ S_{11} $ [dB]	$ S_{21} $ Max. [dB]	$NF_{min}$ [dB]	$IIP3$ [dBm]	Total $P_{diss}$ [mW]	Technology [ $\mu\text{m}$ ]	Die Area [ $\text{mm}^2$ ]	FoM
[22]	0.55–1.0	< -3	16	1.9	-6@ 0.9GHz	12@ 1.2V	0.18 $\mu\text{m}$	0.66	1.49
	2.0–2.65	< -5	17	2.0	-2@ 2.4GHz				2.71
This work	3.1–4.8	< -10	13.4	4.5	-10@ 3.96 GHz	9.1@ 1.8 V <sup>c</sup>	0.18 $\mu\text{m}$	0.83	4.09
	7.3–9.4	< -6	13.6	6.2	-12@ 8.18GHz				5.29

<sup>a</sup> Simulation results

<sup>b</sup> With buffer

<sup>c</sup> Without buffer

both the low-band mode (3.95 GHz) and high-band mode (8.35 GHz) to demonstrate the accuracy of (10) and (11a–11g).

Measurement results show that the measured NF in low-band mode was 4.5–5.3 dB between 3.1 and 4.8 GHz. In high-band mode, the measured NF was 6.2–7.9 dB between 7.3 and 9.4 GHz. The discrepancy between the measured and post-layout simulated noise figures was caused by inaccuracies in the noise model. Figure 10a and b presents the measured third-order intermodulation characteristics of the proposed LNA with two tone frequencies of  $3960 \pm 264$  MHz (low-band mode) and  $8184 \pm 264$  MHz (high-band mode), respectively. The measured input-referred third-order intercept points (IIP3) were  $-10$  dBm (low-band mode) and  $-12$  dBm (high-band mode), respectively. The measured input-referred 1-dB compression points were  $-24$  dBm (low-band mode) and  $-27$  dBm (high-band mode), respectively. From a 1.8 V supply, the proposed LNA consumes 9.1 mW, excluding the buffer.

Table 1 summarizes the performance of recently published dual-band LNAs. A figure of merit (FoM) factor shown as (12) that represents the achieved gain–bandwidth product, which is normalized to the power consumption and the process technology, is introduced to reveal the value of the proposed gain–bandwidth product optimization technique.

$$\text{FoM} = \frac{|S_{21}|_{(\text{Abs.})} \cdot \text{Bandwidth}(\text{GHz})}{P_{\text{diss}}(\text{mW})} \times \frac{L_{\text{min}}(\mu\text{m})}{0.18(\mu\text{m})} \quad (12)$$

where  $L_{\text{min}}$  represents the minimum channel length of the CMOS process technology that is used in the corresponding paper.

Compared with other published dual-band LNAs, the proposed LNA achieves the best FoM in both bands. Although [13] achieved an ultra-high FoM value in high-band mode, it suffered from very large  $|S_{21}|$  variation (up to 9.5 dB) due to the low equivalent parallel resistance of the resonator load when the LNA was switched to low-band mode. However, this work maintains nearly the same  $|S_{21}|$  in both low-band and high-band modes that are attributable to the proposed gain–bandwidth product optimization technique.

## 4 Conclusion

This paper presents a dual-wideband, common-gate cascode CMOS LNA using gain–bandwidth product optimization technique. The gain–bandwidth product of the LNA was optimized by reducing the equivalent parasitic capacitance of the resonator load. Compared with other previous works, the proposed LNA achieves the best gain–bandwidth product, which is normalized to the power consumption and process technology, in both bands by utilizing the proposed optimization technique. In other words, circuit designers can maximize the gain–bandwidth product of the proposed common-gate cascode LNA without increasing power consumption, thereby demonstrating the feasibility of the proposed gain–bandwidth product optimization technique.

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