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An 8-bit, 10 KS/s, 1.87 μW Successive Approximation Analog to Digital Converter in 0.25 μm CMOS Technology for ECG Detection Systems

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Abstract This paper presents an 8-bit successive approximation analog to digital converter (SA-ADC) employing a mostly digital implementation for portable Electrocardiogram (ECG) detection systems. At 10 K samples/s, the proposed SA-ADC consumes 1.87 μW from a 1 V power supply. The layout and extraction of the proposed SA-ADC are done using L-edit and simulated using TSMC 0.25 μm technology file on Pspice. According to the simulation results, the SA-ADC has a signal-to-noise ratio of 57 dB, peak spurious-free dynamic range of 41 dB, and a signal-to-noise-and-distortion ratio of 40.5 dB for a 200 Hz–500 mV_{pp} input sine wave. In addition to that, the SA-ADC has effective number of bits of 6.5-bits, an effective resolution bandwidth of 1.5 kHz and a figure of merit of 6.85 pJ/Conversion step. The digitized ECG signal is precisely reconstructed using a novel reconstruction circuit. These results show that the proposed SA-ADC in 0.25 μm technology is a good candidate for ECG detection systems.

Keywords ECG · Low power circuits · SA-ADC · Low-frequency ADC · Portable systems

1 Introduction

The Electrocardiogram (ECG) is an important biomedical diagnostic technique for medical and consumer applications (e.g., diagnosing abnormal rhythms of the heart,

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monitoring stress, measuring energy expenditure, etc.). Commonly, patients are connected to a bulky and mains-powered instrument, which reduce their mobility and creates discomfort [18]. This method limits the acquisition time and prevents the continuous monitoring of patients. Therefore, there is a growing demand for portable ECG detection systems. These systems need to be accurate, precise, and easy to use. The design of these processing systems must be capable of providing different trade-offs between quality, power consumption, and noise immunity depending on the ECG signal characteristics [18,26].

The sequence of electrical events that occurs in the heart can be observed in a typical ECG signal waveform, which in turn consists of three sections as shown in Fig. 1a. The first section is the P wave, which represents the activation of the atria. The second section has three components, and it is called the QRS spike, which represents the contraction of the heart's largest muscle mass (Ventricles). The third section is the T wave, which represents the depolarization of the Ventricles [3].

For pre-processing the ECG signal, a typical system is used as shown in Fig. 1b [14]. Since the cardiac signals are weak amplitude signals, typically in the range of 400 μV–2.5 mV, a preamplifier (Amp1) is used to amplify the ECG signals [2,19]. After this amplifier, a notch filter with notch frequency of (50/60 Hz) is used to attenuate the line power interference [2,6,10,11,14,16,21]. Due to the attenuation provided by the notch filter to the ECG signals [14], the output of the notch filter is re-amplified by Amp2 and then band-limited by a LPF [12,13,23,24]. Finally, the output of the LPF is amplified, and hence, the dynamic range required by the analog to digital converter (ADC) is relaxed. The combined gain/filtering operations ensure that the unwanted out-of-band signals and the in-band line power interference signal are attenuated while the desired ECG signal is amplified [15]. The last block in the analog front end of the ECG detection systems is the ADC, which is a fundamental part to diagnose the heart activities using a digital signal processor.

The objective of this work is to choose the best ADC candidate for ECG detection systems. Due to the existence of many types of ADCs, a comparative study was performed based on a survey of [4,6–9,20] as summarized in Table 1. As a result of this study, the successive approximation ADC (SA-ADC) was chosen for its moderate speed, moderate accuracy, and low power dissipation which meets the requirements of portable ECG detection systems. Since the ECG signal is a low-frequency signal ranging from 0.05 to 250 Hz, the theoretical sampling frequency is 500 Hz (the Nyquist rate). However, a sampling frequency of 10 kHz was chosen to relax the design of the reconstruction filters, which improves the signal-to-noise ratio and reduces the effects of harmonics. This sampling frequency is also considered sufficient to achieve a trade-off between reasonable conversion time and a practical clock frequency of 100 kHz for an 8-bit ADC [9].

This paper is organized as follows: Section 2 introduces the SA-ADC block diagram and the design and analysis of its building blocks. Next, Sect. 3 gives the post-layout simulation results of the SA-ADC. Section 3 also presents the design of the reconstruction circuit and the final simulation results. Finally, Sect. 4 concludes the paper.

Table 1 Comparison between different types of ADCs

Type	Comparison parameter		
	Speed	Accuracy	Power consumption
Flash ADC	High (fastest type)	Low to medium	High
Interpolating flash ADC	High	Low to medium	Medium
Two step ADC	High	Low to medium	Medium
Folding ADC	High	Low to medium	Medium
Integrating ADC	Low	High	Low
Pipelined ADC	High	Low to medium	Low
Counting ADC	Low	High	Low
Time interleaved ADC	High	Low to medium	Medium to high
Successive approximation ADC	Medium	Medium	Low
Cyclic ADC	Low to medium	Medium	Low
Oversampling ADC	Low to medium	High	Low

2 Circuit Design and Analysis of the SA-ADC Building blocks

A block diagram of the 8- bit SA-ADC [22] is shown in Fig. 2. This ADC consists of a sample and hold (S/H), a comparator, a successive approximation register controller (SAR), and an 8-bit digital to analog converter (DAC). Although SA-ADC is considered to be a low power ADC, the realization of the SA-ADC proposed in this work guarantees further reduction in power. This achieved by using a simple op-amp-free S/H circuit, capacitor-based DAC, and simple logic gates in the SAR controller. Therefore, the only analog circuit in this design is the comparator. The circuit design and analysis of the building blocks of the SA-ADC will be presented in the following subsections.

2.1 Sample and Hold (S/H) Circuit

The proposed successive approximation ADC uses a simple S/H circuit. This S/H circuit achieves the requirements of small offset and low power consumption [5]. The S/H circuit as shown in Fig. 3 consists of the NMOS switch (M_1), the dummy switch (M_2), and the sampling capacitor (C_H). The dummy switch is used to minimize the errors of charge injection and clock-feed-through. These errors will be presented and suppressed in Sects. (2.1.1) and (2.1.2), respectively.

2.1.1 Charge Injection and Clock-Feed-Through

The charge injection and clock-feed-through are issues that mainly occur when using transistors as switches in switched-capacitor circuits [17]. When the clock at the NMOS gate goes high (V_{DD}), the transistor turns ON, and the input voltage (V_{in}) is sampled by the capacitor C_H. The channel charge under the gate oxide is given as follows:

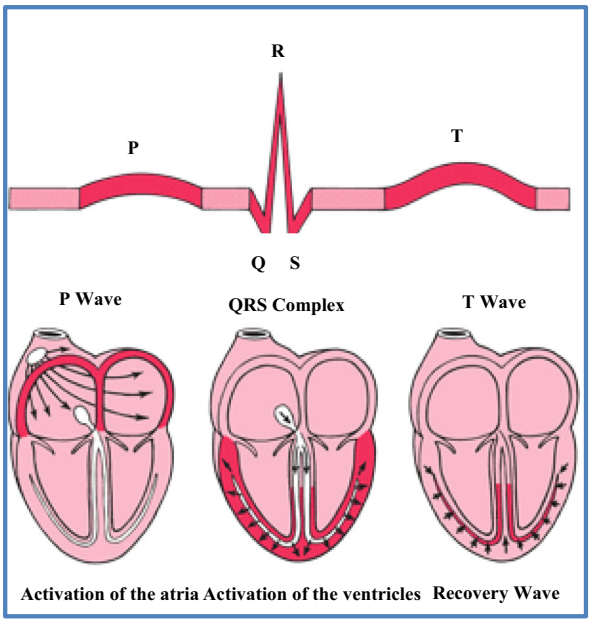


Fig. 1 **a** Typical ECG signal [3], **b** Block diagram of an ECG detection system [15]

$$Q_{\mathrm{ch}} = \mathrm{WLC_{ox}}(V_{\mathrm{DD}} - V_{\mathrm{in}} - V_{\mathrm{tn}}) \tag{1}$$

Then, when the clock goes low, the transistor turns OFF, and its channel charge flows out from its gate into the source and the drain creating an error in the sampled voltage [7]. The charge injection produces different errors that affect the accuracy of the sampler. Assuming that all of the charges are deposited on the capacitor, the sampled output voltage is given by the following equation:

$$V_{\mathrm{out}} = V_{\mathrm{in}}\left(1 + \frac{\mathrm{WLC_{ox}}}{C_{\mathrm{H}}}\right) - \frac{\mathrm{WLC_{ox}}}{C_{\mathrm{H}}}(V_{\mathrm{DD}} - V_{\mathrm{tn}}) \tag{2}$$

Therefore, the output voltage is affected by a non-unity gain which is equal to $(1 + \frac{\mathrm{WLC_{ox}}}{C_{\mathrm{H}}})$ and a constant offset voltage equal to $\{-\frac{\mathrm{WLC_{ox}}}{C_{\mathrm{H}}}(V_{\mathrm{DD}} - V_{\mathrm{tn}})\}$ [8,10].

In the clock-feed-through issue, the MOS switch couples the clock transitions to the sampling capacitor through its gate drain or gate source overlap capacitances. When

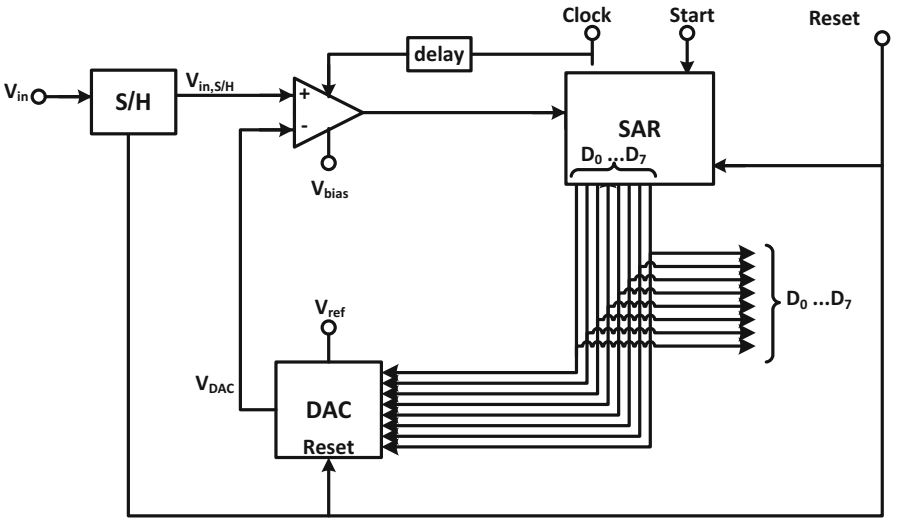
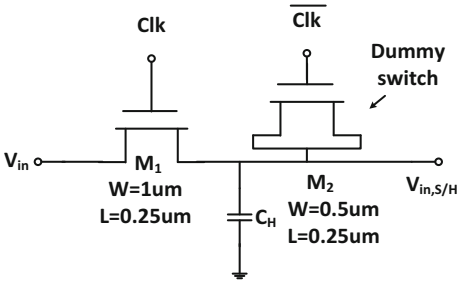


Fig. 2 SA-ADC block diagram [22]

Fig. 3 The S/H circuit



the clock signal goes high, an overlap capacitance is fed through the gate source, the gate drain, or both. On the other hand, when the clock goes low, the transistor turns OFF, and a capacitive divider is created. This operation causes an offset voltage (ΔV_{offset}), which is given as follows:

$$\Delta V_{\text{offset}} = \frac{C_{\text{ov}}}{C_{\text{ov}} + C_{\text{H}}} V_{\text{DD}} \tag{3}$$

where C_{ov} is the overlap capacitance.

2.1.2 Removing Charge Injection

The dummy switch is one of the most commonly used methods to cancel the effect of the charge injection and the clock-feed-through. Referring to Fig. 4, the dummy switch is a normal MOS transistor with its source and drain shorted. When M_1 turns OFF and M_2 turns ON, the channel charge deposited on C_{H} is absorbed by the dummy switch (M_2). The charge injected by $M_1(\Delta q_1)$ and the charge absorbed by $M_2(\Delta q_2)$ can be expressed, respectively, as follows:

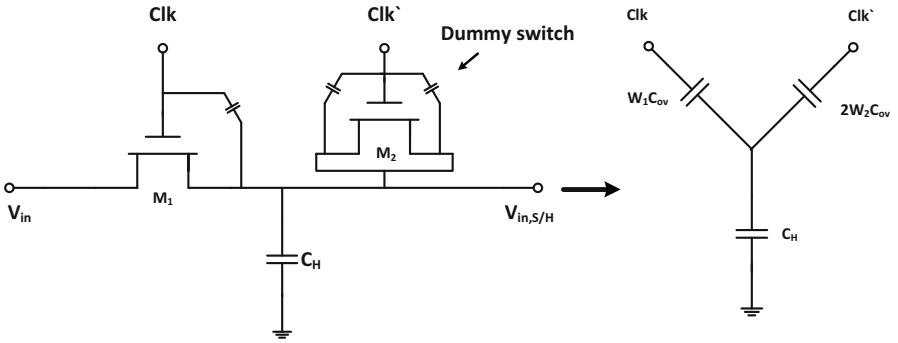


Fig. 4 Clock-feed-through suppression by dummy switch

$$\Delta q_1 = \frac{W_1 L_1 C_{\text{ox}}(V_{\text{DD}} - V_{\text{in}} - V_{\text{tn1}})}{2} \tag{4}$$

$$\Delta q_2 = W_2 L_2 C_{\text{ox}}(V_{\text{DD}} - V_{\text{in}} - V_{\text{tn2}}) \tag{5}$$

For $\Delta q_1 = \Delta q_2$, the channel width of M_2 should be half that of M_1, assuming $L_1 = L_2$ [1,7]. Thus, the effect of the charge injection and clock-feed-through will be suppressed.

The S/H circuit was simulated using TSMC 0.25 μm technology with a clock signal frequency of 10 kHz and a sampling capacitor of 0.5 pF. Figure 5 shows the sampled output signal for a 250Hz–500 mV_{pp} sinusoidal input signal. The signal-to-noise-and-distortion ratio (SNDR) of the sample and hold circuit is about 63.708dB. It is worth noting that the value of the sampling capacitor is a function of two main factors: the ADC input range and resolution, which translates into an equivalent thermal noise specification ($\frac{KT}{C_H}$). The sampled output signal of the S/H circuit will be connected to the non-inverting input terminal ($V_{\text{in}+}$) of the comparator circuit in the following subsection.

2.2 Comparator Circuit

There are two types of comparators: static and dynamic comparators. Since the dynamic comparators are used for high-speed applications, a static comparator has been chosen for this work as it meets the medium speed requirement of the ECG detection systems [25].

Figure 6 shows the comparator circuit. The comparator operational principle is as follows: When the clock goes low, both M_{s1} and M_{s2} will turn OFF, and the circuit executes the comparison between the two inputs. If $V_{\text{in}+} > V_{\text{in}-}$, M_1 will be ON and M_2 will be OFF. Therefore, $V_{\text{out}-}$ will go low, and $V_{\text{out}+}$ will go high. On the other hand, if $\text{Vin}_+ < V_{\text{in}-}$, M_1 will be OFF and M_2 will be ON. Therefore, $V_{\text{out}+}$ will go low, and $V_{\text{out}-}$ will go high. When the clock is high, both outputs are pulled to V_{DD}, and the comparator is operating in resetting mode. The resetting mode is needed to make the comparator idle for a short time until the SAR and DAC blocks complete their operation. The speed of operation is determined by the pole frequency. The dominant pole frequency of the comparator is located at node P and is given as follows:

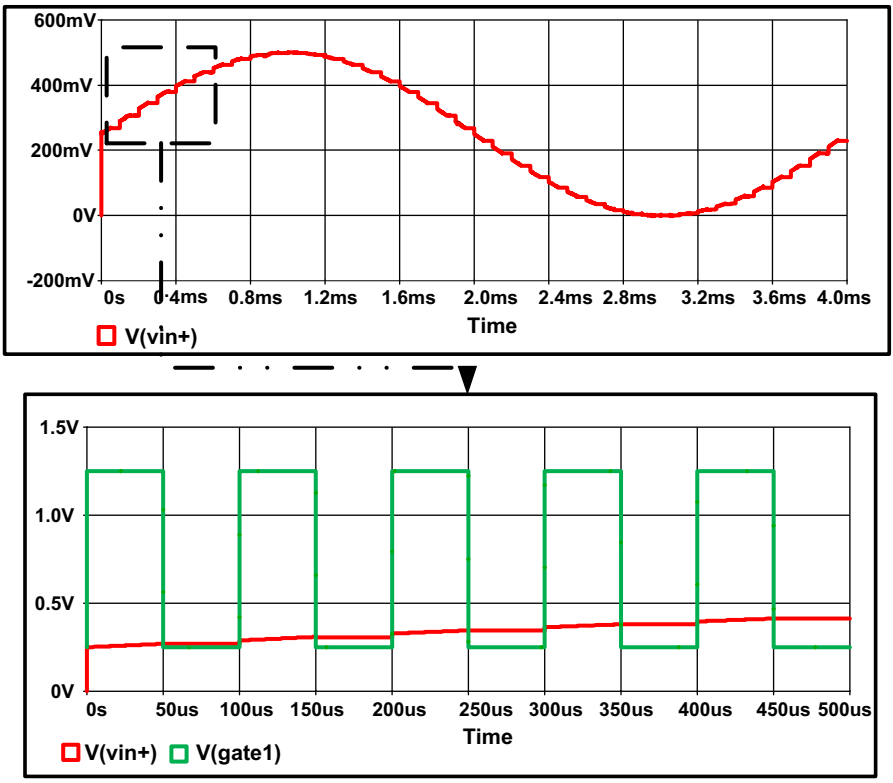


Fig. 5 The sampled output signal

$$\omega_p = \frac{g_{m1}}{C_p}, C_p = C_{gs3} + C_{db2} + C_{db4} + C_{db\_s2} + C_{buffer} \tag{6}$$

where C_p represents the total capacitances at node P.

At 100 kHz clock frequency, the comparator consumes $\approx 0.9\,\mu$W from 1 V power supply. Figure 7 shows the output of the comparator when V_{in+} is connected to the sampled output of the S/H circuit while V_{in-} is DC voltage of 0.4 V. As shown, the comparator output is kept high when the clock is high, whereas the comparison operation is performed when the clock is low. Since this comparator is static, glitches around 0.4 V are expected. It is worth noting that the DC voltage which was fed into the inverting terminal (V_{in-}) of the comparator circuit is coming from the output of the DAC that will be presented in the following subsection.

2.3 Capacitor-Based DAC

In order to achieve low power dissipation and relatively small area of the SA-ADC, a DAC that is based on a binary weighted switched-capacitor array is implemented. Figure 8 shows the schematic of the capacitor-based DAC. The switches are realized

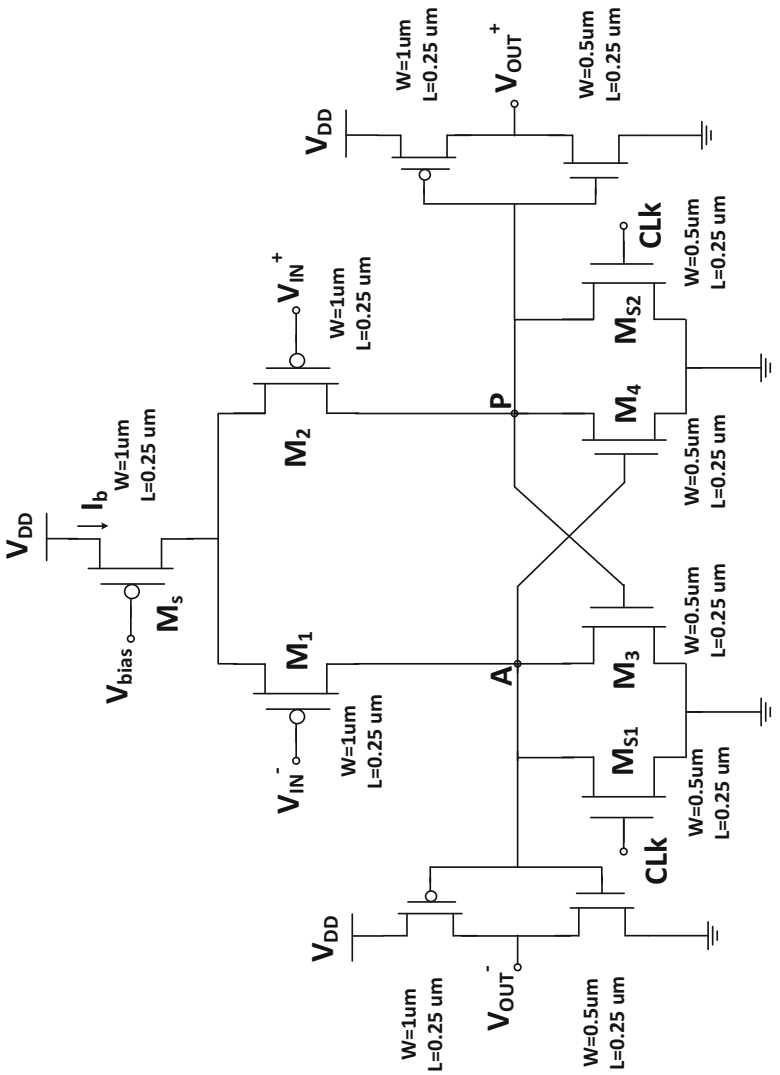


Fig. 6 Schematic of the comparator circuit

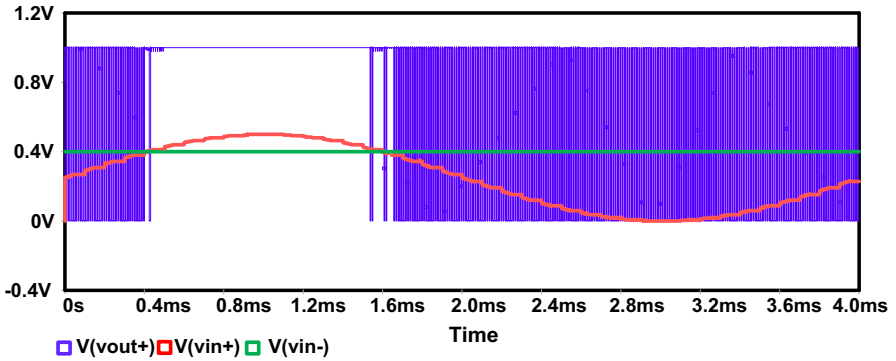


Fig. 7 The comparator output along with the sampled input signal compared with 0.4V

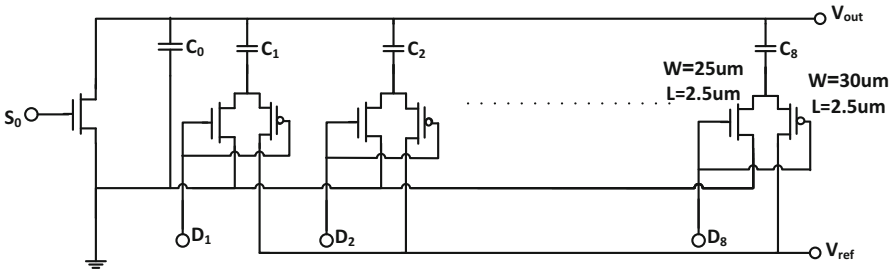


Fig. 8 Schematic of the capacitor-based DAC circuit

by using NMOS and PMOS transistors with each capacitor in the array. The DAC circuit accepts an 8-input bits that are coming from the SAR controller which will be presented in the following subsection.

The DAC was simulated using TSMC 0.25 μm technology with the transistor aspect ratios given in Fig. 8. The unit capacitor (C_0) has a value equal to 24fF, which is used to calculate the values of the other capacitors in the array by the following equation:

$$C_i = 2^{i-1}C_0, i \in \{1, \ldots, 8\} \tag{7}$$

According to the simulation results, the DAC consumes ≈ 55nW from the 1 V reference voltage. The simulated output voltage of the DAC is 0.97 and 0.48 V for the input bit combinations (11111111) and (01111111), respectively. These simulation results show that there is a good agreement between the simulated DAC output and the theoretical DAC output, which in turn can be calculated by the following equation:

$$V_{\mathrm{DACi}} = V_{\mathrm{ref}} \frac{C_i + \sum_{j=i+1}^{8} D_j C_j}{C_{\mathrm{DAC}}} \tag{8}$$

where the V_{DACi} is the DAC output voltage in the ith cycle.

2.4 SAR Controller

In general, two registers are required to implement the SAR controller: one register for storing the results of the conversion and another one for estimating the results. A non-redundant SAR controller is used to reduce the power consumption and minimize the area of the controller.

Figure 9 shows the schematic of the SAR controller. The controller starts its operation when a reset signal sets the MSB to ONE. Then, the output of the controller is applied to the DAC and compared with the input signal. If the output of the comparator is high, the controller will set the MSB to ONE, whereas if the output of the comparator is low, the controller will set the MSB to ZERO. This procedure is then repeated for all bits until the output word is determined.

The design idea of the SAR controller comes from the fact that starting from the second cycle, the value of each bit (j), where $8 > j \geq 0$, has three possibilities:

- If bit (j) and all other least significant bits ($j-2, j-1, \ldots, 0$) have a value of ZERO, the next value of bit (j) is the same as the current value of the bit (j+1).
- If bit (j) has a value of ONE and all other least significant bits have a value of ZERO, the next value of bit (j) is equal to the comparator's output.
- If at least one of the bits that are less significant than bit (j) have a value of ONE, the next value of bit (j) is the same as its current value.

The output of each control unit in each cycle is given by the following equation:

$$\mathrm{Bit}(j)_{\mathrm{next}} = \overline{\mathrm{Mem}} \times \overline{\mathrm{Bit}(j)} \times \mathrm{Shift} + \mathrm{Bit}(j) \times \mathrm{Load} + \mathrm{Mem} \times \mathrm{Bit}(j) \qquad (9)$$

where (load) is the comparator's output, (Mem) is the OR operation result of the least significant bits and (shift) is the value of the previous bit.

Figure 10 shows the output bits of the SAR controller when the (Load) input is low, while Fig. 11 shows the output bits of the SAR controller when the (Load) input is high. These outputs are consistent with the theoretically expected outputs and were obtained from the simulation results of the SAR controller. The SAR consumes $\approx 0.92\,\mu\mathrm{W}$ from a 1V supply voltage. The inverters and the NOR gates have aspect ratios of ($2\,\mu\mathrm{m}/0.25\,\mu\mathrm{m}$) for the PMOS transistors and ($0.5\,\mu\mathrm{m}/0.25\,\mu\mathrm{m}$) for the NMOS transistors, whereas the NAND gates of the flip flop have aspect ratios of ($5.5\,\mu\mathrm{m}/0.25\,\mu\mathrm{m}$) for PMOS transistors and ($2.5\,\mu\mathrm{m}/0.25\,\mu\mathrm{m}$) for the NMOS transistors.

3 SA-ADC Layout, ECG Signal Reconstruction and Performance Evaluation

The overall SA-ADC including the S/H circuit, the comparator circuit, the capacitor-based DAC circuit, and the SAR controller circuit is shown in Fig. 12. The proposed SA-ADC has been designed, extracted, and simulated in $0.25\,\mu\mathrm{m}$ TSMC technology model file using L-edit. The layout of the proposed SA-ADC is illustrated in Fig. 13.

The output of the SA-ADC is fed into the input of a reconstruction circuit to evaluate the performance of the proposed circuits. The proposed ECG reconstruction circuit

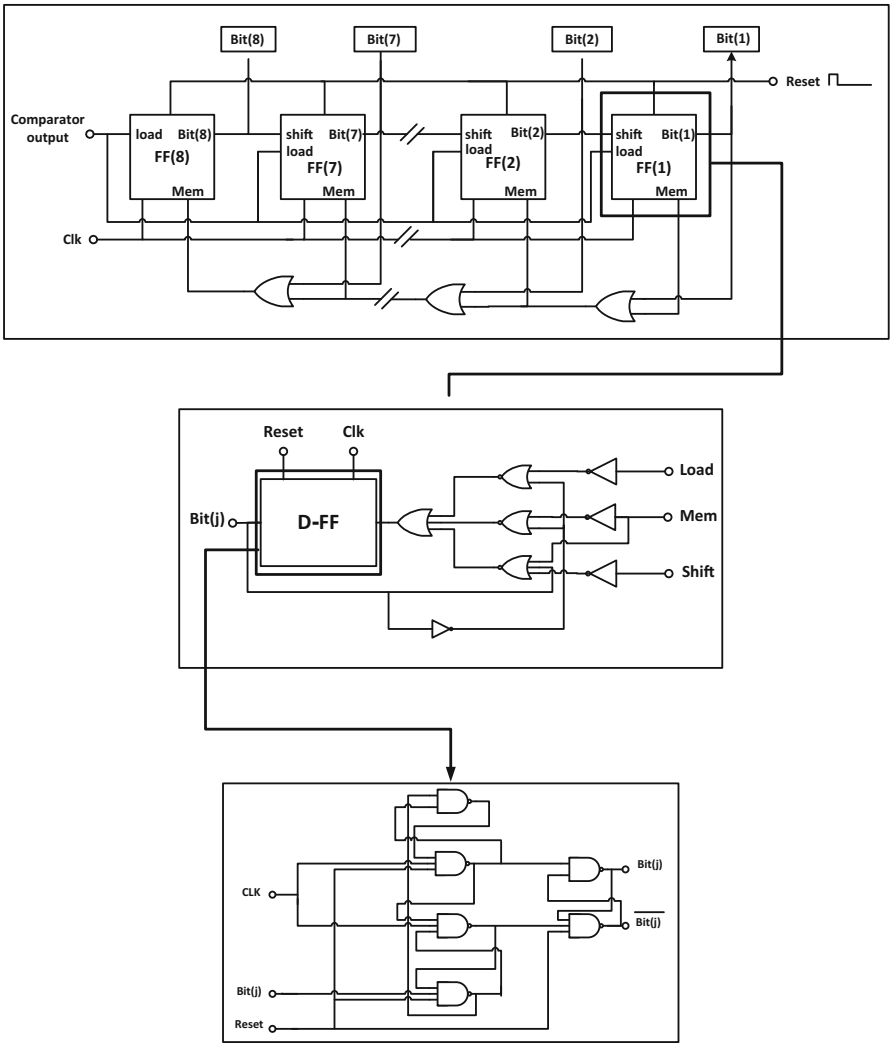


Fig. 9 Schematic of the SAR controller

(as shown in Fig. 14) consists of a DAC, two S/H circuits, two buffers, two low-pass filters, and a voltage summer. Since the ECG signal consists of three main sections that have different amplitudes and rates of change, the dual reconstruction method is adopted [23]. One path is used to reconstruct the QRS spike which has high amplitude and high rate of change, while the other path is used to reconstruct the P and T waves which have lower amplitude and low rate of change. It is worth noting that the QRS path works only during the QRS spike; this is achieved by the AND operation of the clock with the ECG signal as shown in Fig. 14. The QRS path is only activated when the output of the AND gate is high, which in turn occurs when the ECG signal is in the QRS section. The final reconstructed ECG signal is then obtained by adding the

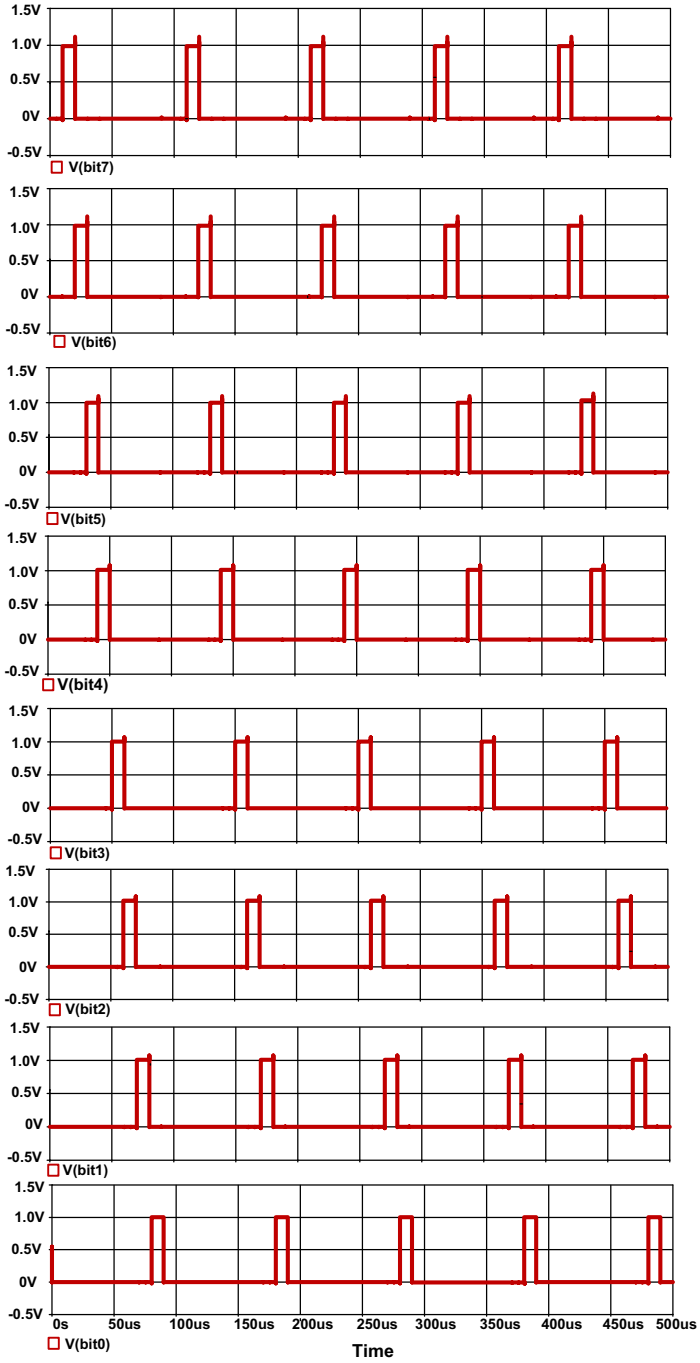


Fig. 10 The SAR controller output when (Load) is LOW

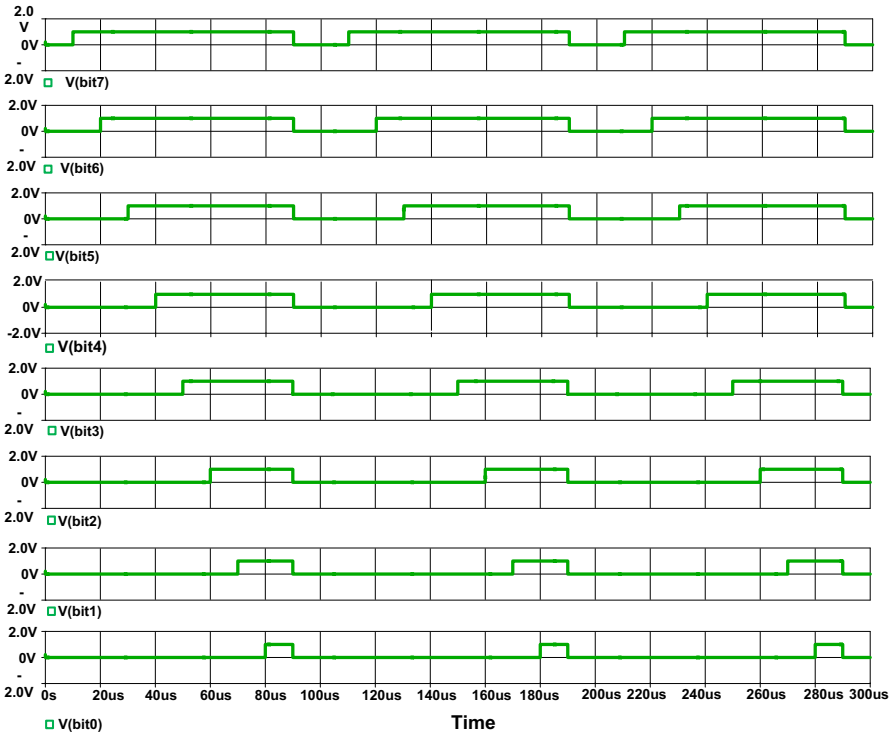


Fig. 11 The SAR controller output when (Load) is HIGH

two outputs of the reconstruction paths. The low-pass filters used in the reconstruction circuit are second-order Sallen-Key filters. The transfer function T(S), radian cutoff frequency (ω_o), and quality factor (Q) of both filters are given, respectively, by the following equations:

$$T(S) = \frac{\frac{K}{R_1 R_2 C_1 C_2}}{S^2 + \left(\frac{1}{R_2 C_1} + \frac{1}{R_1 C_1} + \frac{1-K}{R_2 C_2}\right) S + \frac{1}{R_1 R_2 C_1 C_2}} \tag{10}$$

$$\omega_o = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}, \text{ and } Q = \frac{1}{\left(\sqrt{\frac{R_1 C_2}{R_2 C_1}} + \sqrt{\frac{R_2 C_2}{R_1 C_1}} + (1-K)\sqrt{\frac{R_1 C_1}{R_2 C2}}\right)} \tag{11}$$

The aspect ratios of the S/H circuits along with the values of the resistors and the capacitors of the low-pass filters are given in Tables 2 and 3.

The whole SA-ADC circuit and the reconstruction circuit were simulated using TSMC 0.25 μm technology. The ECG signal shown in Fig. 15 with a peak-to-peak amplitude of 511 mV is fed into the input of the SA-ADC. Figure 16 shows the reconstructed P and T waves. Figure 17 shows the reconstructed QRS spike. Figure 18 shows the final reconstructed ECG signal obtained by adding the two outputs of the two reconstruction paths. The reconstructed waveform is consistent with the input

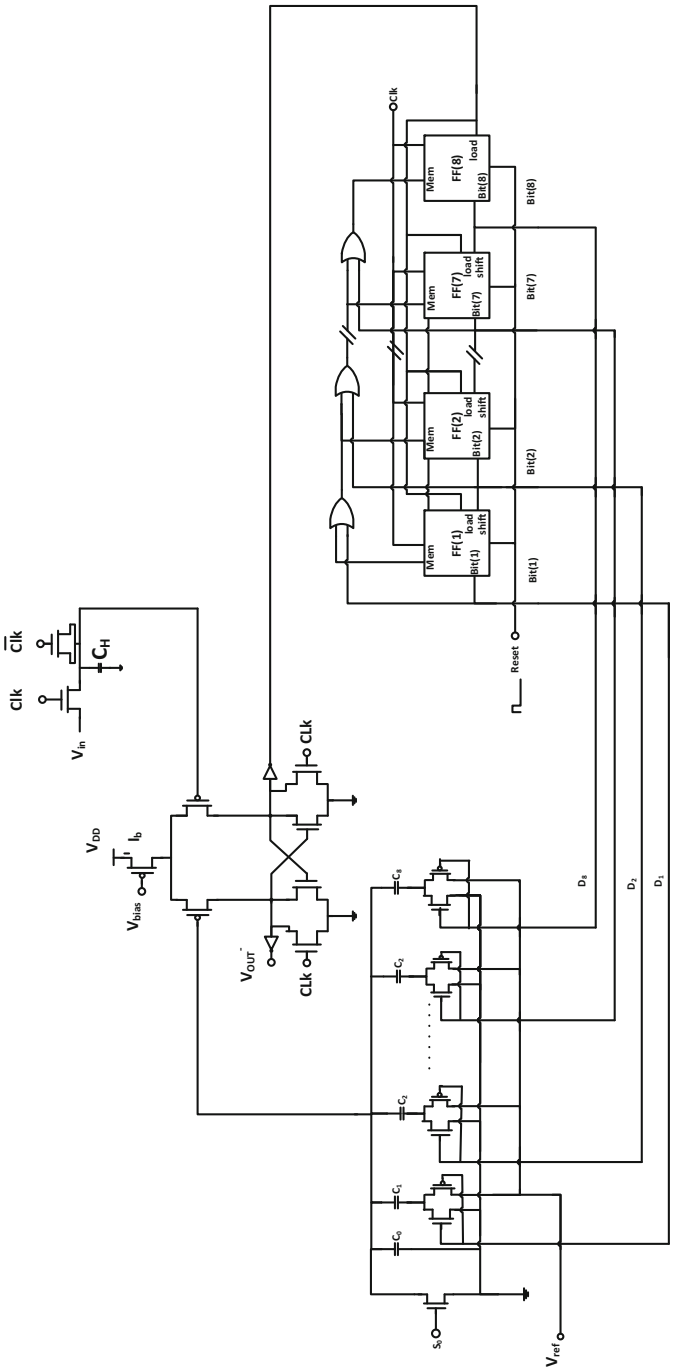


Fig. 12 Schematic of the overall SA-ADC

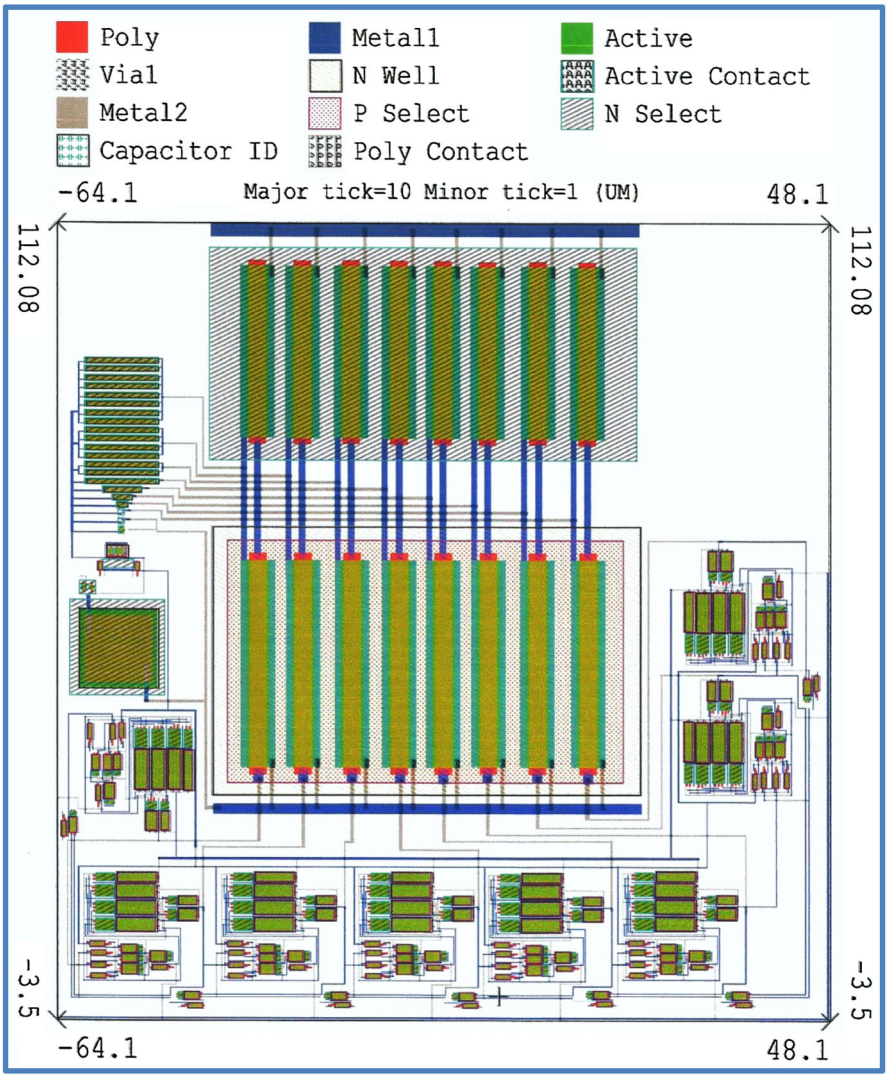


Fig. 13 The ADC circuit's layout

ECG signal. Hence, the 8-bit digital codes of the proposed SA-ADC can be used by a digital signal processor to diagnose the heart activities precisely.

The performance parameters of the SA-ADC such as signal-to-noise ratio (SNR), spurious-free dynamic range (SFDR), and effective number of bits (ENOB) are also measured using FFT of the SA-ADC output for a 200 Hz Sine wave input signal. From the FFT shown in Fig. 19, the SNR, SFDR, and SNDR are about 57, 41, and 40.5 dB, respectively. The ENOB is calculated based on ENOB $= \frac{(\text{SNDR}-1.76)\text{dB}}{6.02\,\text{dB}}$ and is equal to 6.5-bits. One more important parameter of the ADC is the figure of merit (FOM), which is calculated based on the well-known equation:

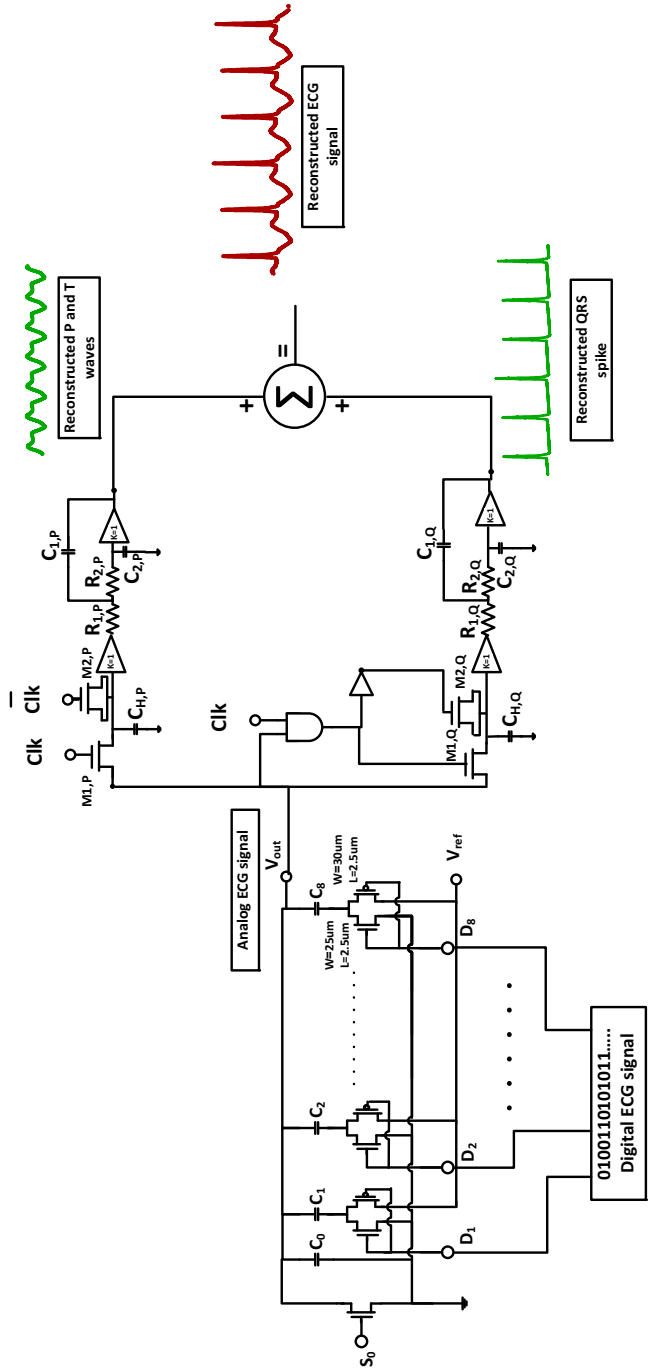


Fig. 14 The proposed ECG reconstruction circuit

Table 2 The S/H circuit and the low-pass filter design values for the P and T waves sections reconstruction block

Component	Dimensions
Sample hold	
$C_{h,p}$	12.5 pF
$M_{1,P}$	$W = 5\,\mu\text{m}$, $L = 0.25\,\mu\text{m}$
$M_{2,P}$	$W = 2.5\,\mu\text{m}$, $L = 0.25\,\mu\text{m}$
Low-pass filter	
$R_{1,p}$	10 KΩ
$R_{2,p}$	10 KΩ
$C_{1,p}$	9 nF
$C_{2,p}$	4.5 nF

Table 3 The S/H circuit and the low-pass filter design values for QRS spike

Component	Dimensions
Sample hold	
$C_{h,Q}$	1.25 pF
$M_{1,Q}$	$W = 5\,\mu\text{m}$, $L = 0.25\,\mu\text{m}$
$M_{2,Q}$	$W = 2.5\,\mu\text{m}$, $L = 0.25\,\mu\text{m}$
Low-pass filter	
$R_{1,Q}$	1 KΩ
$R_{2,Q}$	1 KΩ
$C_{1,Q}$	9 nF
$C_{2,Q}$	4.5 nF

$$\text{FOM} = \frac{\text{power}}{2^{\text{ENOB}} \times 2 \times \text{ERBW}} \tag{12}$$

The figure of merit depends on the power, the ENOB, and the effective resolution bandwidth (ERBW), which is the frequency where the performance of the ADC drops by 0.5-bit. The ERBW is obtained by increasing the frequency of the input signal gradually and observing the frequency at which the ENOB dropped by 0.5-bit. This frequency is found equal to 1.5 kHz as shown in Fig. 20. Therefore, the FOM can be calculated from Eq. (12) and equal to 6.85 pJ/Conversion step. It is worth noting that the plot of the ENOB in Fig. 20 is obtained by sweeping the input frequency while keeping the sampling frequency constant at 10 kHz. For example, at low frequency (≈200 Hz), the sampling frequency is 25 times the Nyquist rate. However, when the input frequency increases (for example at 1.5 kHz), the sampling frequency will be only 3.3 times the Nyquist rate. This reduction ratio increases harmonics distortion and decreases the signal-to-distortion ratio, and this finally reflects on the ENOB.

Table 4 summarizes the performance of the proposed SA-ADC compared with three other designs reported in the literature. From this comparison, the proposed SA-ADC design achieves performance metrics that are close to or better than the ones achieved by using more advanced technologies.

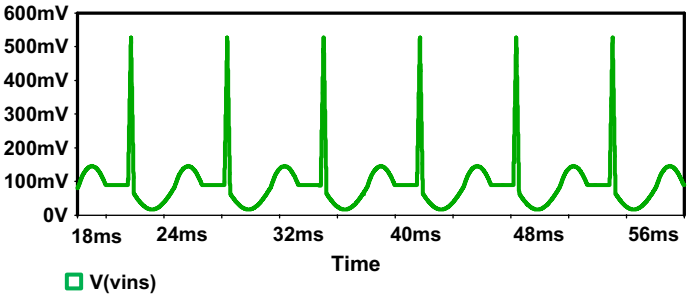


Fig. 15 The ECG input signal to the SA-ADC

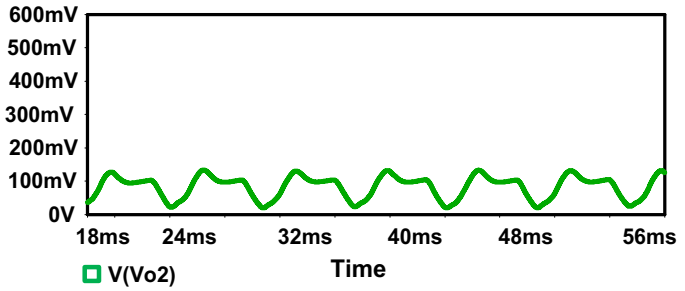


Fig. 16 The reconstructed P and T waves

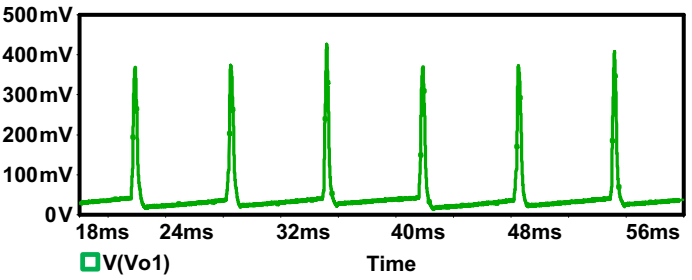


Fig. 17 The reconstructed QRS spike

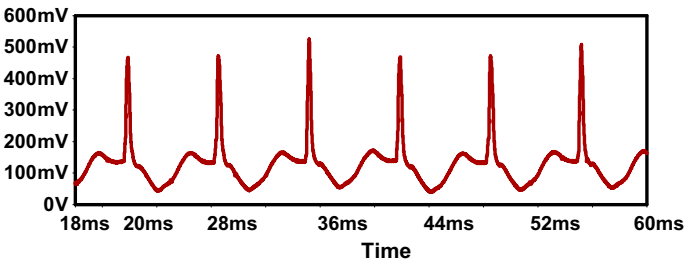


Fig. 18 The final reconstructed ECG

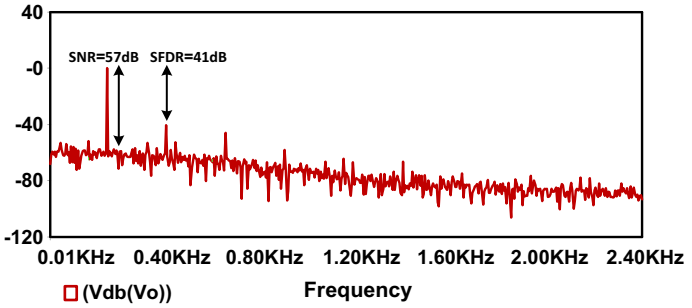


Fig. 19 FFT of the ADC output signal

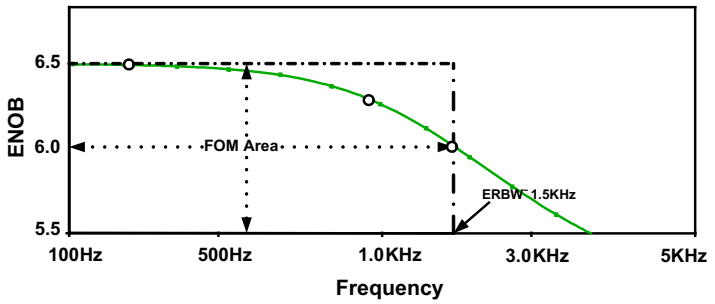


Fig. 20 The effective number of bits (ENOB) versus the input signal frequency at a sampling frequency of 10 kHz

Table 4 Comparison between the design proposed in the work and other reported designs

Technology	This work 0.25 μm CMOS	[9] 0.18 μm CMOS	[5] 0.18 μm CMOS	[6] 0.18 μm CMOS
Supply voltage (V)	1	1	1	1.8
Sampling frequency (samples/s)	10 K	10 K	40 K	70 K
ENOB (bit)	6.5	7.2	9.4	<10
Power consumption (μW)	1.87	0.95	32.6	300
ERBW (Hz)	1.5 K	1 K	300	<2 K
FOM (pJ/conversion step)	6.85	3.23	80.4	>73.2

4 Conclusion

In this paper, an 8-bit SA-ADC with low power, moderate speed, and moderate resolution for ECG detection systems was presented. The SA-ADC has been designed using TSMC 0.25 μm technology. The proposed design achieves performance metrics that are close to or better than the ones achieved by using more advanced technologies. This design consisted of mostly digital circuits in order to lower the power consumption. The simulation results of each of the individual blocks in the SA-ADC were provided. Furthermore, the reconstruction of the ECG signal was realized using two reconstruction paths: one for the QRS spike and the other for the P and T waves.

The reconstructed waveform was consistent with the input ECG signal. Hence, the 8-bit digital codes of the proposed SA-ADC can be processed to diagnose the heart activities precisely.

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