

An Ultra-Low-Power Integrated RF Energy Harvesting System in 65-nm CMOS Process

Lian-xi Liu^{1,2} · Jun-chao Mu¹ · Ning Ma¹ ·
Wei Tu¹ · Zhang-ming Zhu^{1,2} · Yin-tang Yang^{1,2}

Received: 31 August 2014 / Revised: 22 May 2015 / Accepted: 22 May 2015 /
Published online: 3 June 2015
© Springer Science+Business Media New York 2015

Abstract In recent years, radio frequency (RF) energy harvesting systems have gained significant interest as inexhaustible replacements for traditional batteries in RF identification and wireless sensor network nodes. This paper presents an ultra-low-power integrated RF energy harvesting circuit in a SMIC 65-nm standard CMOS process. The presented circuit mainly consists of an impedance-matching network, a 10-stage rectifier with order-2 threshold compensation and an ultra-low-power power manager unit (PMU). The PMU consists of a voltage sensor, a voltage limiter and a capacitor-less low-dropout regulator. In the charge mode, the power consumption of the proposed energy harvesting circuit is only 97 nA, and the RF input power can be as low as -21.4 dBm ($7.24 \mu\text{W}$). In the burst mode, the device can supply a 1.0-V DC output voltage with a maximum 10-mA load current. The simulated results demonstrate that

✉ Lian-xi Liu
adam79416@126.com; lxliu@mail.xidian.edu.cn

Jun-chao Mu
614170947@qq.com

Ning Ma
pfgmaning521@163.com

Wei Tu
tuwei1128@163.com

Zhang-ming Zhu
zhuzhangming@xidian.edu.cn

Yin-tang Yang
ytyang@xidian.edu.cn

¹ Microelectronics School of Xidian University, Xi'an 710071, People's Republic of China

² Key Laboratory of Wide Band-Gap Semiconductor Materials and Devices, Xi'an 710071, People's Republic of China

the modified RF rectifier can obtain a maximum efficiency of 12 % with a 915-MHz RF input. The circuit can operate over a temperature range from -40 to 125 °C which exceeds the achievable temperature performance of previous RF energy harvesters in standard CMOS process.

Keywords RF rectifier · Multistage threshold compensation · Power management unit · Ultra-low-power · RF energy harvesting

1 Introduction

Ambient radio frequency (RF) power signals, from cellular phones and access points (AP), can be an attractive and promising source for harvesting due to their wide availability in urban areas and the amount of power obtainable from these signals. As inexhaustible replacements for internal power sources, RF energy harvesting circuits rely on the extraction of energy from propagating radio waves instead of batteries to supply power to other circuits or systems. These RF energy harvesting systems utilize an antenna as a receiver to collect RF signals (within a certain frequency band) and then convert the collected AC (RF) signal into energy to store in an off-chip capacitor for DC output.

The harvesting process can be divided into two main steps corresponding to the two modes: charge mode and burst mode, respectively. The voltage across the storage capacitor will change between the high threshold voltage (defined as V_{high}) and the low threshold voltage (V_{low}). However, the energy density of RF signals has an inverse square relationship with the distance from the RF transmission source. Under low input power scenarios ($20 \mu\text{W}$ or less), the RF energy can scarcely be scavenged due to the low input voltage, especially for implementation in standard CMOS process. There are two ways to reduce the minimum input energy for a RF energy harvesting system. One way is to improve the sensitivity of the rectifier which is primarily dictated by the threshold voltage of the rectifying devices, and the other way is to minimize the power consumption of the PMU in the charge mode.

Work by Olgun et al. [9] obtained an efficiency of 20 % with a minimum of -20 dBm input power by using low-threshold-voltage Schottky diodes. Nakamoto et al. [8] implemented floating gate devices to preset the biasing voltage at the gates of MOSFETs, and Li et al. [6] used off-chip high impedance resistor networks to provide different DC biasing voltages at the gates of the MOSFETs. Overall, these techniques effectively reduce the threshold voltage of the rectifying devices and improve the sensitivity of the harvester. However, the discrete Si Schottky diodes [9] or the floating gate devices [8] are not fabricated in standard CMOS processes. Moreover, the techniques outlined in [8] and [6] need additional procedures to correctly program the biasing voltages, which will result in rising production costs.

Minimizing the harvester's power consumption in charge mode, either by lowering the high threshold voltage on the off-chip storage capacitor or by reducing the consumption current, is another efficient way to improve the minimum input RF energy. By using bootstrap capacitors to generate a multi-supply, the RF energy harvester presented by Xia et al. [15] achieved -20 dBm input sensitivity. The two-stage boosting

structure was also proposed by Reinisch [13] to lower the input power threshold. The first stage lowers V_{high} and reduces the current in charge mode, and the second stage boosts the output voltage of the former stage by using a charge pump to satisfy the actual application. Papotto et al. [12] obtained -17.1 dBm input sensitivity and 80 nA charge-mode current by using the self-compensation multistage rectifier, which consists of all NMOS transistors with isolated bodies in a deep n-well CMOS process. Due to the internal voltage boosting, more auxiliary circuits and off-chip capacitors are needed in [15] and [13], which will reduce the efficiency and increase the cost. The structure presented in [12] is difficult to apply over a wide temperature range, because of the large variation in the subthreshold string current with the temperature or the process change.

In this paper, an efficient CMOS RF energy harvester is presented. The harvester is based on a modified multistage RF rectifier and an ultra-low-power PMU for an efficient AC–DC conversion. A 10-stage order-2 complementary compensation is introduced in the RF rectifier to eliminate the body effect in standard CMOS processes. The proposed RF harvester can charge the off-chip storage capacitor to 1.6 V with only 97 nA current consumption in the charge mode and output 10 mA current with 1 V DC voltage in the burst mode. The paper is organized as follows: Sect. 2 provides an overview of the proposed RF energy harvester and introduces the impedance-matching network. The block circuits of the harvester are presented and analyzed in detail in Sect. 3. The simulation results based on SMIC 65-nm CMOS process are shown and discussed in Sect. 4, and conclusions are drawn in Sect. 5.

2 Proposed RF Energy Harvesting System

2.1 The Structure of the Proposed RF Energy Harvesting Circuit

The RF energy harvesting system collects RF energy using an antenna. An impedance-matching resonator is used to boost the induced voltage received at the antenna and deliver the maximum power to the RF rectifier. The main purpose of a rectifier is to convert the transmitted RF signal to a DC signal. Moreover, to generate sufficiently high voltage to power other equipment from the ultra-low input power levels, the rectifier also works as a voltage multiplier.

As shown in Fig. 1, the proposed RF energy harvesting system consists of an impedance-matching network (including a RF antenna), a RF rectifier, a voltage sensor, a voltage limiter and a low-dropout (LDO) regulator. All of these blocks are integrated in one chip except for the impedance-matching network and the storage capacitor C_{buffer} . The RF energy is converted into a DC voltage by the RF rectifier and stored in a large off-chip holding capacitor (C_{buffer}). As the RF input power is too small to supply the whole system continuously, the harvester system is designed to be discontinuous and hence has both a charge mode and a burst mode. The voltage sensor detects the voltage on C_{buffer} and generates a control signal to switch between the charge mode and burst mode. In the charge mode, the rectifier will charge the storage capacitor and only the voltage sensor consumes current in the PMU. When the voltage across C_{buffer} rises up to V_{high} , the voltage sensor will wake up the LDO and the voltage limiter and

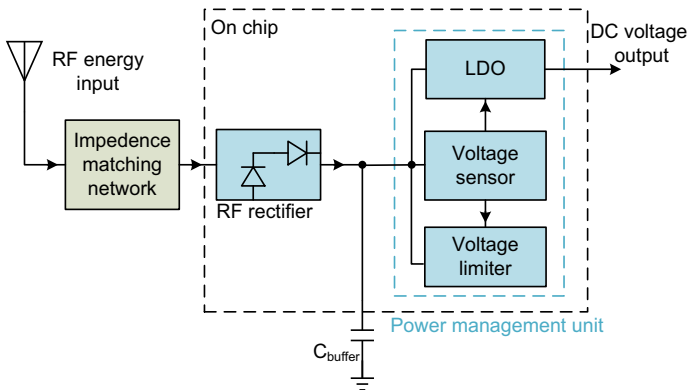


Fig. 1 Block diagram of proposed RF energy harvesting system

the harvester system will switch to burst mode. In this mode, the energy in C_{buffer} will be delivered to the output load by the LDO, and hence the voltage on C_{buffer} drops. The voltage sensor will then shut down the PMU when the voltage on C_{buffer} reduces to V_{low} , and the harvester system then enters the charge mode again.

The voltage limiter aims to protect the whole system if the RF input energy is large or the load current is very small. When the voltage on C_{buffer} reaches the threshold voltage of V_{limiter} , where $V_{\text{limiter}} > V_{\text{high}}$, the voltage limiter will bypass the energy to ground and cause the voltage to drop. As there is a large difference between V_{high} and V_{low} , a LDO regulator is necessary to provide a stable DC output voltage.

2.2 Impedance-Matching Network

As the equivalent impedance of the rectifier mainly varies with the input RF signal power, the impedance-matching network should be optimized considering the rectifier, with the best match chosen when the minimum RF input power is provided. An appropriate impedance-matching network between the antenna and the rectifier can perform a “passive amplification” of the input voltage [6]. Figure 2 shows the equivalent circuit of the AC–DC conversion. The proposed π -type impedance-matching network is optimized for 915 MHz.

As shown in Fig. 2, the antenna can be generally assumed to be a voltage source with a $50\ \Omega$ internal resistance. The RF rectifier can be represented by an equivalent resistor R_1 paralleled with a capacitor C_3 [6]. The equivalent impedance of the rectifier is $0.4\ \text{pF}/1300\ \Omega$ ($\Gamma_{\text{in}} = 0.902 - 0.210j$), which is estimated by circuit simulations. For a more convenient application, off-chip devices are chosen for the impedance-matching network. According to the maximum power transmission theorem, the impedance of the rectifier should be matched to $50\ \Omega$ to obtain the maximum power input. The π -type impedance-matching network optimized at 915 MHz is designed to achieve the impedance matching. At the chip pin, we should be concerned about the parasitic effects [4]. The parasitic inductance at the chip pin is estimated at $1\ \text{nH}/\text{mm}$ and hence can be neglected here [14]. However, the parasitic capacitance

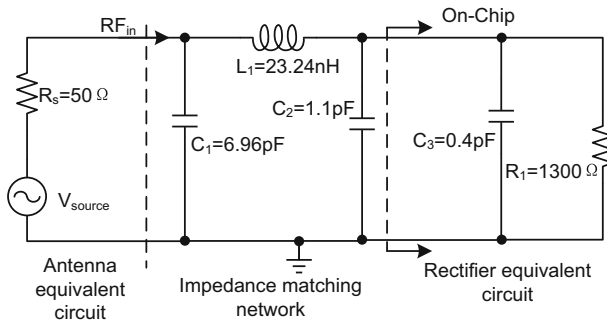


Fig. 2 Equivalent circuit of the AC–DC conversion

can be as large as 0.3 pF [11] and thus must be considered in the design. In order to eliminate the influence of the parasitic capacitance, the capacitor C_2 should be as large as possible, and this is the main reason that the π -type matching structure is used. The impedance-matching network is designed as off-chip and can be flexibly adjusted to reduce the influence of the parasitic effects and improve the performance of the RF energy harvesting system. Importantly, the larger the capacitance of C_2 , the higher the Q value of the matching network. However, high Q values can lead to a narrow bandwidth of this system. In this design, the 1.1 pF C_2 is chosen by setting the Q to 14, and a tradeoff is made between the Q value and the bandwidth.

3 Circuit Design

3.1 Modified RF Rectifier

The RF rectifier proposed by Giuseppe Papotto et al. [11] is based on Dickson's topology [1] and compensates the threshold voltage by connecting the gate to the adjacent stage, which does not need auxiliary bias circuits. Because all of the transistors for [11] are NMOS, a deep n-well process is used to eliminate the body effect. However, this deep n-well process is not suitable in standard CMOS technology.

For the standard CMOS process, the substrate of NMOS must be connected to ground while PMOS is fabricated in an n-well of which the bulk can be individually biased. So the body effect can be eliminated by properly setting the body bias of the PMOS in the RF rectifier. To compensate the threshold voltage, the gate of the PMOS should be connected to a lower potential than that of the source. Therefore, in the Dickson's cascade boosting topology, the gate of PMOS should be biased by the former stage to help lower the threshold voltage. On the contrary, the gate of NMOS in this structure should be biased by the latter stage to compensate the threshold voltage. Based on the previous analysis, a complementary threshold-compensation RF rectifier is proposed to eliminate the body effect in a standard CMOS process. For the sake of simplicity, a 3-stage rectifier with order-1 compensation structure is presented in Fig. 3a. The first stage consists of two NMOS transistors (N_1 , N_2) and two capacitors (C_1 , C_4), and the next two stages are comprised of four PMOS (P_1 – P_4) and four

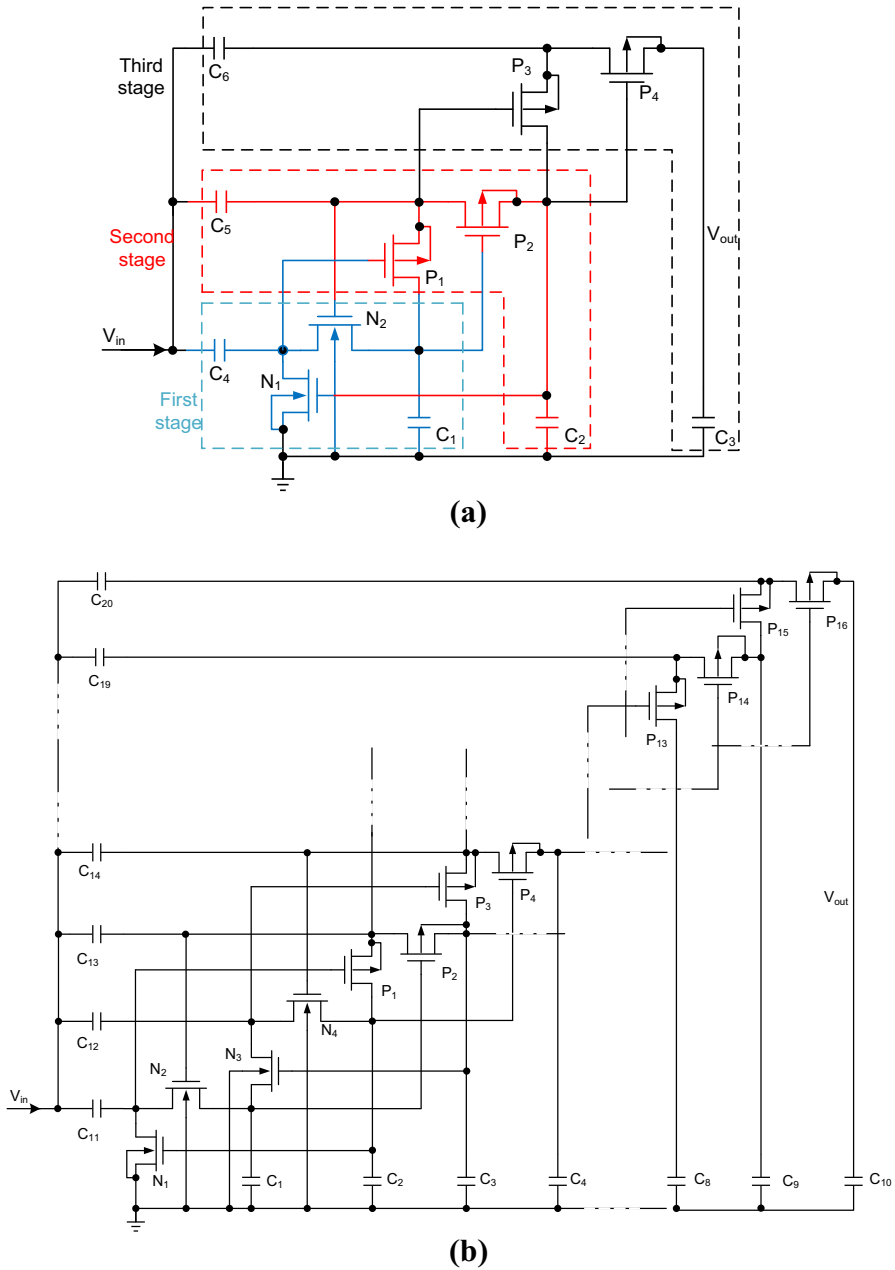


Fig. 3 Complementary threshold-compensation RF rectifier. **a** 3-Stage order-1 structure, **b** the proposed 10-stage order-2 structure

capacitors (C_2, C_3, C_5 and C_6). As the energy density of the RF input is very low, the voltage generated by the first few stages is not high and thus the body effect of the NMOS in these stages can be neglected. As shown in Fig. 3a, the first NMOS stage

and the second PMOS stage provide the bias voltage for each other. Therefore, this structure is called complementary threshold compensation. In the third stage, each PMOS stage is compensated by the adjacent former stage. So it is defined as order-1 compensation.

As the boosting voltage by one stage is not high enough, the greater the order within a certain range, the better the compensation. Moreover to lower the minimum input RF power and obtain a higher output voltage, the number of the whole stages is designed to be large. However, the large orders and stages will lead to a significant decrease in the efficiency. Based on the structure in Fig. 3a, a 10-stage order-2 complementary threshold-compensation RF rectifier is adopted in the proposed energy harvester circuit, as shown in Fig. 3b. The first two stages are made up of NMOS transistors, and the next eight stages comprise of PMOS transistors. The first and the third stage provide the bias voltage for each other, and the second and the fourth stage do the same. After the fifth stage, the bias voltage of the Nth stage is provided by the (N-2)th stage. As mentioned earlier, the body effect of NMOS can be neglected while the body effect of PMOS is eliminated by connecting the substrate to the source. In order to minimize the grounding effect, the ground of the rectifier is separated as a single pad and not connected with the ground of other circuits. With 5 M Ω load and -21.4 dBm RF input power, the proposed rectifier can provide 1.68 V DC output with about 7.7 % efficiency, which is high enough for most applications.

3.2 Low-Power PMU

As analyzed in Sect. 1, lowering the power consumption of the PMU in the charge mode can improve the requirement of the minimum RF input energy. In the charge mode, to ensure the harvester can scavenge energy from the holding capacitor C_{buffer} , the input energy should be larger than the power consumed by the PMU. So the Eq. (1) should be satisfied.

$$P_{\text{in}} \times \eta_{\text{eff}} > V_{\text{buffer}} \times I_{\text{charge}} \quad (1)$$

where P_{in} is the RF input energy, η_{eff} is the conversion efficiency of the rectifier, V_{buffer} is the voltage on the holding capacitor, and the current consumed by the PMU is I_{charge} .

The proposed low-power PMU is shown in Fig. 4 and mainly consists of a voltage sensor, a voltage regulator and a voltage limiter. A long-channel and diode-connected transistor string consisting of M_1 – M_3 is designed as a voltage divider to detect the voltage on C_{buffer} . In the charge mode, the harvested energy from the rectifier causes the voltage on the holding capacitor C_{buffer} to rise gradually. When the voltage on C_{buffer} is lower than V_{high} , the PMOS switch M_4 is turned off to reduce I_{charge} and hence there are only the COMP1, bandgap and bias circuits consuming current in the proposed PMU. When the voltage rises up to V_{high} , the output of COMP1 will change to a high level and then turn on M_4 . Then the comparator COMP2 and the voltage limiter are woke up. At the same time, the output of COMP2 VEN changes to high and enables the voltage regulator. The energy stored in C_{buffer} is converted to stable DC voltage by the LDO, and the whole energy harvester system enters the burst mode.

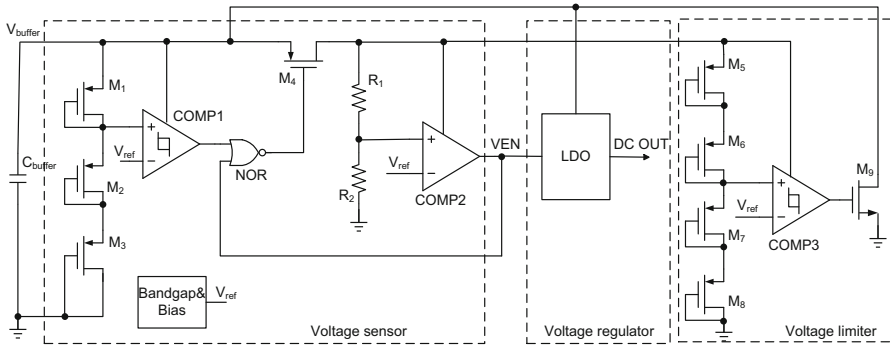


Fig. 4 Proposed PMU

With the power consumption by the PMU, the voltage on C_{buffer} begins to decrease, and then the output of COMP1 will change to low level. However, the VEN remains high at this time, and switch M_4 is still on. When the voltage V_{buffer} drops to V_{low} which is set by the ratio of R_1 and R_2 , the output of COMP2 VEN will change to low, and then the LDO will be shut down and M_4 turned off. Under this condition, the PMU except the COMP1, bandgap and bias circuit stops working. The whole energy harvester system goes into the charge mode again. To prevent the output of COMP1 from oscillation, COMP1 is designed with a 70 mV hysteresis voltage.

Except for the comparator COMP1, bandgap and bias circuits, the other circuits in this proposed PMU work in a discontinuous mode. Overall, this greatly reduces the power consumption in the charge mode. In the circumstances of large RF input signal or low load current demand, the voltage across C_{buffer} can exceed the high threshold voltage V_{high} and attain an unsafe voltage value. When V_{buffer} reaches V_{limiter} (about 2.05 V), the switch M_9 is turned on and draws current from C_{buffer} to ground, thus preventing the PMU from high voltage damage. In this protection mode, the LDO can work continuously and the extra energy is dissipated by the limiter. The detailed working procedure of the PMU is shown in Fig. 5.

3.3 Ultra-Low-Power Bandgap Reference and Nano-ampere Bias

Since the bandgap and bias circuits work in both the charge mode and burst mode, lowering their current consumption means better input sensitivity. This result can be inferred from Eq. (1). Resistor-less voltage reference circuits that operate with ultra-low power have been reported [12]. However, the reference voltage in [12] based on the threshold voltage of MOSFETs is seriously affected by the process. In this paper, an ultra-low-power bandgap reference without resistors is proposed for the RF energy harvester. Based on the structure of [10], the presented bandgap accepts the base-emitter voltage of the bipolar transistor and generates a 1.1-V reference voltage in combination with proportional-to-absolute-temperature (PTAT) voltage generators. Figure 6 shows the schematic of the proposed PTAT voltage generator and the bandgap reference.

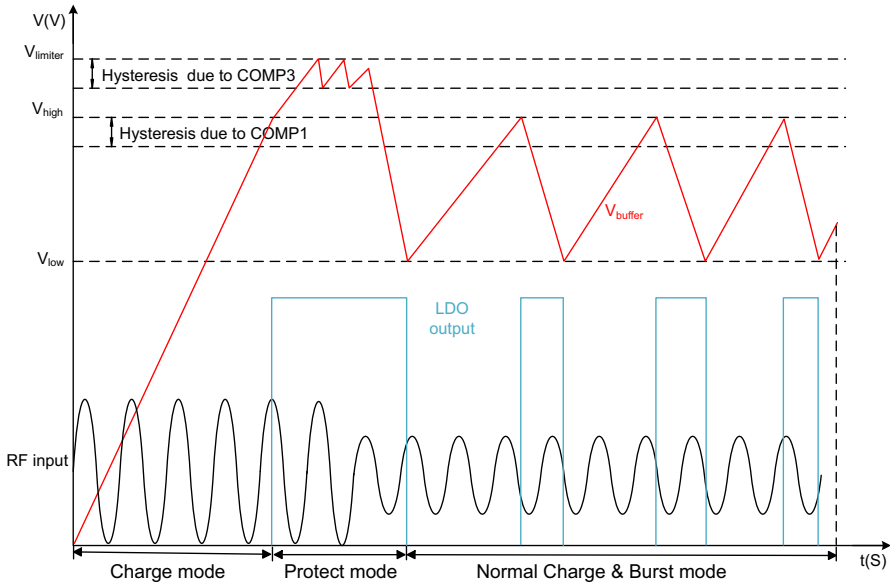


Fig. 5 Operating procedure of the proposed PMU

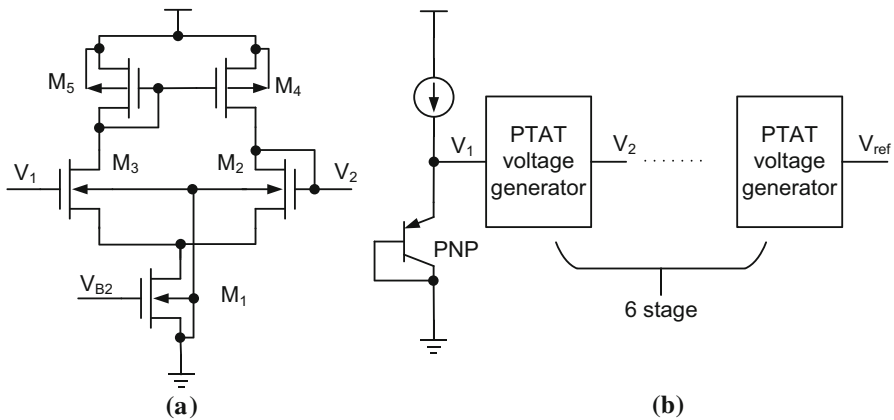


Fig. 6 a PTAT voltage generator, b bandgap reference

As shown in Fig. 6a, all the MOSFETs operate in the subthreshold region. The drain current of the MOSFET in subthreshold can be illustrated by Eq. (2) [10].

$$I = KI_0 e^{\frac{V_{gs} - V_{TH}}{\eta V_T}} \tag{2}$$

where K is the aspect ratio of the transistor, $I_0 (= \mu C_{ox} (\eta - 1) V_T^2)$ is a process-dependent parameter, V_{TH} is the threshold voltage of the transistor, $V_T (= KT/q)$ is the thermal voltage, and η is the subthreshold slope factor. The difference between V_2 and V_1 can be shown using Eq. (3).

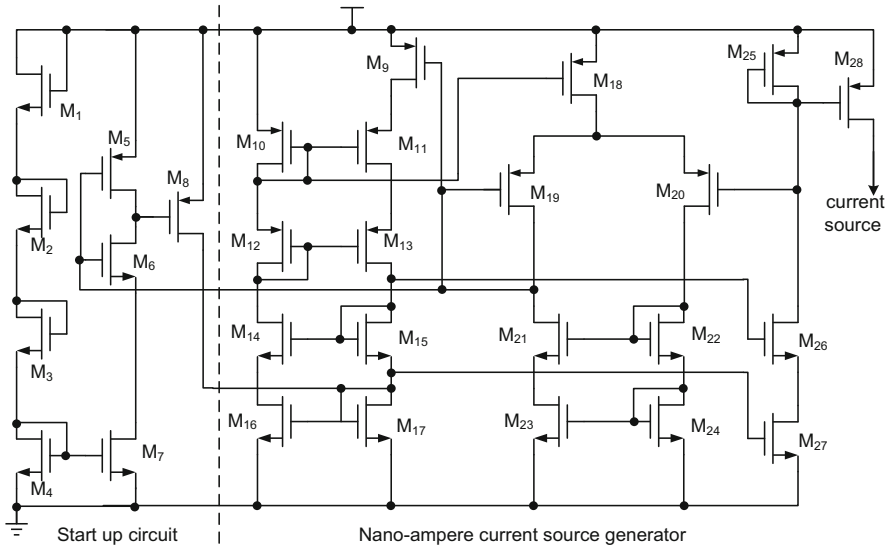


Fig. 7 Schematic of the nano-ampere current source

$$V_2 - V_1 = \eta V_T \ln \frac{I_{M2}(W/L)_{M3}}{I_{M3}(W/L)_{M2}} \tag{3}$$

Obviously, the difference between V_2 and V_1 is a PTAT voltage and this PTAT voltage can be set by changing the bias current and the aspect ratio of M_2 and M_3 . The reference voltage V_{ref} is generated by superimposing the 6-stage PTAT voltage on the V_{BE} of the BJT transistor, as shown in Fig. 6b. The resulting V_{ref} can be illustrated using Eq. (4).

$$V_{ref} = V_{BE} + 6 \times (V_2 - V_1) \tag{4}$$

The power consumption of the bandgap is mainly determined by the bias current which can be as low as several nano-amperes. Generating a current source smaller than 10 nA is another challenge, as the conventional structure such as a Wilson current source is not suitable here. To create the ultra-low current source, the structure presented in [2] is used to generate a 4-nA current source. Figure 7 shows the schematic of the presented ultra-low current source.

The PMOS transistor M_9 in Fig. 7 works in the deep-triode region. So the drain current of M_9 can be expressed as:

$$I_{M9} = \beta_9 (V_{GS9} - V_{TH}) V_{DS9} \tag{5}$$

The aspect ratio of M_{19} and M_{20} is designed differently, and hence the V_{GS9} can be expressed as:

$$V_{GS9} = V_{GS25} + \eta V_T \ln \frac{\beta_{20}}{\beta_{19}} \tag{6}$$

The aspect of M_{10} and M_{11} is also different, and thus V_{DS9} can be expressed as:

$$V_{DS9} = \eta V_T \ln \frac{\beta_{11}}{\beta_{10}} \quad (7)$$

Combining equation (5) with Eqs. (6) and (7), the current I_{M9} can be expressed as:

$$I_{M9} = \beta_9 \eta^2 V_T^2 \ln \frac{I_{M9} \beta_{20}}{I_{0M25} \beta_{19}} \ln \frac{\beta_{11}}{\beta_{10}} \quad (8)$$

where $I_{0M25} = (\mu C_{ox}(W/L)M_{25}V_T^2(\eta - 1))$ is the pre-exponential factor of the subthreshold current. As the MOSFETs work in subthreshold region, the output of the current source can be very low.

3.3.1 Voltage Sensor and Voltage Limiter

The voltage sensor is used to detect the voltage on the holding capacitor C_{buffer} and output control signals. As discussed in the previous analysis in Sect. 2, to lower the input RF power threshold, in the charge mode, the power consumption of the voltage sensor should be as low as possible. However, in the burst mode, there are two facts that will inevitably lead to large current consumptions by the voltage sensor. Firstly, the capacitive load of the voltage sensor is very large because it needs to wake up the whole energy harvester system in the burst mode. Secondly, the rate of fall of the voltage V_{buffer} in the burst mode is faster than its rate of rise in charge mode. Hence, the voltage sensor should exhibit a higher bandwidth for the faster conversion rate in the burst mode. That is to say, the voltage sensor needs different performance requirements in the two operating modes.

Two comparators with different characteristics are introduced in the proposed voltage sensor as shown in Fig. 4. The low-power comparator COMP1 is used to detect the high threshold voltage V_{high} on the holding capacitor in the charge mode, while the high-performance comparator COMP2 senses the low threshold voltage V_{low} in the burst mode. Importantly, in the charge mode, COMP2 is shut down completely to ensure that ultra-low-power consumption is possible. The COMP2 with higher bandwidth and higher gain needs a large bias current and works only in the burst mode to achieve a faster transient response. In addition, the use of the two comparators can also increase the accuracy of the detecting threshold voltage. It is worth mentioning that the current consumption of COMP2 is not taken into account in the proposed design example, since it is much lower than that of the regulator in the burst mode. To prevent the output of COMP1 from oscillation, a little hysteresis voltage is introduced in the design of COMP1.

Figure 8a presents the schematic of the low-power hysteresis comparator COMP1. As the rise rate of the voltage across C_{buffer} is very small for the charge mode, the current consumption of COMP1 can be as low as tens of nano-ampere. By setting the aspect ratio of M_4 and M_5 larger than M_6 and M_7 , respectively, a hysteresis voltage can be generated between the input V_{in+} and V_{in-} . The schematic of the high-performance comparator COMP2 is shown in Fig. 8b, and the classical two-stage structure is applied

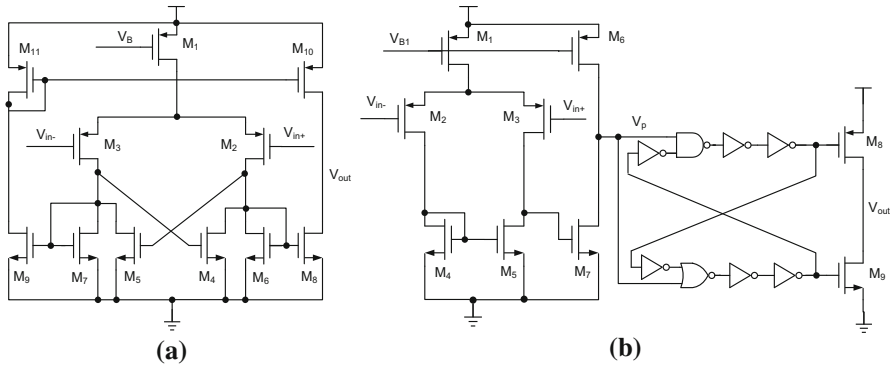


Fig. 8 **a** Schematic of low-power comparator COMP1, **b** the circuit of schematic of high-performance comparator COMP2

to the presented design to get a wide bandwidth. A logic circuit with positive feedback is used in the COMP2 to accelerate the output change. By increasing the bias current, a high gain (more than 60 dB) can be obtained easily and consequently the gain error of COMP2 can be neglected in the burst mode.

In the proposed voltage sensor, the voltage divider is made up of a strong-inversion diode-connected transistor string. As mentioned above, reducing the current consumption should be taken into account carefully in the voltage divider design. In [11], the current consumption of the divider is reduced by increasing the number of diode-connected MOSFETs in the string and making these transistors operate in the subthreshold region. However, the subthreshold current of a MOSFET varies exponentially with the threshold voltage V_{TH} , as illustrated in Eq. (2). Unfortunately, the threshold voltage V_{TH} of a MOSFET in standard CMOS technology is greatly affected by the variations in the process and the temperature. On the contrary, the threshold voltage V_{TH} has a negligible effect on the saturation current of the MOSFET. Therefore, we can reduce the number of MOSFETs in the diode-connected transistor string to ensure these transistors all operate in the saturation region, and extend the channel length of the MOSFETs to reduce the current consumption in this design example. The leakage current of a MOSFET in the non-saturation region is very small, and thus the current consumption of the transistor string operating in the non-saturation region can be neglected.

The comparator in the voltage limiter COMP3 is the same as COMP1, while the hysteresis voltage is slightly larger than that of COMP1. When the voltage of V_{buffer} reaches $V_{limiter}$ (2.05 V), COMP3 will turn on the switch M_9 and bypass the extra current from C_{buffer} to ground, thus preventing the PMU from high voltage damage. A strong-inversion diode-connected transistor string is made up of M_5 – M_8 as shown in Fig. 4 and plays the same role as the divider in the voltage sensor.

3.3.2 Cap-Less LDO

To provide a stable DC voltage output and reduce the application costs, a capacitor-less LDO is applied to the presented PMU to achieve DC–DC conversion, of which the

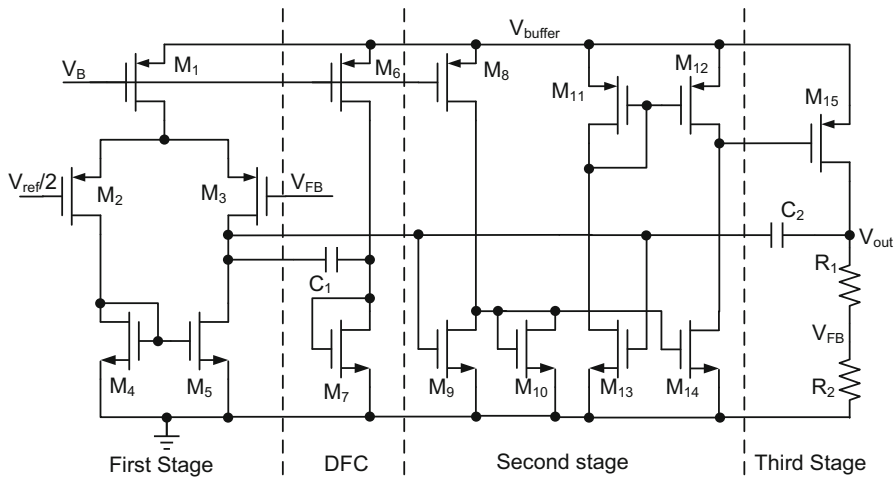


Fig. 9 Cap-less regulator

schematic is shown in Fig. 9. The proposed cap-less LDO is based on three gain stages with a damping-factor-control (DFC) compensation [5]. Thanks to the low threshold voltage in the 65-nm CMOS process, the transistors of the differential input pair, M_2 – M_3 , can work with a gate voltage as low as 0.55 V (about $V_{ref}/2$). Current source M_6 , diode-connected transistor M_7 and capacitor C_1 constitute the DFC compensation stage. Transistors M_8 , M_9 and M_{10} convert the single-ended current coming from the output of the first stage into a differential voltage signal. A current mirror consisting of M_{11} – M_{12} and transistors M_{13} – M_{14} amplify the differential signal and then convert it into a single-ended voltage, while also performing the second gain stage. M_{15} provides the third-stage gain to power the overall output load. With 10 mA output current and 0.25 V dropout voltage, the simulated voltage regulator has a quiescent current of only 14 μ A.

As a final remark, it should be mentioned that the leakage current of M_{15} can additionally be taken into account in the design of the regulator if a large load current (>5 mA) is required. The large leakage current will lead to an efficiency decrease of the rectifier and the input sensitivity deterioration of the harvesting system. However, this is not really necessary for the proposed design example, as the maximum 10-mA output current meets most wireless sensor network node (WSNN) applications.

4 Simulation Results

The proposed ultra-low-power integrated RF energy harvesting system is implemented and simulated with the SMIC 65-nm standard CMOS process. The layout of the proposed RF energy harvesting system is shown in Fig. 10. The area costs of the whole chip and the core circuit are about 0.54×0.44 mm² and 0.35×0.25 mm², respectively. The RF rectifier is surrounded by guard rings to isolate it from adjacent cells. The ground of the RF rectifier is separated as a single pad (RF ground as shown in

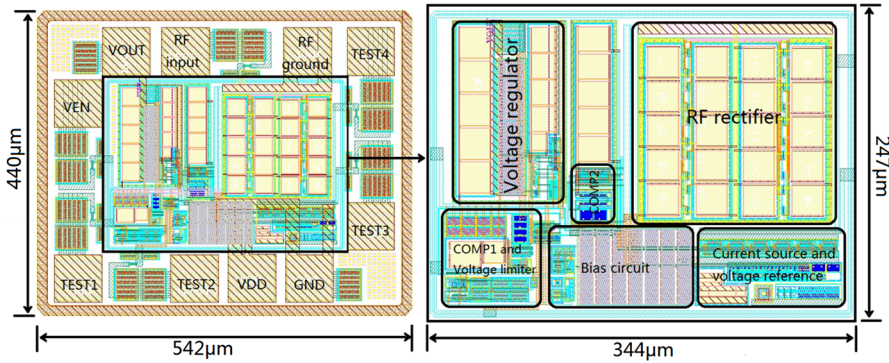


Fig. 10 Layout of the proposed RF energy harvesting system

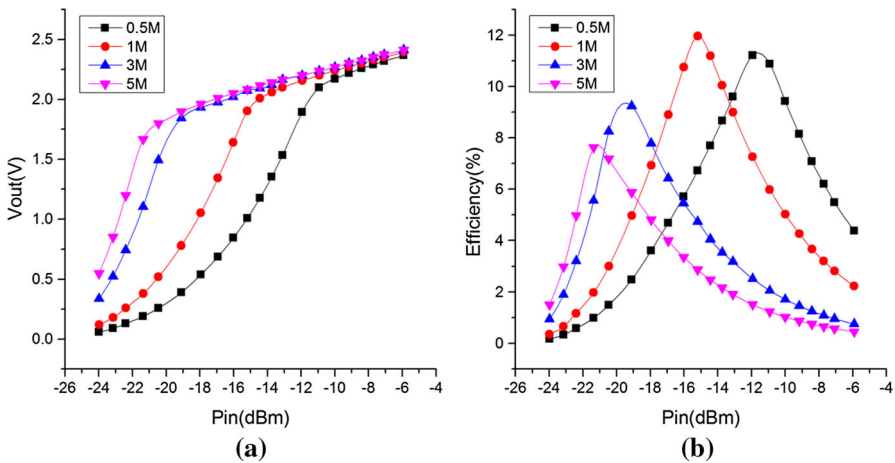


Fig. 11 Rectifier simulation results ($f = 915$ MHz, single-tone CW input). **a** Output DC voltage versus available input power, **b** PCE versus available input power

Fig. 10) and is not connected with the ground of other circuits. The parasitic parameters of the system are extracted to the post-layout simulation for more accurate results.

The simulation performances of the proposed 10-stage order-2 compensation RF rectifier are shown in Fig. 11; this circuit is simulated with a single-tone continuous-wave (CW) $50\ \Omega$ input source at the nominal frequency of 915 MHz. Figure 11a shows the output DC voltage of the rectifier as a function of the available input power for different load resistances ranging from 0.5 to 5 M Ω . The modified RF rectifier exhibits a quite low input power threshold and is able to supply a 1.68-V output voltage with a 5 M Ω resistive load when the available input power is as low as -21.4 dBm ($7.24\ \mu\text{W}$). When loaded with a 1 M Ω resistance, the circuit can deliver the nominal output voltage of 1.05 V with an available input power of -18 dBm ($16\ \mu\text{W}$). The power conversion efficiency (PCE) of the rectifier is reported in Fig. 11b as a function of the available input power for different load resistances. Under nominal conditions (1.05 V output on a 1 M Ω load), the circuit attains a PCE

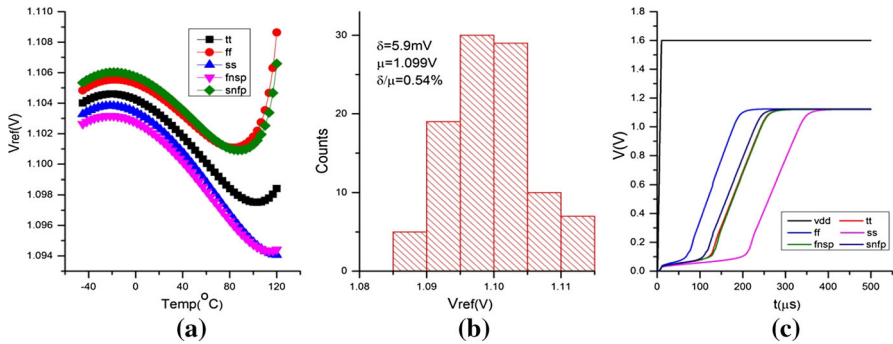


Fig. 12 Bandgap reference simulation results. **a** Simulated voltage of the reference versus temperature in different corners, **b** distribution of the reference voltage, **c** transient simulation results of the bandgap with 1.6 V supply voltage

about of 6.9%. With a 1 M Ω load, the maximum PCE is about 12% at -15.2 dBm RF input power and the performance of the rectifier exceeds the previous works in a standard CMOS process.

Figure 12a plots the simulation voltages of the proposed bandgap reference as a function of temperature from -40 to 125 °C in different process corners. The average temperature coefficient (TC) is about 33 ppm/°C thanks to the technique of curvature compensation as explained in Sect. 2. In order to evaluate the robustness to process variations, Monte Carlo SPICE simulations were performed on the bandgap reference. The results for 100 runs are depicted in Fig. 12b. The coefficient of variation ($=\sigma/\mu$, where σ and μ are the standard deviation and the mean value) in the simulation results is 0.54%. The coefficients of variation are very small as the proposed circuit is based not on the threshold voltage of MOSFETs, but on the bandgap voltage of the silicon. As shown in Fig. 12c, with a 1.6-V supply voltage, the output of the bandgap is about 1.1 V in different process corners. Due to the low current consumption, the setup time of the bandgap is about 400 μs and is much less than the charging time of the off-chip holding capacitor.

Figure 13a plots the output currents of the proposed nano-ampere current source as a function of temperature from -40 to 125 °C in different process corners. The output current is proportional to the absolute temperature, and the slope is almost the same (about 0.014 nA/°C) in each corner. The Monte Carlo simulation results for 100 runs are shown in Fig. 13b. The coefficient of variation for the output current is 11.52%. Although the relative change is large with process variations, it has little influence on the harvester system because the absolute value of the output current is very small. Figure 13c shows the transient simulation results of the current source with a 1.6-V supply voltage in different corners. The overshoot during start-up is very small, and the deviation from the different corners is less than ± 5.8 %.

As shown in Fig. 14a, the hysteresis voltage of COMP1 is nearly 70 mV. It is worth mentioning that this hysteresis voltage will be amplified by the divider. So the hysteresis voltage of V_{high} is about 100 mV, when the typical value of V_{high} is set as 1.6 V. To reduce the current consumption in charge mode, the current of COMP1 is

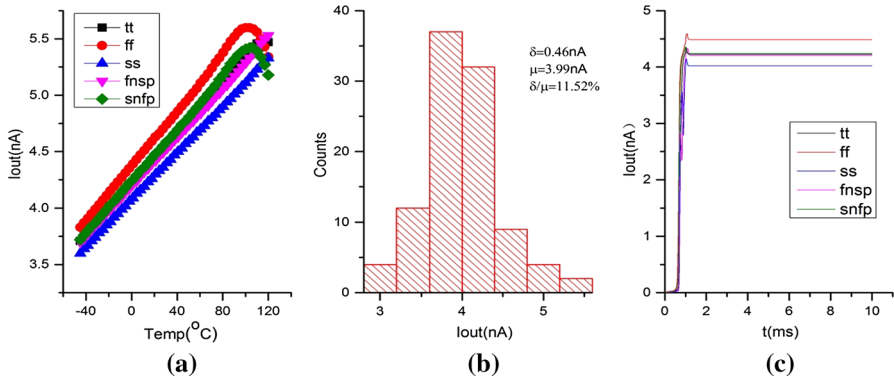


Fig. 13 Nano-ampere current source simulation results. **a** Output current versus temperature in different corners, **b** distribution of the output current, **c** transient simulation results of the current source with a 1.6-V supply voltage

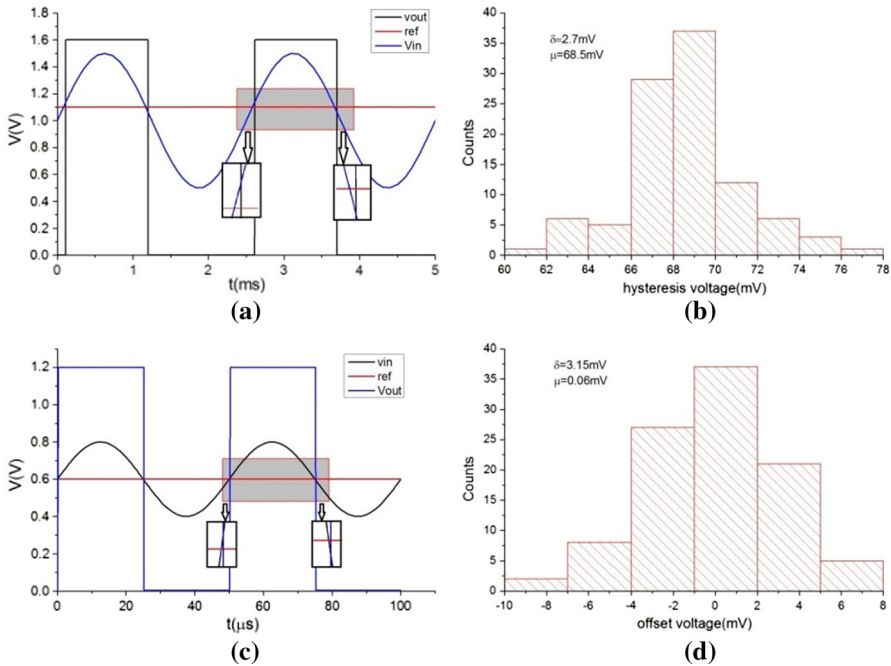


Fig. 14 **a** Transient response of COMP1, **b** Monte Carlo simulation result for hysteresis voltage of COMP1, **c** transient response of COMP2, **d** Monte Carlo simulation result for the offset voltage of COMP2

just 16 nA. Figure 14b presents the Monte Carlo simulation results for 100 runs for the hysteresis voltage of COMP1. The mean value (μ) of the hysteresis voltage is 68.5 mV with the standard deviation (σ) of 2.7 mV. Even with 3σ variation, the possible spread of the hysteresis voltage in COMP1 is sufficiently small, and so it has a negligible influence on the performance of the energy harvester. COMP2 is used to detect the

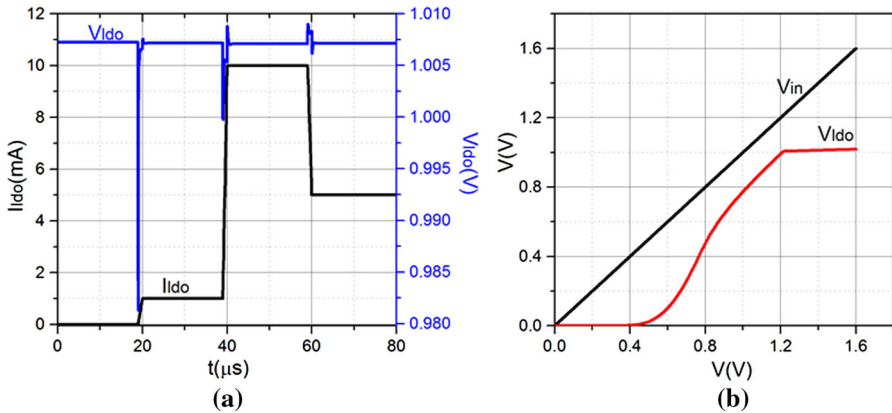


Fig. 15 **a** Load transient response of the proposed LDO, **b** line regulation simulation of the proposed LDO

low threshold voltage on the holding capacitor without the hysteresis voltage, and its performance can be seen in Fig. 14c. Due to the high gain of the two-stage structure, the gain error of COMP2 can be neglected. The offset voltage is the dominant factor in the accuracy of the comparator COMP2. To investigate the effect that this offset voltage has on the harvester, Fig. 14d presents 100 Monte Carlo simulation results for the offset voltage of COMP2. As shown in Fig. 14d, the offset voltage of COMP2 is only about 9.5 mV (3σ). When setting V_{low} to 1.25 V, it can be calculated that V_{low} has a change of ± 10.8 mV due to the offset voltage of COMP2 and this change is very small compared with the previous work [12, 13]. The current bias of COMP2 is set to $3\ \mu\text{A}$ to meet the requirements of the high output slew rate and the large load capacitor.

Figure 15a presents the load transient response of the proposed cap-less LDO under the condition of 1.25 V input voltage. The proposed LDO can output 1 V DC voltage with a maximum 10-mA current. The simulation was performed at the minimum dropout voltage 250 mV and the output current (rise/fall time = $1\ \mu\text{s}$) varied from 0 to $100\ \mu\text{A}$, then to 10 mA and back again to 5 mA. As expected, the output voltage fluctuated when the load current changed. As shown in Fig. 15a, the output variation of the proposed LDO is no more than 20 mV with the current change in $1\ \mu\text{s}$. Figure 15b shows the simulation result of the line regulation of the LDO with a 10-mA load. The output voltage changes about 12 mV when the input voltage changed from 1.25 to 1.6 V and the line regulation is about 1.2%.

Figure 16 plots the current consumption of the proposed PMU with the voltage changing on the holding capacitor in the charge mode. The PMU exhibits an extremely low current consumption of 97 nA at 1.6 V of V_{buffer} during the charge mode. This low current consumption reduces the load effect of the PMU and improves the charging rate of the harvester.

As the off-chip holding capacitor is very large and the frequency of the input RF signal is also very high, co-simulating both the PMU and rectifier using SPICE tools is very difficult. An equivalent current source model is used in the simulation to replace

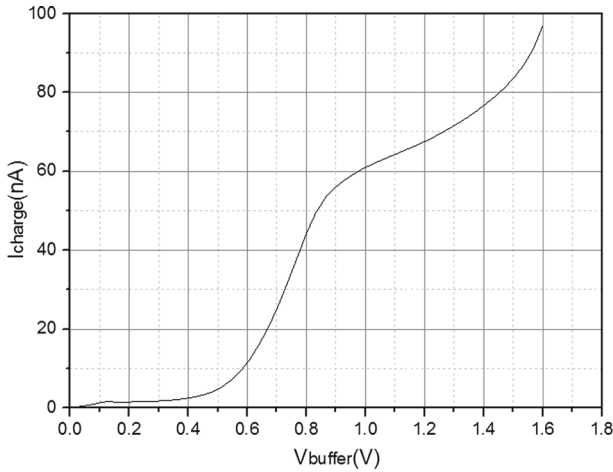


Fig. 16 PMU current consumption versus V_{buffer} during the charge mode

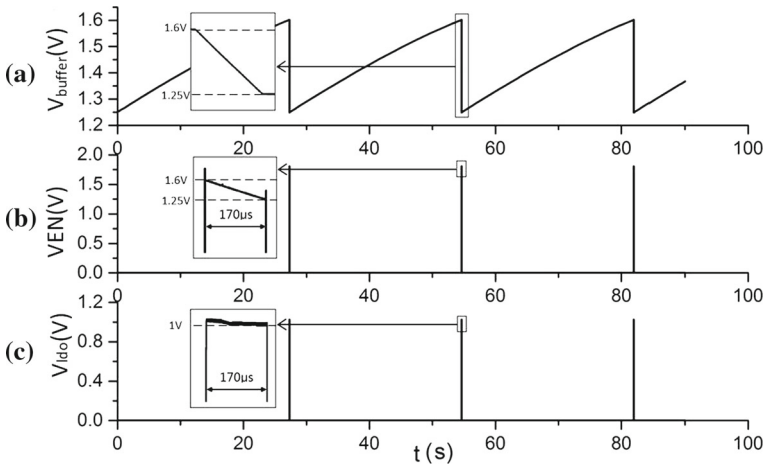


Fig. 17 Simulation results of the proposed RF energy harvester

the rectifier. To prove that the proposed PMU can work at ultra-low input power, the current source is set as 150 nA. The simulation results of the proposed RF energy harvester in the normal charge and burst mode are shown in Fig. 17.

A 4.7- μF storage capacitor was used for simulation. This capacitor results in a charging time of about 30 s under minimum input power and provides an operating time of 170 μs when the system outputs 1 V DC voltage with 10-mA load current. To accelerate the simulation, the initial voltage of the off-chip storage capacitor is set as 1.25 V, and the maximum simulation step is set as 1 μs . To obtain long system operating time and a large load current, a large off-chip holding capacitor is needed. In the proposed harvester system, the voltage across the storage capacitor C_{buffer} is restricted between V_{high} (1.6 V) and V_{low} (1.25 V), as shown in Fig. 17a. The control

Table 1 Current consumption of the proposed PMU

Block	Current consumption	
	Charge mode (nA)	Burst mode (μ A)
COMP1 and divider	28	–
Bandgap reference	28	–
PTAT current source	16	–
Leakage current of power MOSFET	25	–
COMP2	–	3
Voltage limiter	–	3
Voltage regulator	–	14
Total	97	20

signal VEN of the LDO is in the high level in the burst mode, and it follows the supply voltage V_{buffer} , as shown in Fig. 17b. Figure 17c plots the output voltage of the LDO, which is a stable DC 1 V in the burst mode. As shown in the simulation results of the rectifier above, the proposed rectifier can output 1.68 V with $5\text{M}\Omega$ load at -21.4 dBm RF input, which means that the maximum current consumption in charge mode can be up to 336 nA. We provide the current margin of about 240 nA ($=336-97\text{ nA}$) to take into account the variations in the process and temperature. The nominal current consumptions of the PMU building blocks are summarized in Table 1.

The RF energy harvester performance is summarized and compared with previously published state-of-the-art works in Table 2. The proposed RF energy harvester system exhibits an excellent sensitivity of -21.4 dBm due to both the extremely low charge-mode current consumption (97 nA) and the reduced input power threshold achieved by the adopted complementary self-compensated rectifier.

5 Conclusion

This paper proposed a 915-MHz RF energy harvester system based on SMIC 65-nm standard CMOS process. The circuit includes an improved multistage self-compensated rectifier and an ultra-low-power PMU. It exploits the threshold voltage compensation and low charge-mode current consumption techniques to reduce the input sensitivity as low as -21.4 dBm . Moreover, comparators with different performance characteristics are used in different modes to achieve accurate control on the voltage across the holding capacitor without increasing the power consumption. Due to the low-power voltage regulator with DFC compensation, the proposed harvester can output 1 V DC voltage and 10 mA current for other portable or battery-less devices. By reducing the number and extending the channel length of the diode-connected transistors in the divider, a good robustness to process variations and a wide operating temperature range are achieved. The disclosed technical details can provide valuable guidelines for the power-aware circuit design and can be exploited for the implementation of future RF-powered wireless sensor networks.

Table 2 Energy harvester performance and comparison with prior art

Reference	Charge mode	Burst mode	Holding capacitor	Process	Output	Input sensitivity	Temperature range
[3] ^{mea}	995 nA	N/A	N/A	0.5 μm^{S}	N/A	-17.8 dBm	N/A
[13] ^{mea}	172 nA	N/A	20 μF + 2 μF	0.13 μm	1.5 V/9.6 mA	-19.7 dBm	-40 to 125 °C
[7] ^{mea}	N/A	N/A	5 nF	0.18 μm	1 V	-17 dBm	N/A
[15] ^{mea}	> 300 nA	N/A	10 μF + 1 μF + 10 nF	65 nm	0.6 V	-20 dBm	N/A
[12] ^{mea}	80 nA	100 μA	100 nF	90 nm ^D	1 V/1 mA	-17.1 dB	-40 to 85 °C
This work ^{sim}	97 nA	20 μA	4.7 μF	65 nm	1 V/10 mA	-21.4 dBm	-40 to 125 °C

0.5 μm^{S} , Schottky diode used; 90 nm^D, deep n-well used; [X]^{mea}, measured results; This work^{sim}, simulation results

Acknowledgments This work was supported by the National Natural Science Foundation of China (61376033, 61322405, and 61306044) and the National High-tech Program of China (2013AA014103).

References

1. J.F. Dickson, On-chip high-voltage generation in NMOS integrated circuits using an improved voltage multiplier technique. *IEEE J. Solid State Circuits* **11**(3), 374–378 (1976)
2. T. Hirose, Y. Osaki, N. Kuroki, M. Numa, A nano-ampere current reference circuit and its temperature dependence control by using temperature characteristics of carrier mobilities. In: *Proceedings of the ESSCIRC* (2010), pp. 114–117
3. U. Karthaus, M. Fisher, Fully integrated passive UHF RFID transponder IC with 16.7 μ W minimum RF input power. *IEEE J. Solid State Circuits* **38**(10), 602–1608 (2003)
4. T. Le, K. Mayaram, T. Fiez, Efficient far-field radio frequency energy harvesting for passively powered sensor networks. *IEEE J. Solid State Circuits* **43**(5), 1287–1302 (2008)
5. K.N. Leung et al., Analysis of multistage amplifier–frequency compensation. *IEEE Trans. Circuit Syst. I* **48**(9), 1041–1056 (2001)
6. B. Li et al., An antenna co-design dual band RF energy harvester. *IEEE Trans. Circuits Syst. I* **60**(12), 3256–3266 (2013)
7. H.O. Mahmoud et al., 5.2-GHz RF power harvester in 0.18- μ m CMOS for implantable intraocular pressure monitoring. *IEEE Trans. Microw. Theory Tech.* **61**(5), 2177–2184 (2013)
8. H. Nakamoto, D. Yamazaki, T. Yamamoto, H. Kurata, S. Yamada, K. Mukaida, T. Ninomiya, T. Ohkawa, S. Masui, K. Gotoh, A passive UHF RFID Tang LSI with 36.6 % efficiency CMOS-Only rectifier and current-mode demodulator in 0.35 μ m Fe-Ram technology. In: *Proceedings of IEEE ISSC Conference* (2006), pp. 1201–1210
9. U. Olgun, C. Chi-Chih, Investigation of rectenna array configurations for enhanced RF power harvesting. *IEEE Antennas Wirel. Propag. Lett.* **10**, 262–265 (2011)
10. Y. Osaki, T. Hirose, N. Kuroki, M. Numa, 1.2-V supply, 100-nW, 1.09-V bandgap and 0.7-V supply, 52.5-nW, 0.55-V sub bandgap reference circuits for nano watt CMOS LSIs. *IEEE J. Solid State Circuits* **48**(6), 1530–1538 (2013)
11. G. Papotto et al., A 90-nm CMOS threshold-compensated RF energy harvester. *IEEE J. Solid State Circuits* **46**(9), 1985–1997 (2011)
12. G. Papotto et al., A 90-nm CMOS 5Mbps crystal-less RF-powered transceiver for wireless sensor network nodes. *IEEE J. Solid State Circuits* **49**(2), 335–346 (2014)
13. H. Reinisch et al., An electro-magnetic energy harvesting system with 190 nW idle mode power consumption for a BAW based wireless sensor node. *IEEE J. Solid State Circuits* **46**(7), 1728–1741 (2011)
14. A. Shameli, A. Safarian, A. Rofougaran, M. Rofougaran, F. De Flaviis, Power harvester design for passive UHF RFID tag using a voltage boosting technique. *IEEE Trans. Microw. Theory Tech.* **55**(6), 1089–1097 (2007)
15. L.L. Xia et al., 56 V, -20 dBm RF-powered, multi-node wireless body area network system-on-a-chip with harvesting-efficiency tracking loop. *IEEE J. Solid State Circuits* **49**(6), 1345–1355 (2014)