

Design and Evaluation of CNFET-Based Quaternary Circuits

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Abstract This paper presents novel high-performance and PVT tolerant quaternary logic circuits as well as efficient quaternary arithmetic circuits for nanoelectronics. These Carbon Nanotube FET (CNFET)-based circuits are compatible with the recent technologies and are designed based on the conventional CMOS architecture, while the previous quaternary designs used methods which are not suitable for nanoelectronics and have become obsolete. The proposed designs are robust and have large noise margins and high driving capability. The singular characteristics of CNFETs, such as the capability of having the desired threshold voltage by regulating the diameters of the nanotubes, make them very appropriate for voltage-mode multiple-threshold circuits design. The proposed circuits are examined, using Synopsys HSPICE with the standard 32 nm-CNFET technology in various situations and different supply voltages. Simulation results demonstrate the correct and high-performance operation of the proposed circuits even in the presence of process, voltage and temperature variations.

Keywords Carbon nanotube FET (CNFET) · Quaternary logic · Arithmetic and logic circuits · Multiple- V_{th} design · Nanoelectronics

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1 Introduction

The present level of sophistication and application of the binary (two-valued) logic is reached mainly on account of the inherent two-state switching behavior of the efficient microelectronic devices. In addition, many powerful arithmetical components and tools have already supported the binary logic to reach its present status. However, the main problems in the binary integrated circuits of the present time are on-chip and off-chip (pin-out) interconnection problems. The first problem causes difficulties in placement and routing of the logic elements and also very large silicon area used for the interconnections. In addition, the second problem restricts the number of connections of an integrated circuit with the external world and is critical in the packaging process. Moreover, implementing many complex applications such as estimation and analysis procedures, process control and decision systems are not either advantageous or even feasible in binary logic. To overcome these physical and electrical problems, digital systems with radices greater than two and accordingly multiple-valued logic (MVL) should be considered. MVL systems permit more than two levels of logic and depending on the number of permitted logic levels, ternary (three-valued) or quaternary (four-valued) logic systems can be considered. It is worth mentioning that the quaternary logic takes advantage of simple conversion between quaternary signals and binary signals, generated by the existing binary circuits. Using MVL instead of binary logic raises the information content per interconnection which results in saving in the number of interconnection wires and in the insulation between them. Furthermore, pins carry more information which results in saving in the number of pins. In addition, it leads to chips with less complexity, more density, more data processing capabilities per unit area and very high-bandwidth serial and parallel data transfer [7, 9, 24]. From the mathematical aspect, redundant and residue number systems permit to decrease or eliminate the rippling carries resulting in more high-speed arithmetic operations than normal binary logic [7]. MVL can be even utilized to resolve the binary problems more efficiently. For example, a third logic value can be used as a medium for signaling the faulty operation in testing the binary circuits [7]. The most common and energy-efficient method for designing MVL circuits is CMOS voltage-mode multiple-threshold (multiple- V_{th}) design [17]. However, it leads to very complex and high-cost fabrication and in some cases becomes impossible, mainly because of requiring depletion-type devices, multilevel ion implantation process technology, extra fabrication steps and multiple precise bias voltages to realize multiple-threshold voltages in MOS transistors. Besides, by the inescapable scaling down the feature size of the MOS transistor deeper in nanoranges, the CMOS technology meets many critical challenges and problems. These difficulties such as reduced gate control, large parametric variations, high power density and high lithography costs restricts the continuous dimension scaling of the MOSFET and decreases its suitability for the near future energy-efficient and robust applications. To overcome these problems, some beyond-CMOS nanodevices such as Quantum-dot Cellular Automata (QCA), Single Electron Transistor (SET) and Carbon Nanotube Field Effect Transistor (CNFET) have been introduced as the potential alternatives for the bulk MOSFET in the time to come [11, 19, 32]. Nevertheless, among these emerging nan-

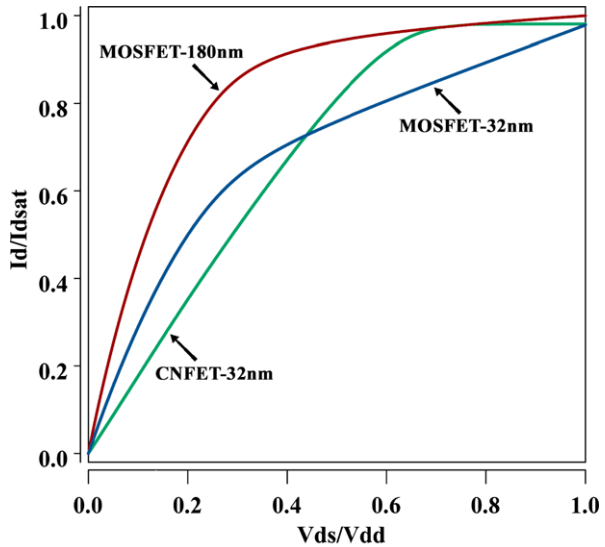
otechnologies, CNFET seems to be more appropriate on account of its likeness with MOSFET in terms of inherent electrical properties and consequently many of the previously designed CMOS structures are applicable in CNFET technology without any significant modifications. Moreover, the unique one-dimensional band structure of the CNFET represses backscattering and causes near-ballistic operation, which results in very high-speed operation [19]. CNFET has very high carrier velocity and higher transconductance and consequently has very higher speed and lower power consumption compared to MOSFET. Besides these benefits, CNFET seems to be very promising for overcoming the mentioned problems facing MOSFET in designing MVL circuits. This is due to the fact that the most prevalent and suitable method for designing voltage-mode MVL circuits is the multiple- V_{th} design technique and the desired threshold voltage can be obtained by adopting proper diameter for the nanotubes of the CNFET device [10, 17, 19, 27].

Several types of MVL circuit, specifically ternary, have already been presented in the literature since the emerging of MOSFET technology [2, 3, 8, 21, 22, 30, 31, 33, 34, 36]. Nevertheless, they suffer from many drawbacks which significantly degrade their suitability for the recent and the near future technologies. For instance designs of [21, 22] use large resistors, designs of [3, 8, 21, 22, 31, 33] require multiple supply voltages and designs of [2, 3, 8, 33, 34, 36] use depletion-mode MOSFETs which have become obsolete. Furthermore, in the recent years, some state-of-the-art CNFET-based ternary circuits have been proposed in the literature which benefit from the unique properties of carbon nanotube transistors [10, 15, 17, 19, 27]. However, limited efforts have been made so far for developing efficient MVL circuits for radices greater than three mostly due to technology concerns and hardware inefficiencies. Notwithstanding the mentioned advantages of MVL, from the hardware implementation point of view, MVL designs must be compatible with the existing inherently binary technologies. In this paper new CNFET-based robust and energy-efficient quaternary logic gates, decoder, multiplexer and arithmetic circuits are proposed. In the remainder of the paper, Sect. 2 briefly reviews the CNFET device. The new CNFET-based MVL circuits are presented in Sect. 3. The functionality, performance and immunity to process variation of the proposed circuits are evaluated in Sect. 4 and finally, Sect. 5 concludes the paper.

2 Review of Carbon Nanotube Field Effect Transistors (CNFETs)

Carbon Nanotube (CNT) is a carbon allotrope and can be considered as a graphene sheet, a two-dimensional honeycomb lattice of carbon atoms, rolled into a cylindrical nanostructure. CNTs can be classified into single-walled CNTs (SWCNTs), made up of a single cylinder, and multiwalled CNTs (MWCNTs), made up of more than one cylinder [18]. For each CNT a vector called chirality vector is defined, which is indeed the wrapping vector that the graphite sheet is considered to be rolled up along it and determines the formation angle of the carbon atoms along the nanotube. The chirality vector is specified by (n, m) pair called chiral number and specifies many physical and electrical characteristics of the CNT. A SWCNT is semiconductor if

Fig. 1 Normalized I_D – V_{DS} characteristic of MOSFET-like CNFET



CNFET: $L=32\text{nm}$, $W=61.487\text{nm}$ (Tubes=4), $D_{\text{CNT}}=1.487\text{nm}$, $V_{\text{DD}}=0.9\text{V}$

MOSFET-32nm: $L=32\text{nm}$, $W=64\text{nm}$, $V_{\text{DD}}=0.9\text{V}$

MOSFET-180nm: $L=180\text{nm}$, $W=360\text{nm}$, $V_{\text{DD}}=1.8\text{V}$

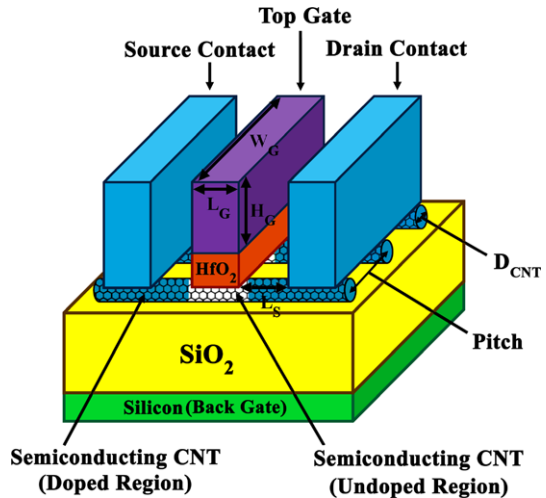
$n - m \neq 3k$ ($k \in \mathbb{Z}$) and otherwise it is conductor [15]. One or more semiconducting SWCNTs can be used as the channel of the CNFET device. In addition to the singular characteristics of the CNT material, removing the channel of the transistor from the silicon bulk decreases and eliminates many parasitic elements. Furthermore, a CNFET has similar I – V characteristics with a well-tempered MOSFET but with a considerably smaller channel-length modulation parameter (λ) [20]. Figure 1 shows the normalized I_D – V_{DS} characteristic of a typical 32 nm N-type CNFET, a 32 nm N-type MOSFET and an 0.18 μm N-type MOSFET, in which I_{Dsat} is the saturation ON current ($I_{\text{Dsat}} = I_D @ V_{\text{GS}} = V_{\text{DS}} = V_{\text{DD}}$).

The transistor sizing process of CNFET-based designs is less complex in comparison with the MOSFET-based designs, specifically for larger and more intricate circuits. This is due to the fact that contrary to MOSFET, electrons and holes have same mobilities in CNT ($\mu_n = \mu_p$) [1]. Ballistic conduction as well as the one-dimensional structure of CNT decrease the resistivity and significantly enhances the speed and minimize the energy dissipation of the device and reduce the power consumption density in the channel of CNFET.

Three distinct types of CNFET have been introduced so far in the literature, i.e. SB-CNFET, T-CNFET and MOSFET-like CNFET [28]. However, considering these kinds of CNFET, MOSFET-like CNFET is more appropriate for designing circuits based on the CMOS platform, on account of more resemblance with MOSFET in terms inherent electrical characteristics and transistor structure.

Moreover, the main preponderance of MOSFET-like CNFET is that its drain/source-channel connections have no Schottky barrier and accordingly it has significantly higher ON current and is very appropriate for ultra high-performance applications. The general structure of a MOSFET-like CNFET is demonstrated in Fig. 2. As

Fig. 2 Schematic diagram of a MOSFET-like CNFET



illustrated in Fig. 2, the distance between the centers of two adjacent CNTs below the same gate of a CNFET is called *Pitch*, which has a direct impact on the width of the contacts and the gate of the transistor.

The width of the gate of a CNFET can be calculated based on the following equation [12]:

$$W_{\text{gate}} = \text{Max}(W_{\text{min}}, (N - 1)\text{Pitch} + D_{\text{CNT}}) \tag{1}$$

where W_{min} is the minimum gate width and N is the number of nanotubes underneath the gate. Like a MOSFET, a CNFET has also threshold voltage (V_{th}), which is the necessary voltage for turning on the transistor electrostatically via the gate. A great attribute of CNFET is that the required threshold voltage can be determined for a CNFET by adopting a relevant diameter for its nanotubes. This is because of the straight dependence of the bandgap of the carbon nanotubes, which is a measure of the CNFET threshold voltage, to the diameter of the nanotubes. This practical characteristic makes CNFET very appropriate for designing voltage-mode MVL circuits. The threshold voltage of a CNFET is nearly considered to the first order as the half bandgap and is calculated according to the following equation [12]:

$$V_{\text{th}} \approx \frac{E_{\text{bg}}}{2e} = \frac{\sqrt{3}}{3} \frac{aV_{\pi}}{eD_{\text{CNT}}} \approx \frac{0.436}{D_{\text{CNT}} \text{ (nm)}} \tag{2}$$

where e is the unit electron charge, E_{bg} is the bandgap, a (≈ 0.249 nm) is the carbon to carbon atom distance, V_{π} (≈ 3.033 eV) is the carbon π - π bond energy in the tight bonding model and D_{CNT} is the diameter of the nanotubes. It can be concluded from Eq. (2) that the threshold voltage of a carbon nanotube transistor is inversely proportional to the diameter of its CNTs, which is calculated based on the following equation [12]:

$$D_{\text{CNT}} = \frac{a\sqrt{n^2 + nm + m^2}}{\pi} \approx 0.0783\sqrt{n^2 + nm + m^2} \tag{3}$$

For instance, D_{CNT} of a CNFET with the chiral number $(n, m) = (29, 0)$ is 2.27 nm and accordingly its threshold voltage is 0.192 V. Progress in fabrication processes of well-regulated CNTs has been reported in [13, 25]. A synthesis procedure for manufacturing SWCNTs with specific (n, m) chirality numbers has been presented in [35]. Postprocessing methods to set the desired threshold voltage of multitube CNFETs has been proposed in [14].

In addition, in [26, 37], fabrication of VLSI-compatible and imperfection-immune combinational and sequential CNFET logic circuits has been reported. These logic circuits, such as half-adder sum generators and D-latches, are the fundamental building blocks of VLSI digital systems. Chemical doping of CNTs to fabricate and integrate p-type and n-type CNFETs on the same substrate is also an important area of future research in order to reach complementary VLSI CNFET circuits [26].

In this work, we utilize multidiameter complimentary CNFET-based design method [17, 19] for designing the proposed quaternary logic circuits.

3 The Proposed Quaternary Circuits

3.1 Quaternary Logic Gates

A k -valued function $F(X)$ with t variables, where $X = \{x_1, x_2, x_3, \dots, x_t\}$ and each x_i can adopt values from $K = \{0, 1, 2, \dots, k-1\}$, is a mapping $f: K^t \rightarrow K$ and consequently there are k^{kt} different functions possible in the set f . Nevertheless, considering these possible functions, MIN, MAX and NOT operations are more consequential as they are the building blocks of many other complex logic and arithmetic circuits. These fundamental logical functions can be defined in a k -valued two-variable system as follows:

$$\text{Min}(a, b) = a \cdot b = \begin{cases} a & \text{if } a \leq b \\ b & \text{otherwise} \end{cases} \quad (4)$$

$$\text{Max}(a, b) = a + b = \begin{cases} a & \text{if } a \geq b \\ b & \text{otherwise} \end{cases} \quad (5)$$

$$\text{NOT}(a) = k - 1 - a \quad (6)$$

Quaternary logic includes four significant logic levels which can be demonstrated by “0”, “1”, “2” and “3” symbols. These logic levels are commonly equivalent to 0 V, $\frac{1}{3}V_{\text{DD}}$, $\frac{2}{3}V_{\text{DD}}$ and V_{DD} voltage levels, respectively. The basic platform of the proposed quaternary circuits is a quaternary buffer which is depicted together with its voltage transfer characteristic (VTC) in Fig. 3.

This quaternary buffer has a different design style with respect to the previously presented quaternary structures and is designed based on binary inverters. In addition, according to Fig. 3(b) the proposed QBuffer has a near-ideal VTC with high gain and very high-steep transition regions which leads to larger noise margins and lower power consumption. As a result, the proposed circuit is more robust and more suitable for low-voltage applications, compared to the previous structures. This high-precision quaternary buffer can be utilized as a driving booster or a voltage level restorer in larger quaternary circuits. In the proposed quaternary buffer, the transition

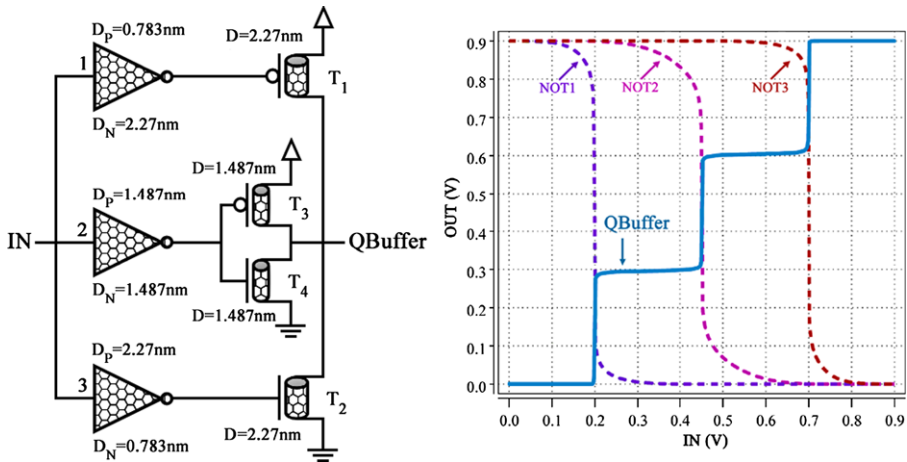


Fig. 3 The proposed quaternary buffer (QBuffer)

points of the binary inverters are specified by setting proper threshold voltages for their CNFETs, which are determined by the diameter of their CNTs [10, 17, 19, 27], according to Eq. (2). In this design, for CNFETs with diameters of 2.27 nm, 1.487 nm and 0.783 nm, the chirality numbers would be (29, 0), (19, 0) and (10, 0) and consequently, the threshold voltage values (V_{th}) would be 0.192 V, 0.293 V and 0.557 V, respectively. Furthermore, the transition regions can be tuned by adopting proper number of nanotubes for the CNFETs. According to Fig. 3, the operation of the proposed CNFET-based quaternary buffer can be briefly described as follows: when the input voltage is around 0 V or V_{DD} , T_2 and T_4 or T_1 and T_3 are ON and the output voltage would be 0 V or V_{DD} , respectively. Moreover, if the input voltage reaches around $\frac{1}{3}V_{DD}$ or $\frac{2}{3}V_{DD}$, T_1 , T_2 and T_4 or T_1 , T_2 and T_3 are ON and the output voltage would be $\frac{1}{3}V_{DD}$ or $\frac{2}{3}V_{DD}$, respectively, according to the voltage division between these CNFETs, which work in the linear region.

Based on Eqs. (4) and (5) as well as the proposed idea of Fig. 3, new two-input quaternary MIN and MAX circuits are proposed which are designed based on CNFET-based binary NAND and NOR gates with the conventional CMOS configuration. The proposed QMIN and QMAX circuits are shown in Figs. 4(a) and 4(b), respectively. The proposed two-input QMIN and QMAX designs can be also extended for determining the minimum and maximum values of three quaternary signals, just by utilizing three-input NAND and NOR gates, respectively.

To complete the set of the basic quaternary logic circuits a quaternary inverter is also proposed based on Eq. (6) and the proposed idea of Fig. 3 which is demonstrated together with its VTC in Fig. 5. According to Fig. 5(b) the proposed QNOT gate has an ideal VTC curve.

It is worth mentioning that for designing the proposed quaternary CNFET-based circuits only three different diameters are used for the nanotubes, while this number of diameters has been used in the previous works for designing ternary logic circuits [15, 17, 19].

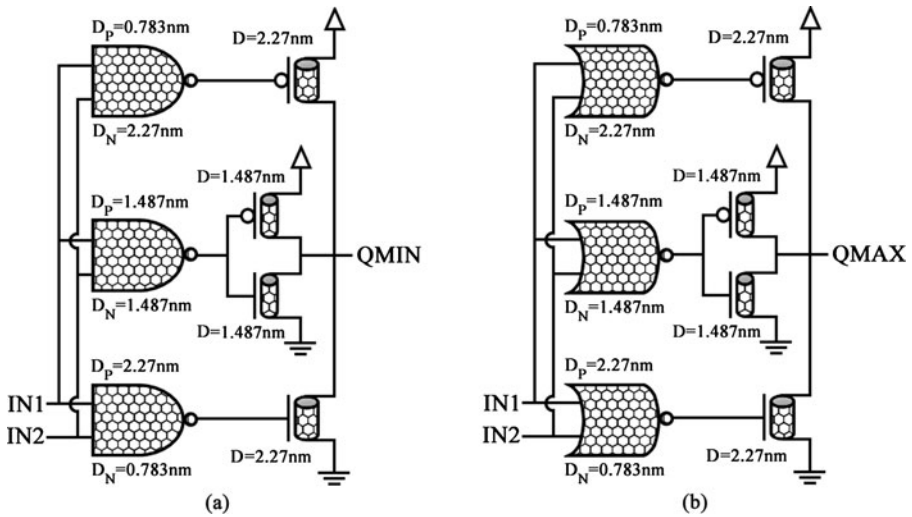


Fig. 4 The proposed quaternary two-input MIN and MAX circuits. (a) Quaternary MIN. (b) Quaternary MAX

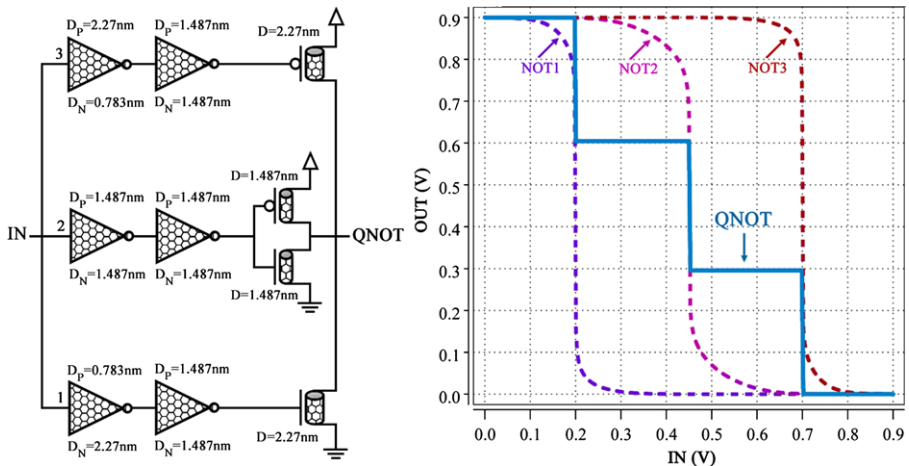


Fig. 5 The proposed quaternary inverter (QNOT)

It is worth mentioning that although the threshold voltage of the nano-MOSFET can also be varied, it cannot be used to design the proposed quaternary circuits with $L_g = 32\text{ nm}$ at 32 nm technology node, due to the very lower gain of the MOSFET-based binary inverters, in the transition region, compared to their CNFET-based counterparts [1], which is not adequate for this application. However, the gain of the input binary inverters is a very determining factor for correct operation, precision and robustness of the proposed quaternary designs, as shown in Figs. 4 and 5. To make the MOSFETs applicable for designing the proposed quaternary circuits, the gain of the binary inverters should become considerably higher, by increasing the channel

Table 1 Truth table of quaternary half adder and one-digit multiplier

Input		Output (quaternary HA)		Output (quaternary multiplier)	
A	B	QSUM	QCarry	QProduct	QCarry
0	0	0	0	0	0
0	1	1	0	0	0
0	2	2	0	0	0
0	3	3	0	0	0
1	0	1	0	0	0
1	1	2	0	1	0
1	2	3	0	2	0
1	3	0	1	3	0
2	0	2	0	0	0
2	1	3	0	2	0
2	2	0	1	0	1
2	3	1	1	2	1
3	0	3	0	0	0
3	1	0	1	3	0
3	2	1	1	2	1
3	3	2	1	1	2

length of the MOSFETs, which results in significant speed degradation and more area wastage, in comparison with the CNFET-based designs. Nevertheless, the gain of the binary inverters is still lower than their CNFET counterparts. In Sect. 4, the proposed CNFET-based quaternary circuits are compared with their MOSFET-based equivalents in terms of performance and energy efficiency.

3.2 Basic Quaternary Arithmetic Circuits

Arithmetic circuits are the essential parts in many VLSI applications [23]. Half adder (HA) and one-digit multiplier are the versatile and widely used building blocks that are used in larger adders, multipliers and many other types of arithmetic circuit. The truth table of the quaternary half adder and one-digit multiplier is given in Table 1.

A gate-level method, such as the one proposed in [17] for ternary logic, can be used for designing the quaternary basic arithmetic circuits based on the following equations, derived from Table 1.

For a quaternary half adder:

$$\begin{aligned} \text{QSUM} = & 1 \cdot (A_0B_1 + A_1B_0 + A_2B_3 + A_3B_2) \\ & + 2 \cdot (A_0B_2 + A_1B_1 + A_2B_0 + A_3B_3) \\ & + A_0B_3 + A_1B_2 + A_2B_1 + A_3B_0 \end{aligned} \quad (7)$$

$$\text{QCarry} = 1 \cdot (A_1B_3 + A_2B_2 + A_2B_3 + A_3B_1 + A_3B_2 + A_3B_3) \quad (8)$$

Also for a quaternary one-digit multiplier:

$$\begin{aligned} \text{QProduct} = & 1 \cdot (A_1 B_1 + A_3 B_3) + 2 \cdot (A_1 B_2 + A_2 B_1 + A_2 B_3 + A_3 B_2) \\ & + A_1 B_3 + A_3 B_1 \end{aligned} \quad (9)$$

$$\text{QCarry} = 1 \cdot (A_2 B_2 + A_2 B_3 + A_3 B_2) + 2 \cdot (A_3 B_3) \quad (10)$$

where \cdot and $+$ symbols denote the QMIN and QMAX operations, respectively and A_i and B_i can be produced according to the following equation:

$$S_i = \begin{cases} 3 & \text{if } S = i \\ 0 & \text{otherwise} \end{cases} \quad (11)$$

where i can adopt of 0, 1, 2 or 3 logic values.

However, this method is not efficient at all for designing quaternary arithmetic circuits and leads to a large number of logic gates and consequently a very large number of transistors. Another method is the multiplexer (MUX) logic design. Nevertheless, the efficiency of this method significantly depends on the hardware efficiency of the quaternary multiplexer. A quaternary four-to-one multiplexer has been proposed in [3], based on the quaternary logic gates. However, using this gate-level quaternary multiplexer for designing the quaternary arithmetic circuits is not efficient and leads to a very large number of transistors as well as a longer critical path.

An efficient design for quaternary four-to-one multiplexer is proposed in this paper, based on a new quaternary literal selector (quaternary decoder) and a CNFET-based transmission gate (TG) network, which is shown in Fig. 6. The proposed quaternary literal selector (Fig. 6(a)) works based on Eq. (11).

It should be noted that the inverters of the quaternary decoder operate based on the VTCs, shown in Fig. 3(b) (NOT1, NOT2 and NOT3), and the NOR circuits are conventional CMOS-style two-input NOR gates with symmetrical VTCs.

Moreover, the required complementary signals in the transmission gate network are generated by means of separate CNFET-based inverters, not included in Fig. 6(b). The transient response of the proposed quaternary MUX is shown in Fig. 7.

Based on the proposed quaternary multiplexer, a CNFET-based quaternary half adder is proposed which is shown in Fig. 8. In this design, besides the efficiency of the proposed quaternary multiplexers, some effective modifications are carried out which considerably reduce the complexity of the proposed design, compared to a pure MUX-based quaternary HA.

According to Table 1, it is obvious that in some cases the outputs are zero or similar to one of the inputs and therefore no multiplexing is required. For instance, when $A = 0$ the QSUM signal is similar to B and as a result B can be transmitted to the output without the first level multiplexing. Moreover, as there are only two different control signals for the TG networks, i.e. A and B , it is enough to decode them one time and then complement the decoded signals once and use them in the QTG modules. In addition, according to the formation of the QCarry output, shown in Table 1, a simpler module is used instead of a multiplexer for generating the QCarry signal in the proposed quaternary HA, which considerably reduces the complexity of the design. This simple module is designed based on the N-type CNFET switches which are controlled by the B input signal through the inverters, acting as threshold detectors. The VTCs of these inverters are shown in Fig. 3(b). According to the method of designing the proposed quaternary HA and contents of Table 1, a quaternary one-digit multiplier is also proposed, which is shown in Fig. 9.

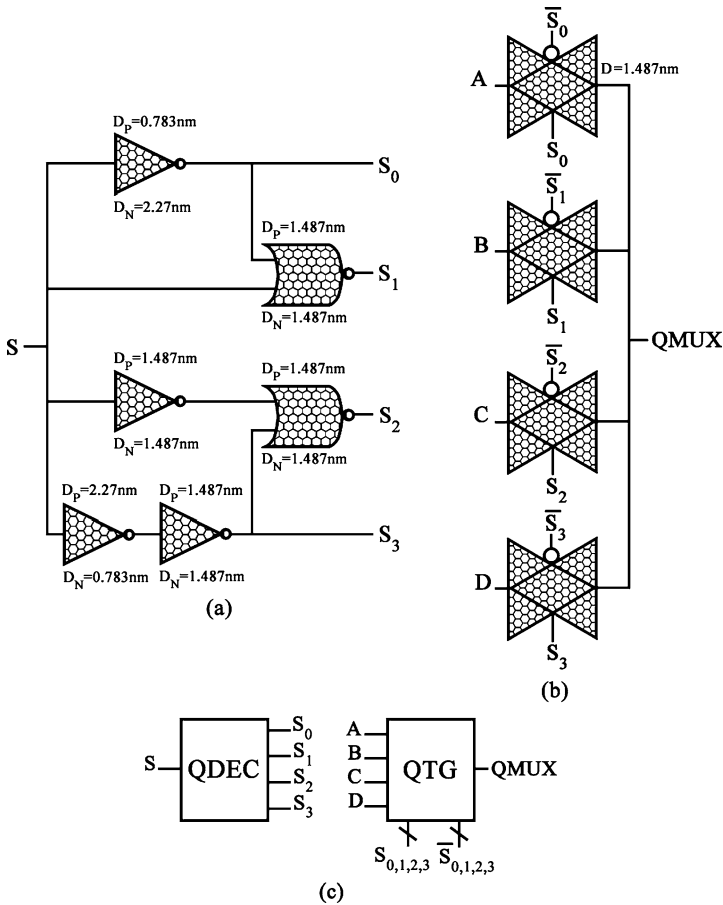


Fig. 6 The proposed quaternary MUX. (a) Quaternary decoder. (b) TG network. (c) Symbols of the quaternary decoder and TG network

It is worth noting that for designing the proposed quaternary CNFET-based arithmetic circuits only three different diameters are used for the nanotubes, whereas this number of diameters has been used in the previous works for designing the simple ternary logic gates [15, 17, 19].

4 Simulation Results

In this section, the performance of the proposed circuits, including tolerating the PVT variations, are evaluated in various conditions, using Synopsys HSPICE simulator with the Compact SPICE Model for CNFET ($L_g = 32\text{nm}$), including the non-idealities [4–6]. This standard model has been designed for unipolar enhancement-mode MOSFET-like CNFET which may contain one or more CNTs as its channel. This model considers a realistic and circuit-compatible CNFET structure and includes practical device nonidealities, parasitics, inter-CNT charge screening effects,

Fig. 7 Transient response of the proposed four-to-one quaternary MUX

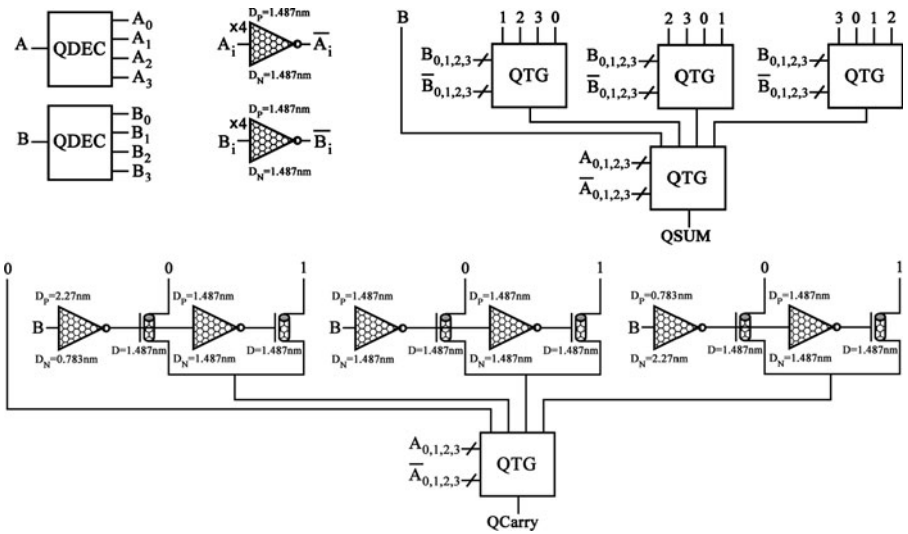
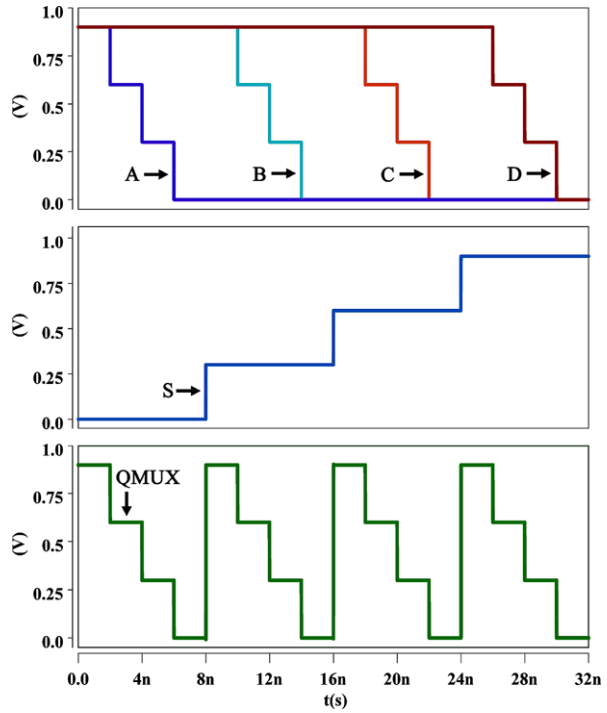


Fig. 8 The proposed quaternary half adder

Schottky-barrier effects at the contacts, scattering, back-gate effect, Source/Drain, Gate resistances and capacitances and doped source/drain expansion regions. Moreover, the model comprises a full transcapacitance network for more accurate tran-

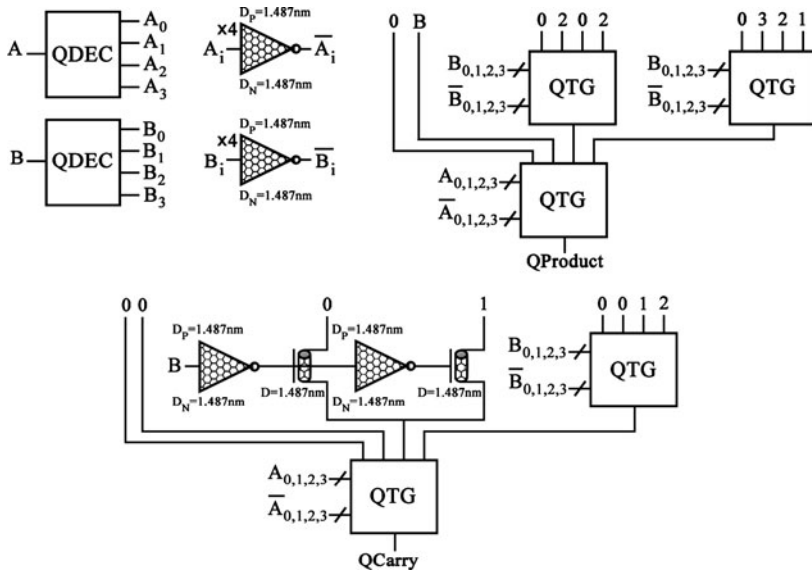


Fig. 9 The proposed quaternary one-digit multiplier

Table 2 Characteristics of the used MOSFET-like CNFET model

Parameter	Brief description	Value
L_{ch}	Physical channel length	32 nm
L_{ss}	The length of doped CNT source-side extension region	32 nm
L_{dd}	The length of doped CNT drain-side extension region	32 nm
L_{geff}	The Scattering mean free path in the intrinsic CNT channel and S/D regions	100 nm
Pitch	The distance between the centers of two neighboring CNTs within the same device	20 nm
L_{eff}	The mean free path in p+/n+ doped CNT.	15 nm
sub_pitch	Sub-lithographic (e.g. CNT gate width) pitch	4 nm
K_{ox}	The dielectric constant of high-k top gate dielectric material (HfO ₂)	16
T_{ox}	The thickness of high-k top gate dielectric material	4 nm
K_{sub}	The dielectric constant of substrate (SiO ₂)	4
C_{sub}	The coupling capacitance between the channel region and the substrate (SiO ₂)	40 aF/μm
E_{fi}	The Fermi level of the doped S/D tube	6 eV
ϕ_{iM}	The work function of Source/Drain metal contact	4.6 eV
ϕ_{iS}	CNT work function	4.5 eV

sient and dynamic performance simulations. The parameters of the CNFET model and their values, with brief descriptions, are listed in Table 2.

Figure 10 shows the input [33] and output signals of the proposed quaternary logic gates, respectively, which authenticate the correct operation of the designs. As

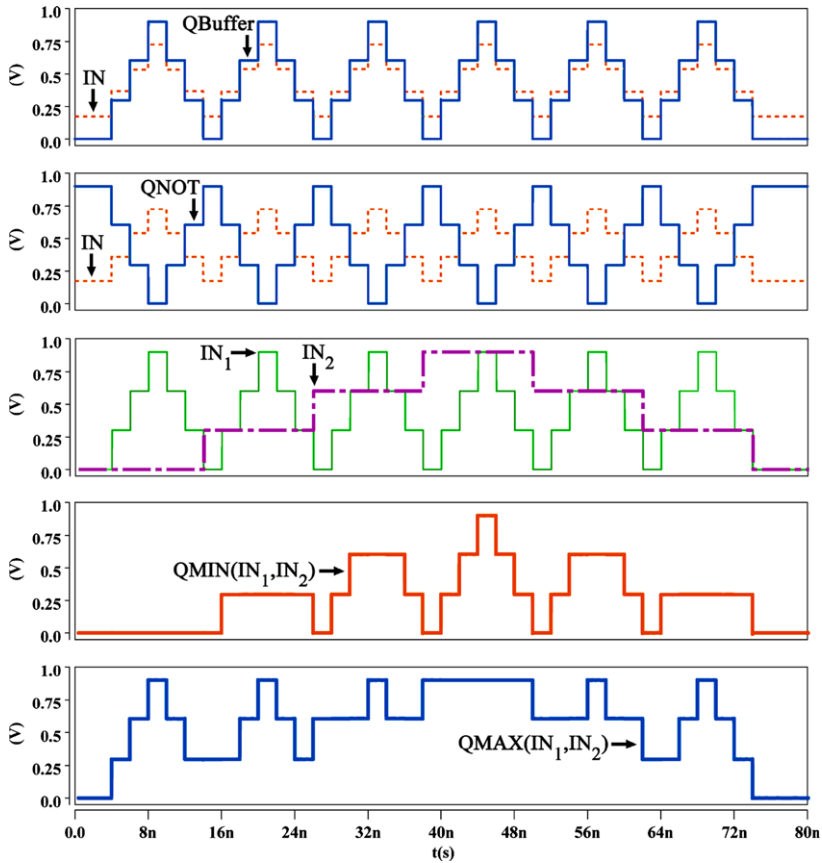


Fig. 10 Transient response of the proposed quaternary one-input and two-input logic gates

demonstrated in Fig. 10, the proposed quaternary buffer and inverter restore the non-full-swing quaternary input signals.

Furthermore, the transient response of the proposed three-input quaternary MIN and MAX circuits are shown in Fig. 11. The proposed CNFET-based quaternary logic circuits and their 32 nm MOSFET-based counterparts are simulated at 0.8 V, 0.9 V and 1 V voltages and 250 MHz frequency, and their propagation delay, average power consumption and average energy consumption are listed in Table 3. According to the results, the CNFET-based designs significantly outperform their MOSFET equivalents in terms of performance, power consumption and energy efficiency.

The delay and energy consumptions of the proposed quaternary logic circuits versus output load capacitor variation are plotted in Fig. 12(a), which demonstrate the correct operation and good driving capability of the designs when driving different load capacitances. To evaluate the performance of the circuits at different operational frequencies, they are tested at 100 MHz up to 2 GHz at 0.9 V supply voltage and the results are plotted in Fig. 12(c) and (d). The results demonstrate that the proposed designs work properly even at high frequencies and experience little performance

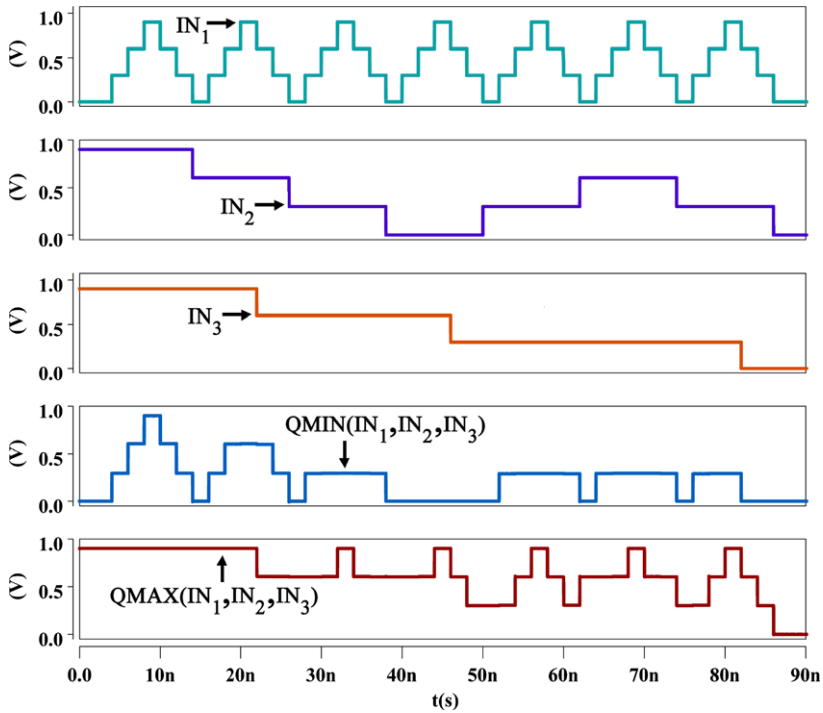


Fig. 11 Transient response of the proposed quaternary three-input logic gates

variation at different operational frequencies. Moreover, the proposed designs are simulated at various ambient temperatures, ranging from 0 °C up to 80 °C, to evaluate their sensitivity to the temperature variations. The experimental results, shown in Fig. 12(e) and (f), indicate little parametric variations of the proposed designs in the presence of temperature variations.

Systematic and random process variations are among the most significant challenges ahead of designing the nanoscale devices and circuits. As the presented CNFET-based quaternary logic circuits are designed based on multiple- V_{th} method, the impact of the process variations, which alternate the threshold voltages of the CNFETs, should be definitely studied. The most important parameters which determine the threshold voltage value of a CNFET are the diameter of its nanotubes and the thickness of its gate oxide layer (T_{ox}). Inasmuch as the timing variation is considered as a very important characteristic for a circuit, delay characteristics together with the energy consumption of the proposed circuits are investigated in the presence of process variation.

Hereupon, Monte Carlo transient analysis with a reasonable number of 30 iterations for each simulation is conducted. The statistical significance of 30 iterations is very high. If a circuit operates correctly for all the 30 iterations, there is a 99 % probability that over 80 % of all the possible component values operate properly [19]. Considering the inaccuracy of fabrication techniques, a standard deviation from the mean in the range of 0.04 nm to 0.2 nm is taken into account for each mean diameter

Table 3 Simulation results of the proposed quaternary logic gates

V_{DD} (V)	0.8 V	0.9 V	1 V
Delay ($\times 10^{-12}$ s)			
CNFET			
QBuffer	3.3999	2.9695	2.9134
QNOT	4.4315	3.0603	2.9412
Two-input QMIN	8.9671	7.0831	7.5787
Two-input QMAX	7.5766	7.0552	7.1490
Three-input QMIN	15.512	12.148	12.136
Three-input QMAX	12.145	11.995	11.037
MOSFET			
QBuffer	45.413	32.612	26.222
QNOT	50.298	38.787	33.071
Two-input QMIN	92.595	69.978	57.650
Two-input QMAX	132.31	98.649	81.909
Three-input QMIN	115.38	90.829	83.279
Three-input QMAX	151.09	120.97	120.12
Power ($\times 10^{-5}$ W)			
CNFET			
QBuffer	1.8306	2.4260	3.1291
QNOT	1.8339	2.4306	3.1588
Two-input QMIN	2.0668	2.7381	3.5507
Two-input QMAX	2.0677	2.7398	3.5550
Three-input QMIN	2.1559	2.8441	3.7408
Three-input QMAX	2.1735	2.8819	3.7233
MOSFET			
QBuffer	2.7027	3.6700	4.8407
QNOT	2.6739	3.6363	4.8099
Two-input QMIN	3.2328	4.3898	5.7571
Two-input QMAX	2.7875	3.7925	4.9911
Three-input QMIN	3.5845	4.866	6.3565
Three-input QMAX	2.8917	3.9631	5.3068
Energy Consumption ($\times 10^{-16}$ J)			
CNFET			
QBuffer	0.6224	0.7204	0.9116
QNOT	0.8127	0.7438	0.9291
Two-input QMIN	1.8533	1.9394	2.6909
Two-input QMAX	1.5665	1.9329	2.5414
Three-input QMIN	3.3442	3.4550	4.5398
Three-input QMAX	2.6397	3.4568	4.1094
MOSFET			
QBuffer	12.274	11.969	12.693
QNOT	13.449	14.104	15.907
Two-input QMIN	29.934	30.719	33.189
Two-input QMAX	36.881	37.413	40.882
Three-input QMIN	41.358	44.197	52.936
Three-input QMAX	43.691	47.942	63.745

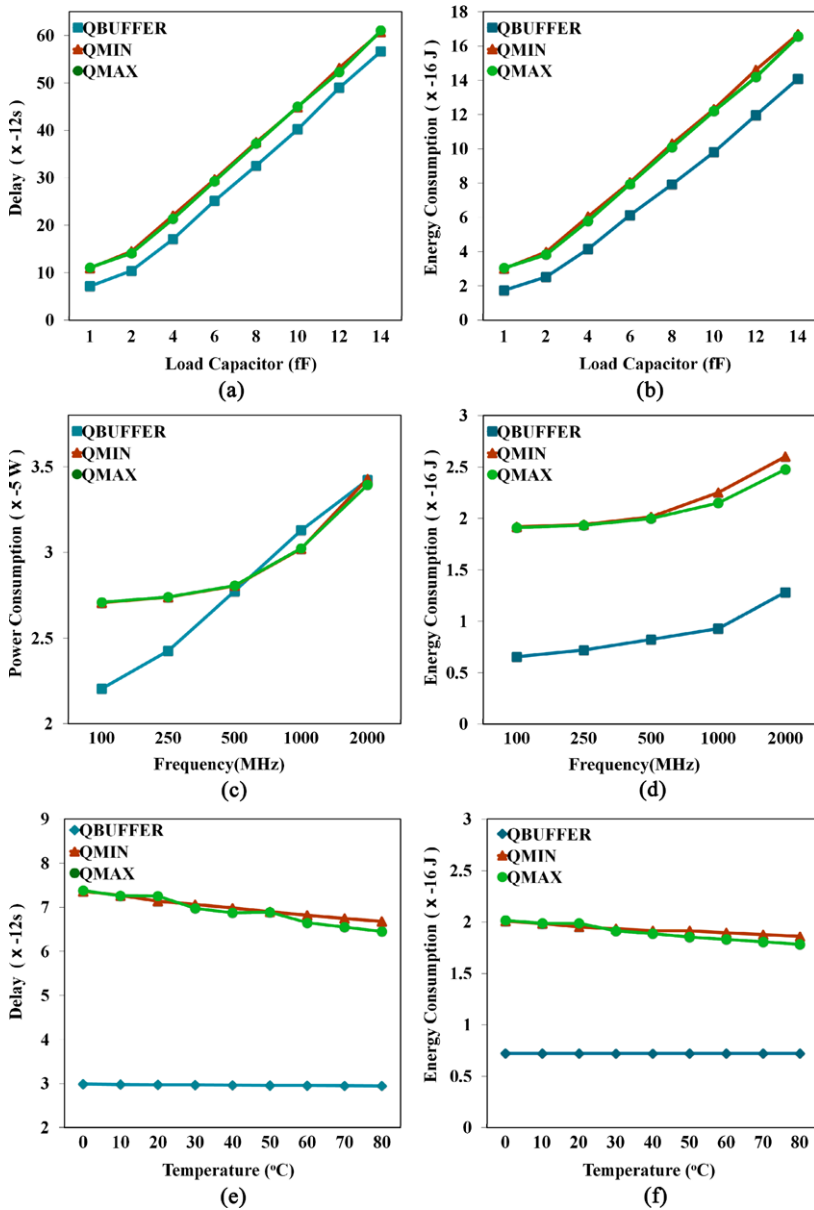


Fig. 12 Performance of the designs versus load capacitor, frequency and temperature variations

value [29]. Moreover, the distribution of the diameter and T_{ox} is assumed as Gaussian with 6-sigma distribution [16, 19]. The results of this experiment are shown in Fig. 13. According to the results, the proposed MVL circuits operate correctly with little parametric variations in the presence of process variations.

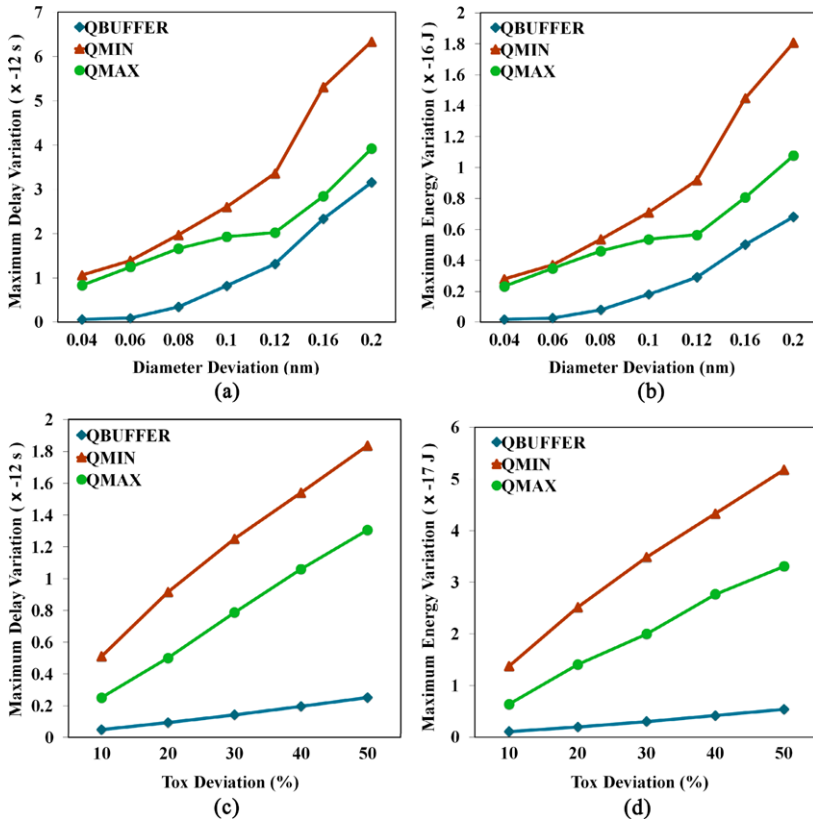


Fig. 13 Parameter variations of the designs in the presence of process variation

It is worth noting that the delay of the proposed quaternary logic circuits experience considerably less variation in the presence of process variation even compared with the state-of-the-art CNFET-based ternary logic circuits presented in the literature [15, 17].

Figure 14 shows the transient responses of the proposed quaternary half adder and one-digit multiplier, which are consistent with the truth table given in Table 1.

Moreover, the simulation results of the quaternary arithmetic circuits at 0.8 V, 0.9 V and 1 V supply voltages are given in Table 4. It is worth noting that in this table the designs based on [17] are gate-level quaternary arithmetic circuits, designed based on the proposed quaternary logic gates according to Eqs. (7), (8), (9) and (10) as well as the method of design proposed in [17]. Moreover, the designs based on [3] are gate-level quaternary arithmetic circuits, designed based on the quaternary multiplexer of [3] and the proposed quaternary logic gates. As predicted before, it can be inferred from the result that the gate-level design is not suitable for designing the quaternary arithmetic circuits and the proposed method leads to quite more efficiency in terms of the number of transistors, delay, power and energy consumption. In addition, the higher performance and more energy efficiency of the proposed quaternary arithmetic circuits compared to the design based on [3] demonstrate the superiority of the

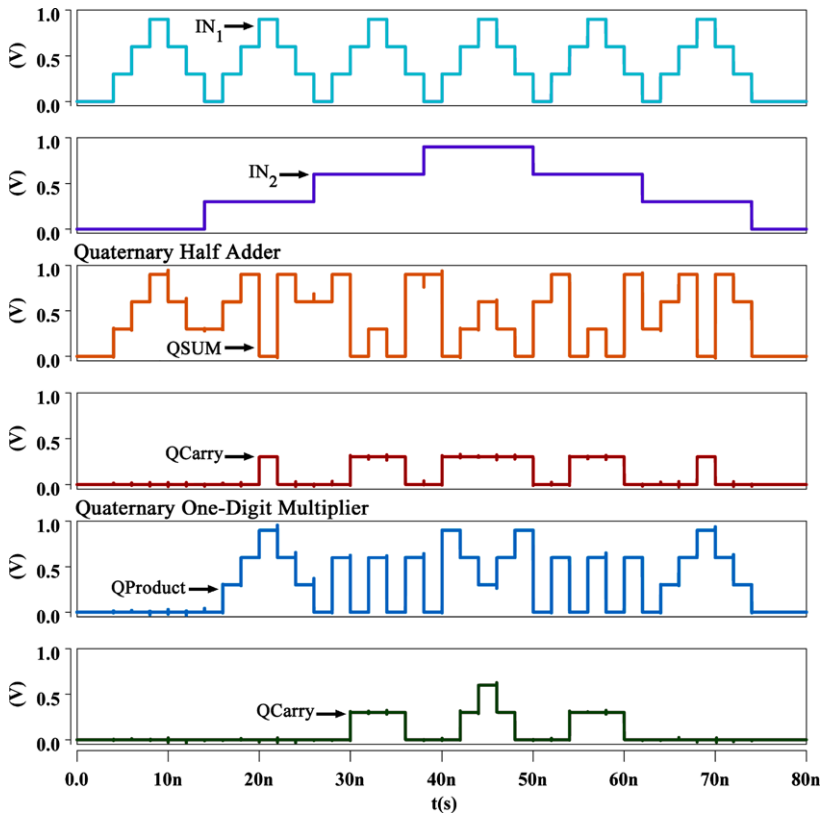


Fig. 14 The transient response of the proposed CNFET-based quaternary half adder and multiplier

proposed quaternary multiplexer in comparison with the gate-level design proposed in [3] for quaternary multiplexer.

5 Conclusion

New high-speed, high-precision and PVT tolerant quaternary logic gates, decoder, multiplexer and arithmetic circuits have been proposed for nanotechnology, based on CNFETs. The proposed CNFET-based circuits have been designed based on the CMOS-style binary gates, composed of multiple- V_{th} nanodevices, and have benefited from the unique properties of CNFET. Moreover, the proposed MVL designs are compatible with the recent technologies. For designing the proposed quaternary circuits only three different CNT diameters, all less than 2.3 nm, have been used which enhance the feasibility and manufacturability of the designs. The simulation results confirm the authenticity of the proposed method in various simulation conditions as well as in the presence of process, voltage and temperature variations.

Table 4 Simulation results of CNFET-based quaternary arithmetic circuits

V_{DD} (V)	0.8 V	0.9 V	1 V
Quaternary half adder			
Delay ($\times 10^{-12}$ s)			
Proposed design	24.219	20.573	18.916
Design based on [17]	45.408	38.336	34.486
Design based on [3]	54.914	46.142	34.486
Power ($\times 10^{-5}$ W)			
Proposed design	0.2294	0.5882	1.2714
Design based on [17]	4.6469	6.3687	8.6289
Design based on [3]	39.195	52.067	86.289
Energy Consumption ($\times 10^{-16}$ J)			
Proposed design	0.5555	1.2101	2.4049
Design based on [17]	21.101	24.415	29.758
Design based on [3]	215.23	240.24	297.58
Quaternary one-digit multiplier			
Delay ($\times 10^{-12}$ s)			
Proposed design	25.745	21.928	20.059
Design based on [17]	33.738	27.580	25.719
Design based on [3]	44.055	33.005	28.865
Power ($\times 10^{-5}$ W)			
Proposed design	0.2164	0.5379	1.1292
Design based on [17]	5.1108	6.9856	9.4342
Design based on [3]	27.845	37.056	48.366
Energy Consumption ($\times 10^{-16}$ J)			
Proposed design	0.5573	1.1795	2.2651
Design based on [17]	17.243	19.267	24.263
Design based on [3]	122.67	122.3	139.61

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