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High Input Impedance NMOS-based Phase Shifter with Minimum Number of Passive Elements

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Abstract In this paper, a new voltage-mode (VM) first-order phase shifter (all-pass filter) employing only four NMOS transistors and minimum number of passive elements (i.e. one resistor and one capacitor) is proposed. The proposed VM phase shifter has high input impedance and does not require passive element matching constraints. Moreover, since only two NMOS transistors are stacked between positive and negative supply voltages, the proposed circuit is suitable for low-voltage operation. Electronic tunability can be provided easily by replacing the employed resistor with an NMOS transistor operating in triode region. Simulation results based on 0.18 μm TSMC CMOS parameters with ±0.9 V supply voltages are given to demonstrate the performance of the proposed phase shifter.

Keywords Phase shifter · All-pass filter · NMOS transistor · Tunability

1 Introduction

Phase shifters (all-pass filters) are generally used to adjust the phase difference between two signals to a particular value. First-order all-pass filters are commonly used as phase shifters since they have ideally constant magnitude against the change in frequency. In a first-order all-pass filter, the amount of phase shifting varies with frequency from 0° to −180° in non-inverting type (or 180° to 0° in inverting type).

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A literature survey shows that several first-order voltage-mode (VM) phase shifters have been reported [1, 2, 4–10, 12–14].

Maundy and Aronhime proposed an all-pass filter consisting of six NMOS transistors, a floating resistor and a grounded capacitor [6]. However, the input signal requires a common-mode input level greater than $2V_{Tn}$ (threshold voltage of the NMOS transistor) to ensure that all of the transistors are in saturation. Moreover, a mandatory DC voltage is appeared in the transfer function (TF) of the circuit which shifts the level of the output signal. Also, it does not provide high input impedance.

The phase shifter reported in [12] is composed of two NMOS and three PMOS transistors, a DC current source for biasing purpose and one floating capacitor. The circuit enjoys the feature of electronic tunability via changing the biasing current. However, considering extra circuitry for realizing the biasing current in the circuit of [12], additional transistors will be required. Moreover, the circuit suffers from frequency-dependent input impedance.

There are also two recently published phase shifters in [13, 14]. The circuit in [13] employs two NMOS and one PMOS transistors together with two floating resistors and one grounded capacitor. However, a matching constraint should be met to provide an all-pass response. Moreover, the circuit requires two external biasing voltages. Although the circuit in [14] employs only two NMOS transistors and one grounded capacitor, it requires three resistors with a matching constraint between two of them. Moreover, the circuit suffers from the attenuation of $1/3$ in its TF. Similarly, the configuration of [7] can provide a gain of only $1/3$, and requires a passive component matching condition.

The circuit of [10] is based on root-domain operation and provides high input impedance. It employs only one grounded capacitor as passive element but requires tens of transistors. Apart from these, an all-pass network employing two BJT transistors, four resistors and one capacitor is reported in [2].

In this paper, a novel VM first-order phase shifter employing four NMOS transistors, one capacitor and one resistor, is introduced. The circuit does not require matching of passive elements and additional biasing voltage or current sources. Removing the employed resistor in the circuit and replacing it with an NMOS transistor, an electronically tunable phase shifter is obtained. Table 1 summarizes the advantages and disadvantages of the previously reported phase shifters as well as the proposed one.

Note that none of the above discussed circuits provide low output impedance, thus a buffer will be required to drive resistive loads.

Finally, it should be mentioned that many VM phase shifters like circuits in [1, 4, 5, 8, 9] using active building blocks (different types of current conveyors) have been reported. However, these active building blocks typically involve more than ten transistors.

2 Proposed Phase Shifter

A common-source (CS) stage with diode-connected load is depicted in Fig. 1 [11]. Neglecting channel-length modulation of the transistors, the voltage characteristic of

Table 1 Comparison of the previously published MOS transistor-based phase shifters and the proposed one

Criteria \ Reference	[6]	[12]	[13]	[14]	[10]	[7]	This work (tunable one)
# of MOS transistors	6	5	3	2	tens	9	5
# of resistors	1	0	2	3	0	2	0
Free of passive element matching constraint	Yes	Yes	No	No	Yes	No	Yes
High input impedance	No	No	No	No	Yes	No	Yes
Gain (magnitude)	1	1	1	1/3	1	1/3	1
Tunability	No	Yes	No	With extra circuitry	Yes	Yes	Yes
Technology	0.35 μm	0.35 μm	0.35 μm	0.18 μm	0.25 μm	0.35 μm	0.18 μm
Power supplies	3.3 V	±1.5 V	±1.5 V	±0.9 V	2.5 V	±1.5 V	±0.9 V

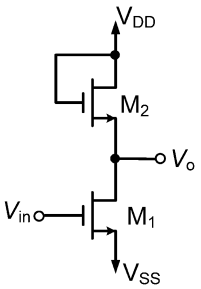


Fig. 1 Simple CS stage with diode-connected load

the amplifier can be described by

$$\begin{aligned} V_{\mathrm{o}} &= g(V_{\mathrm{in}}) \\ &= b_0 + b_1 V_{\mathrm{in}} \end{aligned} \tag{1}$$

where the coefficients in (1) are computed by

$$b_0 = V_{\mathrm{DD}} - V_{\mathrm{Tn2}} + \sqrt{\frac{k_{\mathrm{n1}}}{k_{\mathrm{n2}}}}(V_{\mathrm{SS}} + V_{\mathrm{Tn1}}) \tag{2a}$$

$$b_1 = -\sqrt{\frac{k_{\mathrm{n1}}}{k_{\mathrm{n2}}}} \tag{2b}$$

Here, $k_{\mathrm{n}i}$, and $V_{\mathrm{Tn}i}$ $(i = 1, 2)$ are device transconductance parameter and threshold voltage of the ith transistor, respectively. The parameter $k_{\mathrm{n}i}$ is found as

$$k_{\mathrm{n}i} = \left(\frac{W}{L}\right)_i \mu_{\mathrm{n}} C_{\mathrm{ox}} \tag{3}$$

where W/L is the channel width/channel length ratio, μ_{n} is electron mobility and C_{ox} is the gate capacitance per unit area of the NMOS transistor [11]. If $V_{\mathrm{Tn1}} = V_{\mathrm{Tn2}}$,

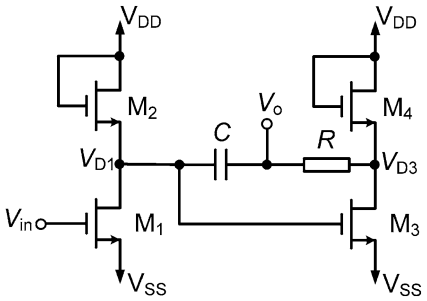


Fig. 2 Proposed voltage-mode phase shifter

$V_{SS} = -V_{DD}$, and $k_{n1} = k_{n2}$, the output voltage in (1) turns to

$$V_o = -V_{in} \tag{4}$$

The proposed phase shifter circuit is shown in Fig. 2. Each of matched transistors M_1–M_2 and M_3–M_4 constitutes a unity-gain inverting amplifier. It is assumed that the effects of the loads connected to the inverting amplifiers are negligible, which can be achieved by selecting the dimensions of M_1–M_4 sufficiently large. The operation of the proposed phase shifter shown in Fig. 2 can be ideally expressed by the following equations:

$$V_{D1} = -V_{in} \tag{5a}$$

$$V_{D3} = V_{in} \tag{5b}$$

$$(V_{D1} - V_o)sC = \frac{V_o - V_{D3}}{R} \tag{5c}$$

From (5a), (5b) and (5c), the phase shifter TF can be derived as follows:

$$\frac{V_o}{V_{in}} = \frac{1 - sCR}{1 + sCR} \tag{6}$$

From (6), the following phase response is obtained:

$$\varphi(\omega) = -2\tan^{-1}(\omega CR) \tag{7}$$

If R and C of the proposed circuit are interchanged, an inverting all-pass response with following TF is obtained:

$$\frac{V_o}{V_{in}} = -\frac{1 - sCR}{1 + sCR} \tag{8}$$

From (8), the following phase response is obtained:

$$\varphi(\omega) = \pi - 2\tan^{-1}(\omega CR) \tag{9}$$

It is important to note that for proper operation of the circuit, transistors M_1 and

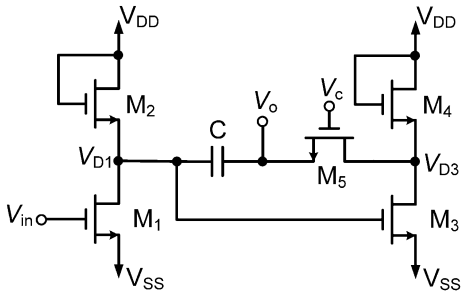


Fig. 3 The proposed tunable phase shifter

M_3 should be kept in saturation region. Considering equal threshold voltages for M_1 and M_3 ($V_{Tn1} = V_{Tn3} = V_{Tn}$) the following conditions should be satisfied:

$$V_{D1} \geq V_{in} - V_{Tn} \tag{10a}$$

$$V_{D3} \geq V_{D1} - V_{Tn} \tag{10b}$$

Combining (5a) and (5b) with the conditions in (10a) and (10b) results in the following restriction for the input voltage:

$$-\frac{V_{Tn}}{2} \leq V_{in} \leq \frac{V_{Tn}}{2} \tag{11}$$

Tunability is an important issue [3] which should be considered in the design of phase shifters. In the circuit of Fig. 2, one can replace the resistor R with a NMOS transistor operated in linear region to obtain an electronically tunable phase shifter as shown in Fig. 3. Here by adjusting the gate voltage of transistor M_5 one can control the phase shift between input and output signals. Assuming triode region operation and small drain–source voltage (V_{DS}) for transistor M_5, the resistive component obtained from M_5 can be approximately evaluated as

$$R_{eq} \cong \frac{1}{k_{n5}(V_{GS5} - V_{Tn5})} \tag{12}$$

The small drain–source voltage condition for transistor M_5 can be expressed as $V_{DS5} \ll V_{GS5} - V_{Tn5}$. Considering that $V_{DS5} = V_{D3} - V_o = V_{in} - V_o$, $V_{GS5} = V_C - V_o$ and using a factor of 10 to satisfy the inequality, the maximum allowable amplitude for the input signal of the tunable phase shifter can be given as

$$|V_{in}|_{max} = 0.1(V_C - V_{Tn5}) \tag{13}$$

From (13) it is observed that the dynamic range of the input signal can be increased selecting higher control voltages (V_C) for the transistor M_5. Note that since the input and output signals in the phase shifter have ideally equal magnitudes; the condition in (13) is valid also for maximum output voltage, $|V_o|_{max}$.

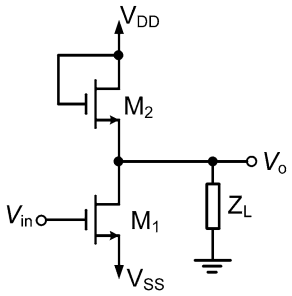


Fig. 4 Inverting amplifier with a load

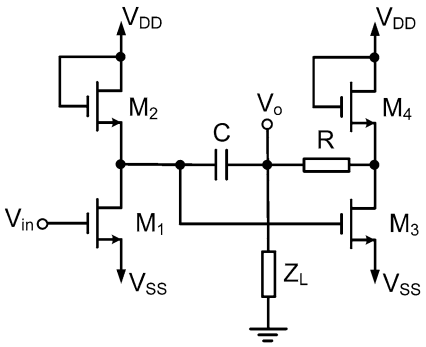


Fig. 5 The proposed phase shifter with a load

3 Loading Effects

In this section loading effects on the inverting amplifier of Fig. 1 and proposed circuit in Fig. 2 are investigated. The inverting amplifier and proposed phase shifter with a load Z_L are depicted in Figs. 4 and 5, respectively. If $V_{Tn1} = V_{Tn2} = V_T$, $V_{SS} = -V_{DD}$ and $k_{n1} = k_{n2} = k_n$, the output voltage of Fig. 4 is evaluated as

$$V_o = \frac{1 + k_n Z_L (V_{DD} - V_T) - \sqrt{1 + k_n Z_L (2V_{DD} - 2V_T + k_n Z_L (V_{DD} + V_{in} - V_T)^2)}}{k_n Z_L} \tag{14}$$

It is observed from (14) that if k_n is sufficiently large, $V_o \approx -V_{in}$. Thus transistors with high W/L ratios should be selected to decrease the loading effect. If ideal inverting amplifiers ($k_n = \infty$ or practically very large) are used in the phase shifter of Fig. 5, the following TF is obtained.

$$\frac{V_o}{V_{in}} = \frac{1 - sCR}{1 + \frac{R}{Z_L} + sCR} \tag{15}$$

Assuming $Z_L = R_L \parallel (1/sC_L)$, the TF in (15) turns to

$$\frac{V_o}{V_{in}} = \frac{1 - sCR}{1 + \frac{R}{R_L} + s(C + C_L)R} \tag{16}$$

Thus one should select $R \ll R_L$ and $C \gg C_L$ to obtain an ideal all-pass response.

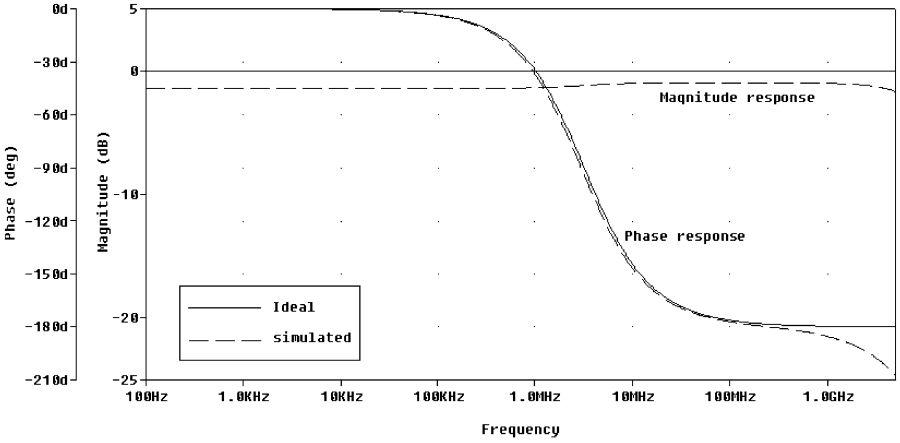


Fig. 6 Ideal and simulation responses of the proposed phase shifter of Fig. 2

4 Simulation and Experimental Results

The proposed circuits of Figs. 2 and 3 are simulated using 0.18 μm TSMC CMOS technology parameters ($V_{TH0} = 0.37$ V, $U_0 = 259.5$ cm^2/(V s) and $T_{OX} = 4.1$ nm) with power supply voltages $V_{DD} = 0.9$ V and $V_{SS} = -0.9$ V. The bulks of all NMOS transistors (except for M_5 which is connected to V_{SS}) are connected to the relevant sources to prevent body effect.

The aspect ratios of all NMOS transistors in Fig. 2 are chosen as $W/L = 27\ \mu m/0.18\ \mu m$. Note that the W/L ratio of the transistors should be selected sufficiently high to decrease the loading effect. The passive components for the circuit of Fig. 2 are selected as $R = 5$ kΩ, and $C = 10$ pF which results in a pole frequency of $f_o \cong 3.18$ MHz. Phase and magnitude responses of the proposed phase shifter of Fig. 2 are shown in Fig. 6. Applying a sinusoidal input signal with 20 mV peak value and frequency of 3.18 MHz to the circuit, the output of the circuit is shown in Fig. 7. From Fig. 7, a phase shifting of 90° between input and output signals can be observed. From Figs. 6 and 7 it can be seen that the gain of the phase shifter is smaller than unity which is due to the loading effects of the C and R elements on the inverting amplifiers of M_1–M_2 and M_3–M_4, respectively. The total harmonic distortion of the output signal is found to be 0.082%. The noise performance of the proposed circuit is shown in Fig. 8. The output and input referred voltage noises of the circuit at pole frequency (3.18 MHz) are found as 6.4 nV/$\sqrt{\text{Hz}}$ and 7.4 nV/$\sqrt{\text{Hz}}$, respectively.

For the tunable phase shifter of Fig. 3, transistor M_5 with $W/L = 27\ \mu m/0.18\ \mu m$ and different control voltages (V_c) are used to exhibit the tunability of the circuit. Applying $V_c = 0.65$ V, 0.69 V, 0.73 V and 0.77 V results in phase shift of 90° at 3.48 MHz, 8 MHz, 15.7 MHz, and 26.1 MHz, respectively. The results are shown in Fig. 9. It can be seen that the phase response of the circuit can be tuned over a wide range of frequency by changing V_c.

Experimental test has been performed for the developed all-pass filter in Fig. 2 with $R = 1$ kΩ, $C = 1$ nF, ±15 V dc supply voltages and CD4007 array transistors. The resultant waveforms with 90° phase shift at 159 kHz are demonstrated in Fig. 10.

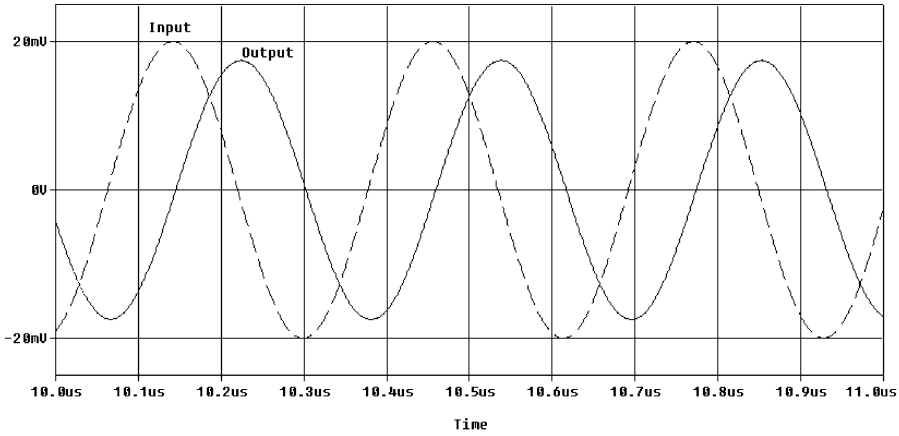


Fig. 7 Sinusoidal input and output responses of the proposed phase shifter at $f = 3.18$ MHz

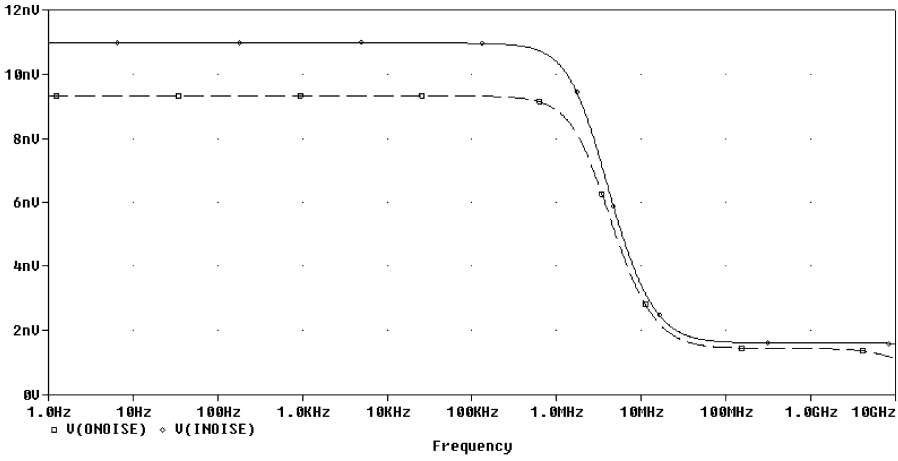


Fig. 8 Output and input referred noise responses of the phase shifter in Fig. 2

5 Conclusion

In this paper, a novel VM first-order phase shifter employing only four NMOS transistors and canonical number of passive elements is developed. The proposed VM phase shifter has high input impedance and does not require passive element matching conditions. In addition, since only two NMOS transistors are stacked between positive and negative supply voltages, the proposed circuit is suitable for low-voltage operation. Electronic tunability can be realized easily by replacing the employed resistor with an NMOS transistor operating in triode region. Simulation based on 0.18 μm TSMC CMOS parameters and experimental test with CD4007 CMOS array transistors are performed, which verify well the theoretical analysis.

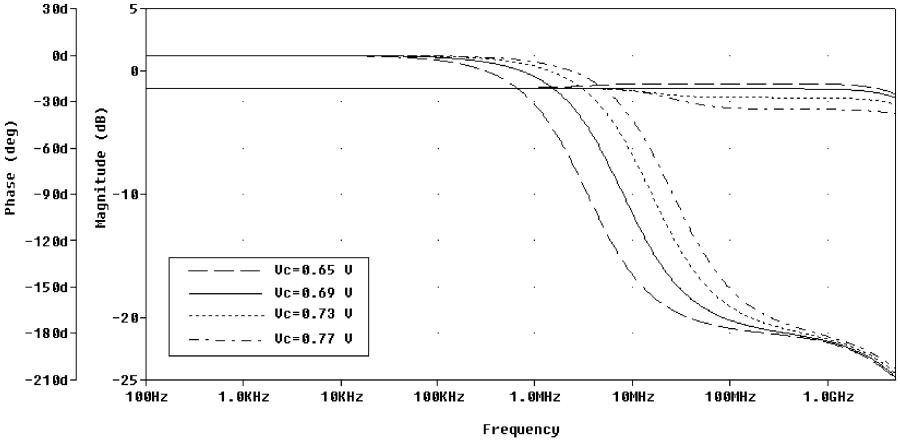
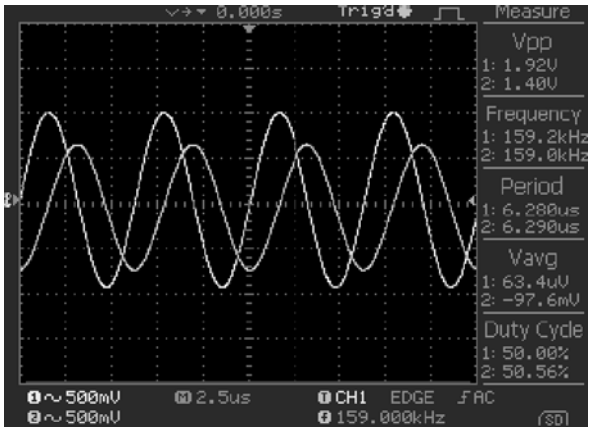


Fig. 9 The tunability performance of the phase shifter in Fig. 3

Fig. 10 Experimental test result for the circuit of Fig. 2



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