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DVCC-Based Non-linear Feedback Neural Circuit for Solving System of Linear Equations

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Abstract A neural circuit to solve a system of simultaneous linear equations is presented. The circuit employs non-linear feedback to achieve a transcendental energy function that ensures fast convergence to the exact solution while enjoying reduction in hardware complexity over existing schemes. A new building block for analog signal processing, the digitally controlled differential voltage current conveyor (DC-DVCC) is introduced and is utilized for the non-linear synaptic interconnections between neurons. The proof of the energy function has been given and it is shown that the gradient network converges exactly to the solution of the system of equations. PSPICE simulation results are presented for linear systems of equations of various sizes and are found to be in close agreement with the algebraic solution. The use of CMOS DC-DVCCs and operational amplifiers facilitates monolithic integration.

Keywords Neural network applications · Neural network hardware · Non-linear circuits · Linear algebra · Linear equations · Digitally Controlled DVCC

1 Introduction

Solution of a system of simultaneous linear equations has been a primary goal for computation since the time of the abacus. References to word problems requiring the solution of a system of linear equations appear in ancient Babylonian texts dating back to *circa* 300 BC [3]. Some examples of applications requiring the solution of systems of linear equations are curve fitting, electrical circuit analysis, multiple cor-

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relation as well as real-time applications like real-time speech coding, image processing, stochastic modelling, and computer-aided realistic three-dimensional image synthesis [1, 3, 5, 10, 11]. Traditional methods for solving systems of linear equations typically involve an iterative process [3], but long computational time limits their usage. There is an alternative approach to the solution of this problem. It is to exploit the artificial neural networks (ANN's), which can be considered as an analog computer relying on a highly simplified model of neurons [1, 5, 10, 11]. Massively parallel processing and fast convergence, which are inherent to neural networks, are utilized to reduce the time taken to arrive at the solution [1, 10, 11]. However, existing neural networks have variable penalty parameters which decrease to zero as time increases to infinity in order to get better accuracy of solution. Therefore, the time taken to arrive at the solution in such cases is not always short [1, 10].

Hardware solutions for solving a system of linear equations based on neural networks have been put forward by Xia, Wang and Hung [11], Cichocki and Unbehauen [1] and Wang [10]. To solve an n-variable system of equations, the network of [10] uses three operational amplifiers, one capacitor and $(n + 5)$ resistances to emulate a single neuron and the time to arrive at the solution is of the order of hundreds of milliseconds. The network of [1] provides a significantly improved solution time of around a microsecond but at the cost of increased hardware complexity. Each neuron in [1] comprises three weighted summers and an inverting integrator. The architecture of [11], which is a generalized neural network based implementation of Censor and Elfving's method for linear inequalities, also uses an approach similar to [10], utilizing weighted adders and integrators to realize the neurons.

A new digital programmable architecture with fast convergence and reduced circuit complexity is presented. The proposed architecture uses non-linear feedback which leads to a new energy function that involves transcendental terms. This transcendental energy function is fundamentally different from the standard quadratic form associated with Hopfield network and its variations. The non-linear feedback is realized by utilizing a new building block viz. the digitally controlled differential voltage current conveyor (DC-DVCC). Along with presenting the analysis of the proposed circuit and the proof of the energy function, it is also shown that the stable state of the network corresponds exactly with the solution of the given system of linear equations. Further, the use of CMOS DC-DVCCs and opamps makes monolithic integration viable.

This paper is organized as follows. A new digitally programmable analog building block (DC-DVCC) is presented in Sect. 2. Section 3 contains the details of the proposed network along with the design equations. Proofs of the energy function and validity of the solution are given in Sect. 4. Section 5 presents the results of SPICE simulation of the circuit applied to solve various sample equation sets. A discussion on VLSI implementability of the proposed circuit appears in Sect. 5. Some conclusive remarks appear in Sect. 6.

2 Digitally Controlled DVCC

The differential voltage current conveyor (DVCC) was proposed in 1997 [2] as a five terminal device characterized by the following port relations (Fig. 1):

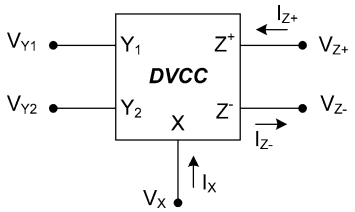

Fig. 1 Block representation of the DVCC

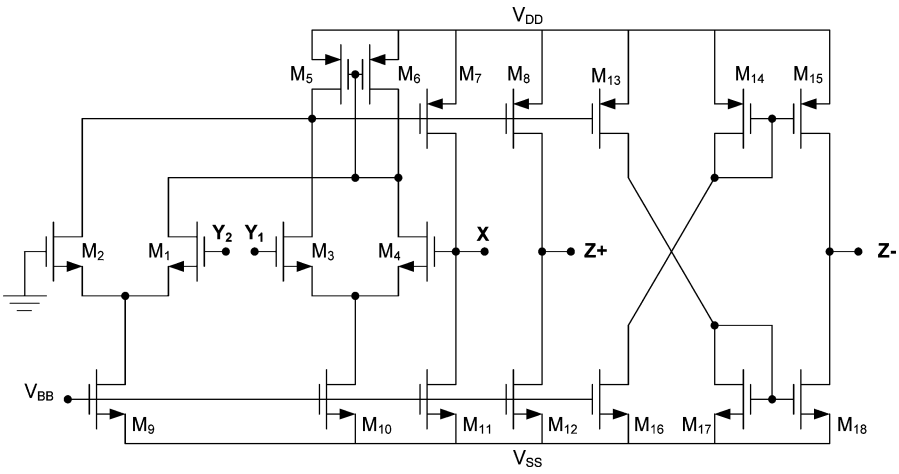

Fig. 2 CMOS implementation of DVCC

$$\begin{bmatrix} V_X \\ I_{Y_1} \\ I_{Y_2} \\ I_Z^+ \\ I_Z^- \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ k & 0 & 0 & 0 & 0 \\ k & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y_1} \\ V_{Y_2} \\ V_Z^+ \\ V_Z^- \end{bmatrix} \tag{1}$$

While the voltage on the X-terminal follows the difference in voltages of terminals Y_1 and Y_2, a current injected at the X-terminal is replicated by a factor k to the Z-terminals. For the Z^+ terminal, the direction of the conveyed current is the same as that of the current flowing in the X-terminal whereas for the Z^- terminal, the current flows in the opposite direction. Ideally, k is unity.

One possible CMOS realization of the DVCC is shown in Fig. 2 [6]. As can be seen, the current at Z^+ port will be the same as the current in the X terminal and the current at the Z^- terminal will have the same magnitude but opposite direction as the X port current.

Although both Z^+ and Z^- types of current outputs are mentioned in (1), the DVCCs used in the proposed network use only Z^+ type of outputs. Therefore, we next describe the proposed digitally controlled DVCC with only Z^+ outputs. The technique is to control the current transfer gain parameter k of the DVCC by replacing the Z terminal transistors of the DVCC with transistor arrays associated with

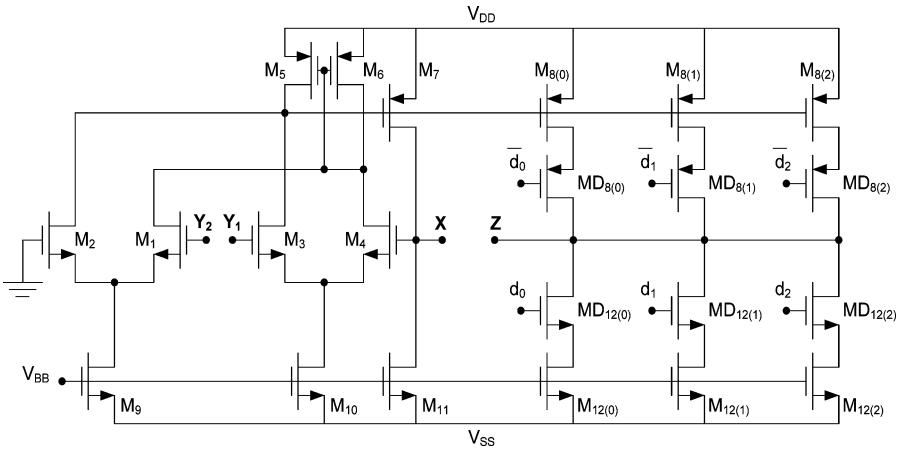

Fig. 3 CMOS realization of Digitally Controlled DVCC with gain k

switches [4]. The gain parameter k can take values from 1 to $(2^n - 1)$, where n represents the number of transistor arrays. Actually, the transistor arrays implement a current summing network (CSN) at the Z terminal. The circuit of DC-DVCC obtained after suitable modifications in the circuit of Fig. 2 is presented in Fig. 3.

The CSN consists of n transistor pairs, whose NMOS and PMOS aspect ratios are given by:

$$\text{NMOS:} \quad \left(\frac{W}{L}\right)_i = 2^i \left(\frac{W}{L}\right)_{11}, \quad i = 0, 1, 2, \ldots, (n-1) \tag{2}$$

$$\text{PMOS:} \quad \left(\frac{W}{L}\right)_i = 2^i \left(\frac{W}{L}\right)_{7}, \quad i = 0, 1, 2, \ldots, (n-1) \tag{3}$$

Therefore, the current at the Z terminal, assumed flowing out of the DC-DVCC, can be expressed by

$$I_Z = \sum_{i=0}^{n-1} d_i 2^i (I_7 - I_{11}) \tag{4}$$

Therefore, the proposed DC-DVCC provides a current transfer gain equal to

$$k = \frac{I_Z}{I_X} = \frac{\sum_{i=0}^{n-1} d_i 2^i (I_7 - I_{11})}{(I_7 - I_{11})} = \sum_{i=0}^{n-1} d_i 2^i \tag{5}$$

Parameter d_i represents the digital code-bit applied to the ith branch in the CSN. Depending upon its value, it enables or disables the current to flow in that particular branch. It is instructive to note the numbering of the transistors in the CSN. Transistors labeled $M_{8(i)}$ and $M_{12(i)}$ refer to the PMOS and NMOS transistors in the CSN that have been put there in the place of their counterparts of Fig. 2. Transistors $MD_{8(i)}$ and $M_{D12(i)}$ are the actual digital control transistors as the digital control bits d_0, d_1 and d_2 are applied at their respective gate terminals.

For the DC-DVCC, comparator action can be achieved by putting $R_X \to 0$ i.e. by directly grounding the X-terminal [6]. For such a case, the current in the X-port will saturate and can be written as

$$I_X = I_m \tanh \beta(V_{Y_1} - V_{Y_2}) \tag{6}$$

where β is the open-loop gain of the comparator (practically very high), $\pm I_m$ are the saturated output current levels of the comparator and $V_1, V_2, \ldots, V_n$ are the neuron outputs. Equation (6) can also be written in an equivalent notation as

$$I_X = g V_m \tanh \beta(V_{Y_1} - V_{Y_2}) \tag{7}$$

where g is the transconductance from the input voltage ports (Y_1 and Y_2) to the output current port X and is governed by the resistance at the X port; and $\pm V_m$ are the biasing voltages of the DVCC-based comparator.

By virtue of DVCC action, this current will be transferred to the Z^+ ports as

$$I_Z^+ = k I_X = kg V_m \tanh \beta(V_{Y_1} - V_{Y_2}) \tag{8}$$

Therefore, the current at the Z terminal can be made a digitally controlled scaled replica of the X port current. This property will be utilized in the design of the multi-output DVCCs needed for the proposed circuit. It may be mentioned that multiple Z^+ outputs can be obtained by repeating the output stage comprising transistors $M_{8(i)}$ and $M_{12(i)}$.

3 Proposed Neural Network

Let the simultaneous linear equations to be solved are

$$\mathbf{AV} = \mathbf{B} \tag{9}$$

where

$$\mathbf{A} = \begin{bmatrix} a_{11} & a_{12} & \ldots & a_{1n} \\ a_{21} & a_{22} & \ldots & a_{2n} \\ \vdots & \vdots & \ldots & \vdots \\ a_{n1} & a_{n2} & \ldots & a_{nn} \end{bmatrix} \tag{10}$$

$$\mathbf{B} = \begin{bmatrix} b_1 \\ b_2 \\ \vdots \\ b_n \end{bmatrix} \tag{11}$$

$$\mathbf{V} = \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_n \end{bmatrix} \tag{12}$$

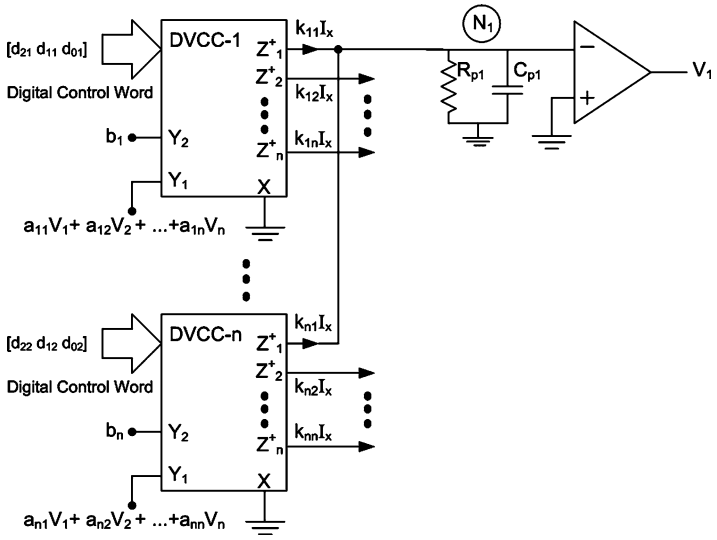

Fig. 4 First neuron of the proposed digitally programmable, feedback neural circuit to solve simultaneous linear equations in n-variables

where $V_1, V_2, \ldots, V_n$ are the variables and a_{ij} and b_i are constants. We will assume that the coefficient matrix **A** is invertible, and hence, the system of linear equations (9) is consistent and not under-determined. In other words, the linear system (9) has a uniquely determined solution.

The proposed neural network based circuit to solve the system of equations of (9) is presented in Fig. 4. As can be seen from Fig. 4, individual equations from the set of equations to be solved are passed through non-linear synapses which are realized using multi-output DC-DVCC based comparators.

The outputs of the comparators are fed to neurons having weighted inputs. These weighted neurons are realized by using opamps where the scaled currents coming from various comparators act as weights. R_{pi} and C_{pi} are the input resistance and capacitance of the opamp corresponding to the ith neuron. These parasitic components are included to model the dynamic nature of the opamp.

Node equation for node 'N_i' gives the equation of motion of the ith neuron as

$$C_{pi}\frac{du_i}{dt} = k_{1i}I_{X_1} + k_{2i}I_{X_2} + \cdots + k_{ni}I_{X_n} - u_i\left[\frac{1}{R_{pi}}\right] \tag{13}$$

where u_i is the internal state of the ith neuron and k_{ji} is the current scaling factor at the jth output of ith DVCC. Using (7) in (13) results in

$$\begin{aligned} C_{pi}\frac{du_i}{dt} &= k_{1i}gV_m \tanh\beta(a_{11}V_1 + a_{12}V_2 + \cdots + a_{1n}V_n - b_1) \\ &\quad + k_{2i}gV_m \tanh\beta(a_{21}V_1 + a_{22}V_2 + \cdots + a_{2n}V_n - b_2) + \cdots \\ &\quad + k_{ni}gV_m \tanh\beta(a_{n1}V_1 + a_{n2}V_2 + \cdots + a_{nn}V_n - b_n) - \frac{u_i}{R_{pi}} \end{aligned} \tag{14}$$

Moreover, as has been shown in Sect. 4, the network in Fig. 4 can be associated with an Energy Function 'E' given by

$$E = V_m \sum_{i=1}^{n} \ln\cosh\beta\left(\sum_{j=1}^{n} a_{ij} V_j - b_i\right) - \sum_{i=1}^{n} \frac{1}{R_i} \int_0^{V_i} u_i \, dV_i \tag{15}$$

From (15), it follows that

$$\begin{aligned}\frac{\partial E}{\partial V_1} &= V_m a_{11} \tanh\beta(a_{11}V_1 + a_{12}V_2 + \cdots + a_{1n}V_n - b_1) \\ &\quad + V_m a_{21} \tanh\beta(a_{21}V_1 + a_{22}V_2 + \cdots + a_{2n}V_n - b_2) + \cdots \\ &\quad + V_m a_{n1} \tanh\beta(a_{n1}V_1 + a_{n2}V_2 + \cdots + a_{nn}V_n - b_n) - u_1\left[\frac{1}{R_{p1}}\right]\end{aligned} \tag{16}$$

Also, if 'E' is the energy function, it must satisfy the following condition [8].

$$\frac{\partial E}{\partial V_i} = K_R C_{pi} \frac{du_i}{dt} \tag{17}$$

where K_R is a constant of proportionality having the dimensions of resistance and is normalized to $(1/g)$ for simplicity.

Comparing (14) and (16) according to (17) yields

$$\begin{bmatrix} k_{11} & k_{12} & \ldots & k_{1n} \\ k_{21} & k_{22} & \ldots & k_{2n} \\ \vdots & \vdots & \ldots & \vdots \\ k_{n1} & k_{n2} & \ldots & k_{nn} \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} & \ldots & a_{1n} \\ a_{21} & a_{22} & \ldots & a_{2n} \\ \vdots & \vdots & \ldots & \vdots \\ a_{n1} & a_{n2} & \ldots & a_{nn} \end{bmatrix} \tag{18}$$

4 Energy Function

4.1 Proof of the Energy Function

Differentiating the energy function of (15) w.r.t. V_i, we get

$$\begin{aligned}\frac{\partial E}{\partial V_i} &= V_m a_{1i} \tanh\beta(a_{11}V_1 + a_{12}V_2 + \cdots + a_{1n}V_n - b_1) \\ &\quad + V_m a_{2i} \tanh\beta(a_{21}V_1 + a_{22}V_2 + \cdots + a_{2n}V_n - b_2) + \cdots \\ &\quad + V_m a_{ni} \tanh\beta(a_{n1}V_1 + a_{n2}V_2 + \cdots + a_{nn}V_n - b_n) - \frac{u_i}{R_{pi}}\end{aligned} \tag{19}$$

Further, the time derivative of the energy function is given by

$$\frac{dE}{dt} = \sum_{i=1}^{N} \frac{\partial E}{\partial V_i} \frac{dV_i}{dt} = \sum_{i=1}^{N} \frac{\partial E}{\partial V_i} \frac{dV_i}{du_i} \frac{du_i}{dt} \tag{20}$$

Using (12) in (15) we get

$$\frac{dE}{dt} = \sum_{i=1}^{N} KC_i \left(\frac{du_i}{dt}\right)^2 \frac{dV_i}{du_i} \tag{21}$$

The transfer characteristics of the output opamp used in Fig. 4 implements the activation function of the neuron. With u_i being the inverting terminal, it is monotonically decreasing and it can be seen that [8]

$$\frac{dV_i}{du_i} \leq 0 \tag{22}$$

thereby resulting in

$$\frac{dE}{dt} \leq 0 \tag{23}$$

with the equality being valid for

$$\frac{du_i}{dt} = 0; \quad \text{for all } i \tag{24}$$

Equation (23) shows that the energy function can never increase with time which is one of the conditions for a valid energy function. The second criterion viz. the energy function must have a lower bound is also satisfied for the circuit of Fig. 4 wherein it may be seen that $V_1, V_2, \ldots, V_n$ are all bounded (as they are the outputs of opamps) amounting to 'E', as given in (15), having a defined lower bound.

4.2 Stable States of the Network

Convergence of the network to the global minimum of the energy function, which is exactly the solution of the set of linear equations, and the fact that there are no other minima, can be shown as follows.

For n variables, the second term in the energy function expression (15) is significant only near the saturating values of the opamp and is usually neglected [9]. The energy function can therefore be expressed as

$$E = V_m \sum_{i=1}^{n} \ln\cosh\beta \left(\sum_{j=1}^{n} a_{ij} V_j - b_i\right) \tag{25}$$

from which it follows that

$$\begin{aligned}\frac{\partial E}{\partial V_1} = {} & V_m a_{11} \tanh\beta(a_{11}V_1 + a_{12}V_2 + \cdots + a_{1n}V_n - b_1) \\ & + V_m a_{21} \tanh\beta(a_{21}V_1 + a_{22}V_2 + \cdots + a_{2n}V_n - b_2) + \cdots \\ & + V_m a_{n1} \tanh\beta(a_{n1}V_1 + a_{n2}V_2 + \cdots + a_{nn}V_n - b_n)\end{aligned} \tag{26}$$

$$\frac{\partial E}{\partial V_2} = V_m a_{12} \tanh\beta(a_{11}V_1 + a_{12}V_2 + \cdots + a_{1n}V_n - b_1) + V_m a_{22} \tanh\beta(a_{21}V_1 + a_{22}V_2 + \cdots + a_{2n}V_n - b_2) + \cdots + V_m a_{n2} \tanh\beta(a_{n1}V_1 + a_{n2}V_2 + \cdots + a_{nn}V_n - b_n) \tag{27}$$

$$\vdots$$

$$\frac{\partial E}{\partial V_n} = V_m a_{1n} \tanh\beta(a_{11}V_1 + a_{12}V_2 + \cdots + a_{1n}V_n - b_1) + V_m a_{2n} \tanh\beta(a_{21}V_1 + a_{22}V_2 + \cdots + a_{2n}V_n - b_2) + \cdots + V_m a_{nn} \tanh\beta(a_{n1}V_1 + a_{n2}V_2 + \cdots + a_{nn}V_n - b_n) \tag{28}$$

For a stationary point, we have

$$\left.\begin{aligned} \frac{\partial E}{\partial V_1} &= 0 \\ \frac{\partial E}{\partial V_2} &= 0 \\ &\vdots \\ \frac{\partial E}{\partial V_n} &= 0 \end{aligned}\right\} \tag{29}$$

which yields

$$a_{11} \tanh\beta(a_{11}V_1 + a_{12}V_2 + \cdots + a_{1n}V_n - b_1) + a_{21} \tanh\beta(a_{21}V_1 + a_{22}V_2 + \cdots + a_{2n}V_n - b_2) + \cdots + a_{n1} \tanh\beta(a_{n1}V_1 + a_{n2}V_2 + \cdots + a_{nn}V_n - b_n) = 0 \tag{30}$$

$$a_{12} \tanh\beta(a_{11}V_1 + a_{12}V_2 + \cdots + a_{1n}V_n - b_1) + a_{22} \tanh\beta(a_{21}V_1 + a_{22}V_2 + \cdots + a_{2n}V_n - b_2) + \cdots + a_{n2} \tanh\beta(a_{n1}V_1 + a_{n2}V_2 + \cdots + a_{nn}V_n - b_n) = 0 \tag{31}$$

$$\vdots$$

$$a_{1n} \tanh\beta(a_{11}V_1 + a_{12}V_2 + \cdots + a_{1n}V_n - b_1) + a_{2n} \tanh\beta(a_{21}V_1 + a_{22}V_2 + \cdots + a_{2n}V_n - b_2) + \cdots + a_{nn} \tanh\beta(a_{n1}V_1 + a_{n2}V_2 + \cdots + a_{nn}V_n - b_n) = 0 \tag{32}$$

Denoting

$$\tanh\beta(a_{11}V_1 + a_{12}V_2 + \cdots + a_{1n}V_n - b_1) = A_1 \tag{33}$$

$$\tanh\beta(a_{21}V_1 + a_{22}V_2 + \cdots + a_{2n}V_n - b_2) = A_2 \tag{34}$$

$$\vdots$$

$$\tanh\beta(a_{n1}V_1 + a_{n2}V_2 + \cdots + a_{nn}V_n - b_n) = A_n \tag{35}$$

Therefore, for a stationary point we have

$$\begin{bmatrix} a_{11} & a_{12} & \dots & a_{1n} \\ a_{21} & a_{22} & \dots & a_{2n} \\ \vdots & \vdots & \dots & \vdots \\ a_{n1} & a_{n2} & \dots & a_{nn} \end{bmatrix} \begin{bmatrix} A_1 \\ A_2 \\ \vdots \\ A_n \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ \vdots \\ 0 \end{bmatrix} \tag{36}$$

This is a homogeneous system of linear equations in variables $A_1, A_2, \dots, A_n$. Since the coefficient matrix of the set of (36) is the same as that of (9) which is invertible, it follows that (36) will have a uniquely determined solution which is the trivial solution of the homogeneous system.

Therefore,

$$\begin{bmatrix} A_1 \\ A_2 \\ \vdots \\ A_n \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ \vdots \\ 0 \end{bmatrix} \tag{37}$$

which results in

$$\left.\begin{aligned} &a_{11}V_1 + a_{12}V_2 + \cdots + a_{1n}V_n - b_1 = 0 \\ &a_{21}V_1 + a_{22}V_2 + \cdots + a_{2n}V_n - b_2 = 0 \\ &\vdots \\ &a_{n1}V_1 + a_{n2}V_2 + \cdots + a_{nn}V_n - b_n = 0 \end{aligned}\right\} \tag{38}$$

Thus, the energy function of the proposed neural network has a unique stationary point which coincides exactly with the solution of the given system of linear equations.

This energy function can be visualized in three dimensions for a two-variable problem and is shown in Fig. 5. From the plot, it can be seen that there exists only one minimum, to which the network must converge.

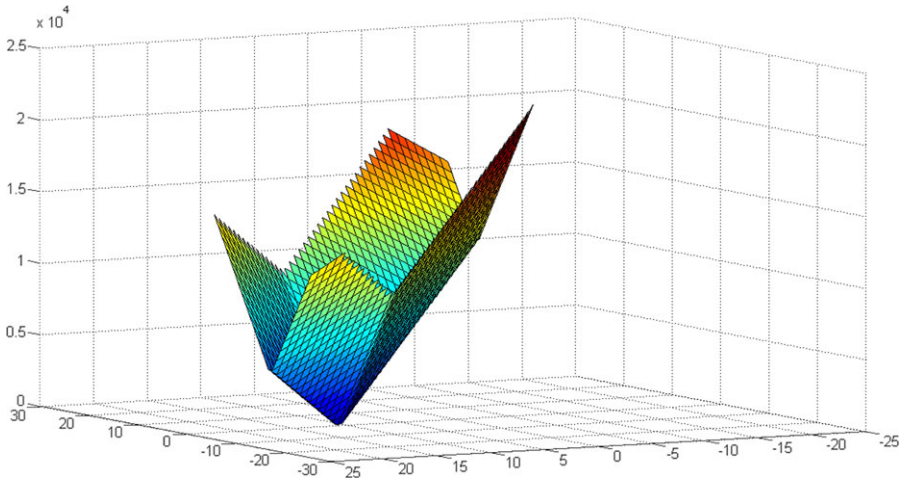

Fig. 5 Typical energy function plot for a two-variable problem

5 PSPICE Simulation Results

The proposed circuit was tested using PSPICE simulation program for solving sets of two, three, four, five and 10 simultaneous linear equations. The application of the proposed circuit to a chosen three-variable problem (39) is presented below.

$$\begin{bmatrix} 2 & 1 & 1 \\ 3 & 2 & 1 \\ 1 & 1 & 2 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} 5 \\ 10 \\ 6 \end{bmatrix} \tag{39}$$

The circuit to solve (39) as obtained from Fig. 4 is presented in Fig. 6. The values of the current scaling coefficients k_{ji} are given as

$$\begin{bmatrix} k_{11} & k_{12} & k_{13} \\ k_{21} & k_{22} & k_{23} \\ k_{31} & k_{32} & k_{33} \end{bmatrix} = \begin{bmatrix} 2 & 1 & 1 \\ 3 & 2 & 1 \\ 1 & 1 & 2 \end{bmatrix} \tag{40}$$

For implementing these values of k_{ji} appropriate values of the control words were selected. For the first DC-DVCC, the three control words were kept as [0 1 0], [0 0 1]

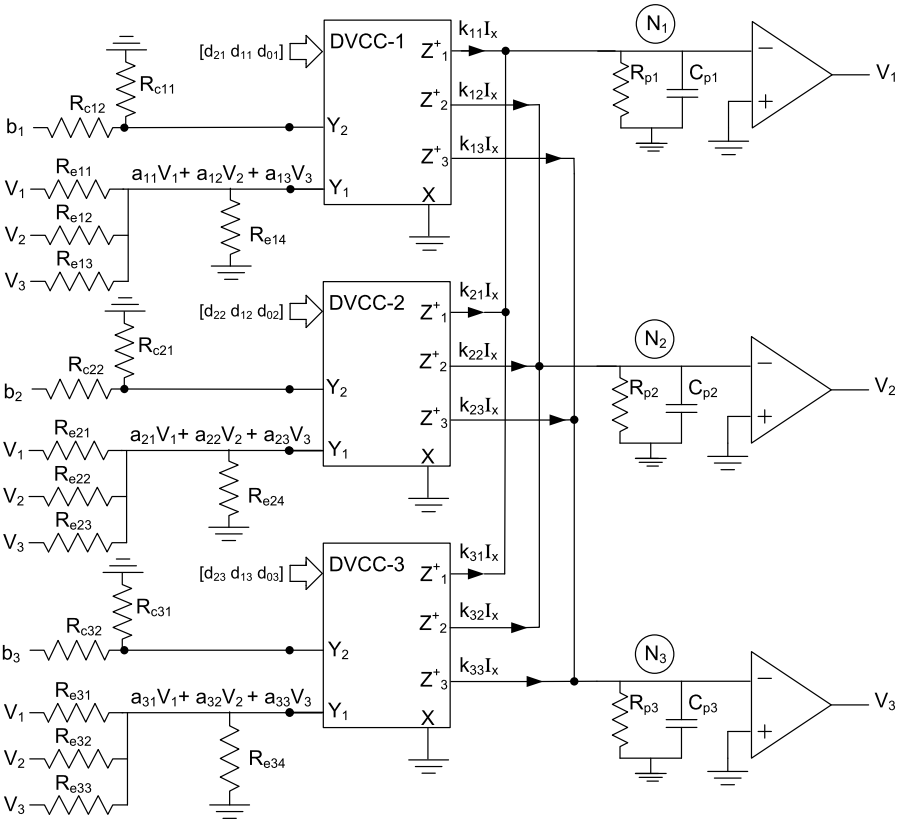

Fig. 6 The proposed circuit applied to a three-variable problem

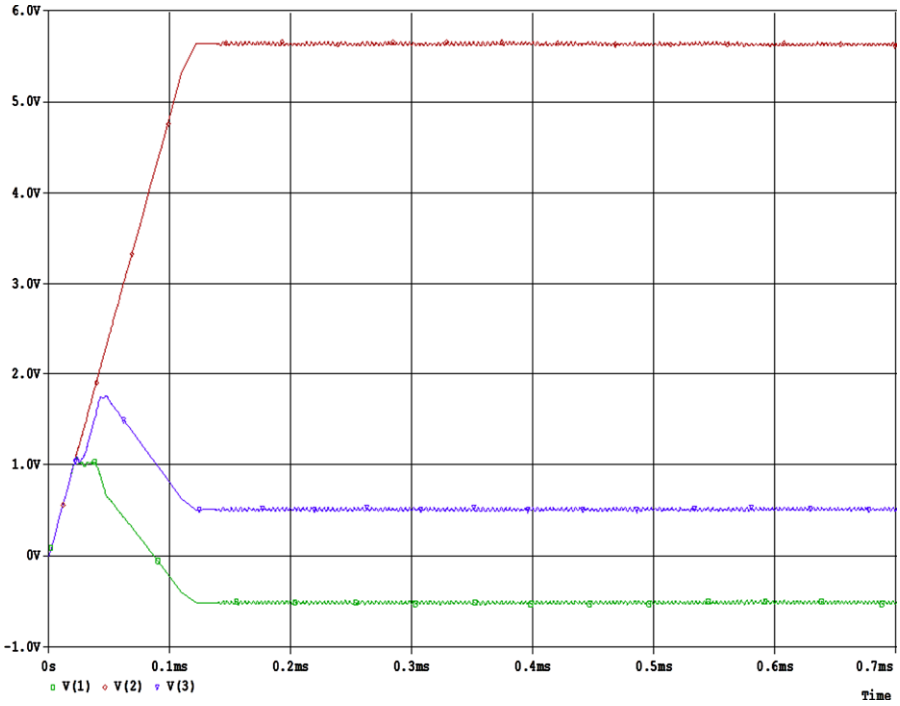

Fig. 7 Simulation results for the chosen three-variable problem

and [0 0 1]. Similarly, the control words for the second DC-DVCC were [0 1 1], [0 1 0] and [0 0 1]. Finally, for the third DC-DVCC the control words were [0 0 1], [0 0 1] and [0 1 0]. Thus, a proper selection of the control words can be used to achieve any current scaling factor between 1 and 7 and therefore this particular realization is restricted to solving systems of equations with coefficients in that range. However, that range may be widened further by having four control bits in the CSN.

As can be seen, some additional circuitry is needed to generate the inputs to the non-linear synapses. Routine analysis yields the following values of the resistors at the input of the non-linear synapses.

$$R_{e11} = 2.5\ \text{K}, \quad R_{e12} = R_{e13} = R_{e14} = 5\ \text{K}, \quad R_{e21} = 3.33\ \text{K}, \quad R_{e22} = 5\ \text{K},$$
$$R_{e23} = 10\ \text{K}, \quad R_{e24} = 2.5\ \text{K}, \quad R_{e31} = R_{e32} = 6\ \text{K}, \quad R_{e33} = R_{e34} = 3\ \text{K},$$
$$R_{c11} = R_{c21} = R_{c31} = 1\ \text{K}, \quad R_{c12} = 4\ \text{K}, \quad R_{c22} = 9\ \text{K}, \quad R_{c32} = 5\ \text{K}.$$

Algebraic analysis of (39) gives the solution as $V_1 = -0.5$ V, $V_2 = 5.5$ V and $V_3 = 0.5$ V. The results of PSPICE simulation of the circuit of Fig. 6, shown in Fig. 7, are found to match perfectly with the algebraic solution. The initial node voltages were kept as $V(1) = 10$ mV, $V(2) = -10$ mV and $V(3) = 20$ mV. The circuit for DVCC was taken from [6] and standard 0.5 micron CMOS parameters were used for simulation purposes. The DVCCs were biased with ± 2.5 V supplies. For the opamp, use was made of the LMC7101A CMOS opamp from National Semiconductor. The sub-circuit file for this opamp is available in Orcad Model Library. The

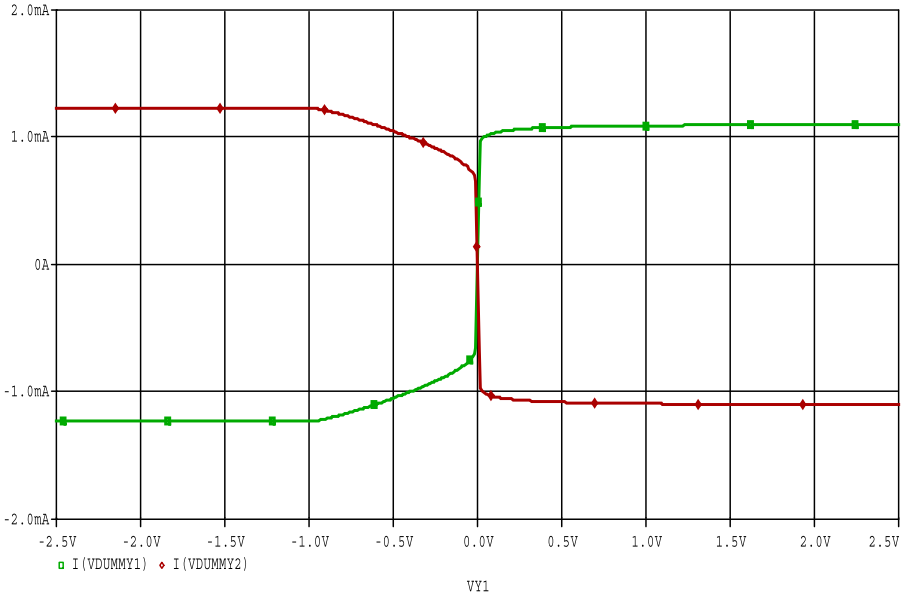

Fig. 8 Transfer characteristics of the DC-DVCC used to realize the comparator

biasing voltages for the opamps were taken to be ±15 V. The transfer characteristics of the DVCC-based comparator, shown in Fig. 8, were also plotted using SPICE simulation and value of 'β' was found to be 2.4×10^3.

The proposed circuit was further tested in PSPICE for solving systems of linear equations in two, four, five, and ten variables. Results of simulation runs for these problems are presented in Table 1. Each of the simulations was run using various initial conditions in the millivolt range. As can be seen from Table 1, the proposed network always converges to the solution of the given system of linear equations. As can be seen, the obtained results are quite near the algebraic solutions with the maximum error being approximately 6% and the average error being 0.49%.

6 Performance Evaluation

This section deals with the effect of component mismatches and device non-idealities on the accuracy of the solution obtained from the circuit proposed.

If the proposed circuit is implemented using discrete resistances, variations in the values of the resistances need to be considered keeping in mind the tolerances associated with discrete resistors. However, if the proposed network is targeted for monolithic integration, *random* variations in the resistance values need not be considered. In that case, all the resistances are expected to deviate from their assigned values by the same factor [7]. Therefore, a worthy performance appraisal of the circuit could be obtained by testing the circuit with all resistances having the same percentage deviation from their assigned values. Such an assessment of the quality of the obtained solution is presented in Table 2 from which it can be seen that the percentage error

Table 1 PSPICE Simulation results for the proposed circuit applied to different systems of linear equations

[**A**]	[**B**]	Algebraic Solution [V]	Simulated Results (Using PSPICE) [V]	Percentage Error in the solution (%)
$\begin{bmatrix} 1 & 2 \\ 2 & 1 \end{bmatrix}$	$\begin{bmatrix} 3.5 \\ 4 \end{bmatrix}$	$\begin{bmatrix} 1.5 \\ 1 \end{bmatrix}$	$\begin{bmatrix} 1.51 \\ 1.02 \end{bmatrix}$	$\begin{bmatrix} -0.66 \\ -2.00 \end{bmatrix}$
$\begin{bmatrix} 2 & 1 & 1 \\ 3 & 2 & 1 \\ 1 & 1 & 1 \end{bmatrix}$	$\begin{bmatrix} 5 \\ 10 \\ 6 \end{bmatrix}$	$\begin{bmatrix} -0.5 \\ 5.5 \\ 0.5 \end{bmatrix}$	$\begin{bmatrix} -0.52 \\ 5.54 \\ 0.48 \end{bmatrix}$	$\begin{bmatrix} -4.00 \\ -0.72 \\ 4.00 \end{bmatrix}$
$\begin{bmatrix} 2 & 3 & 6 & 1 \\ 3 & 2 & 5 & 4 \\ 2 & 5 & 5 & 2 \\ 2 & 4 & 2 & 5 \end{bmatrix}$	$\begin{bmatrix} 48.75 \\ 67.5 \\ 54 \\ 59.25 \end{bmatrix}$	$\begin{bmatrix} 3.5 \\ 1.5 \\ 5 \\ 7.25 \end{bmatrix}$	$\begin{bmatrix} 3.51 \\ 1.53 \\ 5.09 \\ 7.19 \end{bmatrix}$	$\begin{bmatrix} -0.28 \\ -2.00 \\ -1.80 \\ 0.83 \end{bmatrix}$
$\begin{bmatrix} 2 & 3 & 9 & 2 & 5 \\ 2 & 6 & 9 & 9 & 5 \\ 2 & 6 & 2 & 4 & 5 \\ 2 & 4 & 7 & 8 & 3 \\ 5 & 3 & 6 & 3 & 5 \end{bmatrix}$	$\begin{bmatrix} -54.9 \\ -91.0 \\ -54.9 \\ -74.8 \\ -70.0 \end{bmatrix}$	$\begin{bmatrix} -6.7 \\ -4.3 \\ -2.8 \\ -3.3 \\ 0.64 \end{bmatrix}$	$\begin{bmatrix} -6.65 \\ -4.33 \\ -2.63 \\ -3.19 \\ 0.63 \end{bmatrix}$	$\begin{bmatrix} 0.75 \\ -0.69 \\ 6.07 \\ 3.33 \\ 1.56 \end{bmatrix}$
$\begin{bmatrix} 1 & 2 & 1 & 3 & 4 & 2 & 1 & 1 & 1 & 2 \\ 2 & 1 & 1 & 3 & 1 & 2 & 2 & 1 & 2 & 3 \\ 1 & 1 & 4 & 3 & 3 & 1 & 1 & 4 & 4 & 1 \\ 4 & 2 & 1 & 5 & 3 & 3 & 1 & 1 & 2 & 2 \\ 1 & 1 & 5 & 1 & 2 & 1 & 2 & 2 & 5 & 2 \\ 3 & 3 & 1 & 2 & 1 & 1 & 5 & 2 & 1 & 1 \\ 5 & 5 & 1 & 4 & 1 & 1 & 3 & 4 & 2 & 2 \\ 1 & 1 & 1 & 2 & 2 & 2 & 3 & 3 & 4 & 1 \\ 4 & 2 & 2 & 1 & 3 & 2 & 5 & 4 & 3 & 2 \\ 1 & 2 & 3 & 1 & 2 & 3 & 1 & 2 & 3 & 4 \end{bmatrix}$	$\begin{bmatrix} 10 \\ -11 \\ 10 \\ 2 \\ -7 \\ -9 \\ -8 \\ -3 \\ -3 \\ 7 \end{bmatrix}$	$\begin{bmatrix} -2 \\ 1 \\ 3 \\ -1 \\ 2 \\ 7 \\ -3 \\ 4 \\ -5 \\ -4 \end{bmatrix}$	$\begin{bmatrix} -1.91 \\ 1.04 \\ 3.05 \\ -0.95 \\ 1.94 \\ 7.04 \\ -3.06 \\ 3.99 \\ -4.91 \\ -3.95 \end{bmatrix}$	$\begin{bmatrix} 4.50 \\ -4.00 \\ -1.66 \\ 5.00 \\ 3.00 \\ -0.57 \\ -2.00 \\ 0.25 \\ 1.80 \\ 1.25 \end{bmatrix}$

Table 2 Effect of variation in resistances on the obtained results

Percentage Variation in Resistances	Simulated Results (Using PSPICE) [V]	Percentage Error in the Solution (%)
+2%	$\begin{bmatrix} -0.508 \\ 5.602 \\ 0.499 \end{bmatrix}$	$\begin{bmatrix} +1.6 \\ +1.85 \\ -0.2 \end{bmatrix}$
+5%	$\begin{bmatrix} -0.509 \\ 5.619 \\ 0.501 \end{bmatrix}$	$\begin{bmatrix} +1.8 \\ +2.16 \\ +0.2 \end{bmatrix}$
+10%	$\begin{bmatrix} -0.514 \\ 5.681 \\ 0.507 \end{bmatrix}$	$\begin{bmatrix} +2.8 \\ +3.29 \\ +1.4 \end{bmatrix}$
−2%	$\begin{bmatrix} -0.507 \\ 5.601 \\ 0.505 \end{bmatrix}$	$\begin{bmatrix} +1.4 \\ +1.83 \\ +1 \end{bmatrix}$
−5%	$\begin{bmatrix} -0.518 \\ 5.679 \\ 0.506 \end{bmatrix}$	$\begin{bmatrix} +3.6 \\ +3.25 \\ +1.2 \end{bmatrix}$
−10%	$\begin{bmatrix} -0.516 \\ 5.678 \\ 0.504 \end{bmatrix}$	$\begin{bmatrix} +3.2 \\ +3.23 \\ +0.8 \end{bmatrix}$

Table 3 Effect of gains of the DVCC-based comparators on the solution quality

X-terminal resistances of the DVCCs (Ω)	Simulated Results (Using PSPICE) [V]	Percentage Error in the solution (%)
5	$\begin{bmatrix} -0.512 \\ 5.610 \\ 0.500 \end{bmatrix}$	$\begin{bmatrix} 2.4 \\ 2.0 \\ 0.0 \end{bmatrix}$
10	$\begin{bmatrix} -0.514 \\ 5.617 \\ 0.510 \end{bmatrix}$	$\begin{bmatrix} 2.8 \\ 2.1 \\ 2.00 \end{bmatrix}$
20	$\begin{bmatrix} -0.520 \\ 5.620 \\ 0.511 \end{bmatrix}$	$\begin{bmatrix} -4.00 \\ 2.18 \\ 2.2 \end{bmatrix}$

in the solution varies with the percentage errors specified in the values of the resistances and even for $\pm 10\%$ variation in the values of the resistors, the solution point changes by approximately 3%.

Further, the gains of the DVCC-based comparators were varied to investigate their effect on the solution quality. Toward that end, a resistance was connected between the X-terminal of each DVCC and ground. Ideally, these resistances were assumed to have zero value. However, by assigning different values to these resistances, the gains of the DVCCs were varied. The solutions, as obtained for the three-variable problem of Fig. 6, are presented in Table 3. It can be seen that small variations in the gains of the comparators do not affect the quality of the solution.

Next, the effect of offset voltages in the DVCC-based comparators was explored. Offset voltages were applied at the Y_2 inputs of the DVCCs of Fig. 6 and the results of PSPICE simulations were compared with the algebraic solution as given in Table 4. As can be seen, the offset voltages of the comparators do not affect the obtained solutions to any appreciable extent. However, the error does tend to increase with increasing offset voltages.

Finally, offset voltages for the opamps were also considered. Offset voltages were applied at the non-inverting inputs of the opamps of Fig. 6 and the results of PSPICE simulations were compared with the algebraic solution as given in Table 5. As can be seen, the offset voltages of the opamps have little effect on the obtained solutions.

7 Conclusion

In this paper we have described a novel approach to solve n simultaneous linear equations in n variables, which uses n neurons and n synapses. Each neuron requires one opamp and each synapse is implemented using one comparator. The comparators were realized using a new digitally controlled DVCC. This results in significant reduction in hardware over the existing schemes [1, 5, 10, 11]. From VLSI implementation point of view, use of CMOS DC-DVCCs and opamps facilitates viability for monolithic integration.

The working of the proposed network was verified using PSPICE for various sample problem sets of two to 10 simultaneous linear equations. While the simulation

Table 4 Effect of offset voltages of the DVCC-based comparators on the solution quality

Offset Voltage applied at Y_2 input of the DVCCs (mV)	Simulated Results (Using PSPICE) [V]	Percentage Error in the Solution (%)
−5	$\begin{bmatrix} -0.498 \\ 5.615 \\ 0.497 \end{bmatrix}$	$\begin{bmatrix} -0.4 \\ 2.09 \\ -0.6 \end{bmatrix}$
−10	$\begin{bmatrix} -0.505 \\ 5.620 \\ 0.506 \end{bmatrix}$	$\begin{bmatrix} 1.0 \\ 2.18 \\ 1.2 \end{bmatrix}$
−15	$\begin{bmatrix} -0.512 \\ 5.631 \\ 0.511 \end{bmatrix}$	$\begin{bmatrix} 2.4 \\ 2.38 \\ 2.2 \end{bmatrix}$
+5	$\begin{bmatrix} -0.496 \\ 5.611 \\ 0.494 \end{bmatrix}$	$\begin{bmatrix} -0.8 \\ 2.01 \\ -1.2 \end{bmatrix}$
+10	$\begin{bmatrix} -0.503 \\ 5.627 \\ 0.508 \end{bmatrix}$	$\begin{bmatrix} 0.6 \\ 2.30 \\ 1.6 \end{bmatrix}$
+15	$\begin{bmatrix} -0.519 \\ 5.629 \\ 0.510 \end{bmatrix}$	$\begin{bmatrix} 3.8 \\ 2.34 \\ 2 \end{bmatrix}$

Table 5 Effect of offset voltages of opamps on solution quality

Offset Voltage applied at the non-inverting input of opamps (mV)	Simulated Results (Using PSPICE) [V]	Percentage Error in the Solution (%)
−5	$\begin{bmatrix} -0.494 \\ 5.617 \\ 0.507 \end{bmatrix}$	$\begin{bmatrix} -1.2 \\ 2.12 \\ 1.4 \end{bmatrix}$
−10	$\begin{bmatrix} -0.504 \\ 5.581 \\ 0.510 \end{bmatrix}$	$\begin{bmatrix} 0.8 \\ 1.47 \\ 2 \end{bmatrix}$
−15	$\begin{bmatrix} -0.514 \\ 5.543 \\ 0.491 \end{bmatrix}$	$\begin{bmatrix} 2.8 \\ 0.78 \\ -1.8 \end{bmatrix}$
+5	$\begin{bmatrix} -0.499 \\ 5.642 \\ 0.497 \end{bmatrix}$	$\begin{bmatrix} -0.2 \\ 2.58 \\ -0.6 \end{bmatrix}$
+10	$\begin{bmatrix} -0.506 \\ 5.668 \\ 0.505 \end{bmatrix}$	$\begin{bmatrix} 1.2 \\ 3.05 \\ 1.0 \end{bmatrix}$
+15	$\begin{bmatrix} -0.512 \\ 5.693 \\ 0.507 \end{bmatrix}$	$\begin{bmatrix} 2.4 \\ 3.51 \\ 1.4 \end{bmatrix}$

results confirm the validity of the approach, issues such as the network response to a system of equations which do *not* have a unique solution are yet to be explored. It may be mentioned that the technique can be extended to the standard linear and quadratic programming problems.

References

1. A. Cichocki, R. Unbehauen, Neural networks for solving systems of linear equations and related problems. IEEE Trans. Circuits Syst.—I **39**(2), 124–138 (1992)
2. H.O. Elwan, A.M. Soliman, Novel CMOS differential voltage current conveyor and its applications. IEE Proc. Circuits Devices Syst. **144**(3), 195–200 (1997)
3. J.L. Gustafson, The quest for linear equation solvers and the invention of electronic digital computing, in *Proc. JVA'06, IEEE John Vincent Atanasoff 2006 International Symposium on Modern Computing* (2006)
4. T.M. Hassan, S.A. Mahmoud, Fully programmable universal filter with independent gain-ω_o-Q control based on new digitally programmable CMOS CCII. J. Circuits Syst. Comput. **18**(5), 875–897 (2009)
5. D. Jiang, Analog computing for real-time solution of time-varying linear equations. Proc. ICCCAS **2**, 27–29 (2004)
6. S. Maheshwari, A canonical voltage-controlled VM-APS with a grounded capacitor. Circuits Syst. Signal Process. **27**, 123–132 (2008)
7. J.D. Plummer, M.D. Deal, P.B. Griffin, *Silicon VLSI Technology: Fundamentals, Practices and Modeling* (Pearson Education, Upper Saddle River, 2009)
8. S.A. Rahman, Jayadeva, S.C. Duttaroy, Neural network approach to graph colouring. Electron. Lett. **35**(14), 1173–1175 (1999)
9. D.W. Tank, J.J. Hopfield, Simple neural optimization networks: an A/D converter, signal decision network, and linear programming circuit. IEEE Trans. Circuits Syst. CAS **33**(5), 533–541 (1986)
10. J. Wang, Electronic realization of recurrent neural network for solving simultaneous linear equations. Electron. Lett. **28**(5), 493–495 (1992)
11. Y. Xia, J. Wang, D.L. Hung, Recurrent neural networks for solving linear inequalities and equations. IEEE Trans. Circuits Syst.—I **46**(4) (1999)