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Bulk-Driven Current Differencing Transconductance Amplifier

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Abstract Low-voltage (LV) low-power (LP) integrated circuit design is becoming a leading trend in VLSI technology, particularly in special portable applications. In this paper, the principle of a bulk-driven MOS transistor is employed in the design of a novel LV LP current differencing transconductance amplifier (CDTA). Designs in the 0.25 μm CMOS technology have been verified via PSpice simulation. The supply voltages are only ±0.6 V.

Keywords Bulk-driven CMOS · CDTA · PSpice

1 Introduction

Integrated circuit design is currently directed to low-voltage (LV) and low-power (LP) applications, particularly in the case of portable systems where a low supply voltage, sometimes given by only a single cell battery, is used [10]. In order to overcome the well-known limitations of the traditional techniques based on voltage-feedback operational amplifiers (op amps), this LV LP approach is also combined with the

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current-mode approach [39]. Such devices then exhibit a low power consumption and reasonable dynamic behavior, maintaining a balanced trade-off between speed and accuracy.

An important factor concerning LV LP analog circuits is that the threshold voltages of future standard CMOS technologies are not expected to decrease much below what is available today. To overcome the threshold voltage, a bulk-driven MOS transistor (MOST) can be used. It is well known that a reverse/forward bias on the well-source junction increases/decreases the threshold voltage [19]. The operation of the bulk-driven MOST is conformable with junction gate field effect transistors (JFETs). To enable bulk driving, one must first bias the gate to form a conduction channel inversion layer by connecting the gate terminal to a fixed voltage that is sufficient to form an inversion layer [20].

That is why the bulk-driven transistor can be a good solution to overcome the threshold voltage limitation. Because it is a depletion-type device, it can work under negative, zero, or even slightly positive biasing conditions [6].

Recent publications describe various implementations of a bulk-driving technique in signal processing LV LP applications [16, 21, 22, 29, 44]. Several LV active elements have been designed using this technique, such as voltage followers [11, 43], op amps [27], and operational transconductance amplifiers (OTAs) [7, 9, 24, 28].

In [2], a novel circuit component, namely the current differencing transconductance amplifier (CDTA) has been introduced. As in the CDBA (current differencing buffered amplifier) [1] and the OTRA (operational transresistance amplifier) [8], the input stage is formed by the CDU (current differencing unit) [3]. Providing input and output signals as currents, the CDTA seems to be a promising building block for current-mode signal processing. A number of CDTA applications have been reported in the literature [4, 5, 12–14, 17, 18, 25, 26, 30–38, 40–42]. Both CMOS and bipolar implementations of the CDTA have been proposed [13, 14, 34, 37, 38, 41, 42].

An analysis of the above papers shows that every concrete CDTA implementation is a compromise between several requirements which are in mutual contradiction, particularly DC precision and speed or low supply voltages and dynamic range. Some CDTAs designed in the CMOS technologies are characterized by rather high supply voltages, high power dissipation, and high R_p and R_n resistances ($\pm$2.5 V/1.61 mW/7 kΩ in [13, 14], $\pm$2.5 V/4.4 mW/600 Ω in [41]). These resistances are designed extremely low (below 2 Ω) in [4, 37] but also at the cost of high power dissipation (6.31 mW in [4] and 19 mW in [37]). The bipolar implementation of the CDTA in [38] also provides very low R_p and R_n resistances, of about 4.5 Ω, but the power dissipation is high, almost 10 mW, with a large current offset of 8 μA. Probably the only hitherto published CDTA with a power consumption of less than 1 mW is the simple structure in [42], in which flipped voltage followers are used in the current mirrors of the input stage. With supply voltages of $\pm$0.75 V, the power consumption is only 0.37 mW, with a 54 μA bias current and a 0.4 μA current offset. However, note that the CDTA structure in [42] is a simplified version containing only 18 transistors, without any auxiliary circuits, e.g., for DC biasing. That is why higher power dissipation is expected for a complete topology.

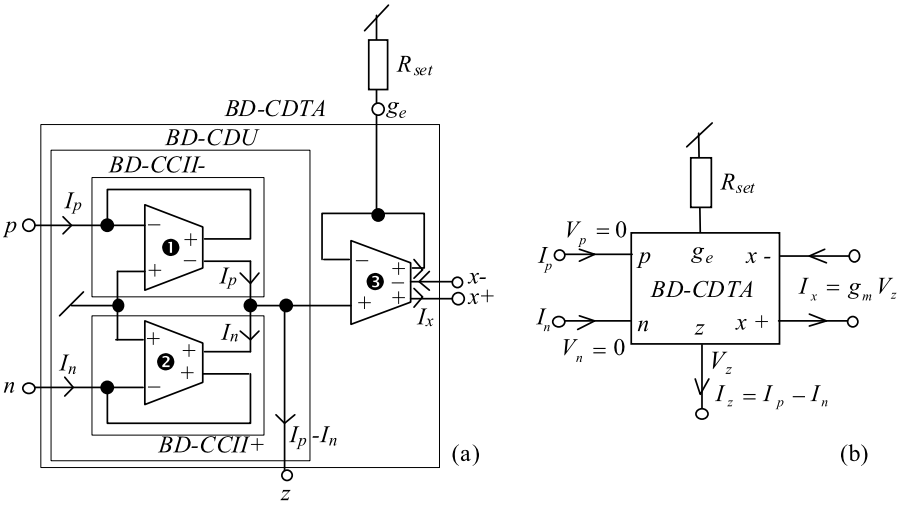

Fig. 1 (**a**) CDTA built from bulk-driven OTAs, (**b**) its schematic symbol

In order to design a low-power CDTA with extra-low supply voltages and with power consumption below ca. 150 μW, these extreme requirements can be fulfilled only at the cost of speed and accuracy. The bulk-driving (BD) technique can be used as a well-known representative of low-power but also low-frequency applications.

Based on the previously reported results from [1–5, 8, 12–14, 17, 18, 25, 26, 31–36, 40], the CDU, an important input part of the CDTA, can be advantageously substituted either by the technique of current followers and mirrors [13] or by a suitable connection of two current conveyors of the second generation (CCIIs) [30]; the CCII can be built up from an OTA with a sufficiently high transconductance g_m [10]. In this way, the internal structure can be designed on the basis of three OTAs.

In this paper, the latter method is used since it is more suitable for the implementation of the bulk-driving principle. As a result, the LV LP CDTA is designed, based on the concept of a bulk-driven OTA. In contrast to conventional gate-driven CMOS structures, such a CDTA uses extra-low power supply voltages.

2 CDTA Based on Bulk-Driving Principle

The conception of the bulk-driven CDTA (BD-CDTA) and its schematic symbol are shown in Fig. 1. The CDU is formed by two bulk-driven OTAs, each of them simulating the bulk-driven current conveyor (BD-CCII) of positive and negative types [10]. In comparison with the classical configuration employing two CCII+'s [1], this solution provides symmetrical paths of I_p and I_n currents. The impedance of the $p(n)$ terminal is given by the reciprocal value of the transconductance of OTA No. 1 (2). The difference current $I_z = I_p - I_n$ flows out of the z-terminal, and the corresponding voltage drop on an external impedance connected to this terminal is transformed into

Table 1 Transistor aspect ratios from Fig. 2

	W/L [μm/μm]
M1, M3, M10, M25	20/3
M4, M6, M11, M13, M26, M28	30/2
M2	10/3
M5, M7, M12, M14, M27, M29	4/2
M8, M15, M17, M19, M21, M23, M30, M32, M34, M36, M38	40/3
M9, M16, M18, M20, M22, M24, M31, M33, M35, M37, M39	16/2

x-terminal currents via OTA No. 3. Note that the number of BD-CDTA x-terminals can be arbitrary, with both directions of the corresponding currents. Two bidirectional $x+$ and $x-$ outputs of OTA No. 3 are shown in Fig. 1 as an example.

In order to make the transconductance of the output OTA stage adjustable, the idea of the CDeTA (current differencing external transconductance amplifier) [3] is applied here. OTA No. 3 is provided with negative feedback from the current output to the negative input terminal, and the transconductance is set via an external resistor R_{set}. Let us denote the self-transconductance of OTA3 by g_m. A simple analysis yields the value of total transconductance $g_{m,\text{set}}$ of the final OTA stage including R_{set} as

$$g_{m,\text{set}} = \frac{g_m}{1 + g_m R_{\text{set}}} \approx \frac{1}{R_{\text{set}}} \quad \text{for } R_{\text{set}} \gg \frac{1}{g_m}. \tag{1}$$

Note that such a method of controlling the transconductance can be more advantageous than the conventional method of modifying the bias current of the transistors operating in the OTA stage: due to the above negative feedback, the linearity of the OTA stage can be significantly improved. This is the main reason for choosing the CDeTA concept. When electronic control of the transconductance is required, it can be accomplished via the commonly used voltage-controlled resistance R_{set} based on simple CMOS circuitry.

A CMOS BD-CDTA, designed in the 0.25 μm CMOS SCN025 technology, is shown in Fig. 2. In comparison with the conventional gate-driving method, this topology works with a lower power supply voltage (±0.6 V), which also results in low power dissipation (143 μW for the complete topology in Fig. 2). Since the bulk-driving principle is applied to conventional MOS transistors, there is no need to use the expensive twin-tub technology [15, 19]. The transistor aspect ratios are summarized in Table 1.

In Fig. 2, the DC biasing of the topology is provided by transistors M1, M2, resistor R, and the corresponding transistors for current mirroring. The R value is designed such that the bias current flowing through the resistor is 4.59 μA. OTA No. 1 (2) in Fig. 1 is implemented via transistors M3–M9 and M19–M24 (M10–M18). The remaining transistors (M25–M39) form differential-output OTA No. 3 from Fig. 1 with the linearizing negative feedback led from the current output of the M30–M31 pair to the inverting voltage input of OTA No. 3 (bulk of M28). Each OTA is of

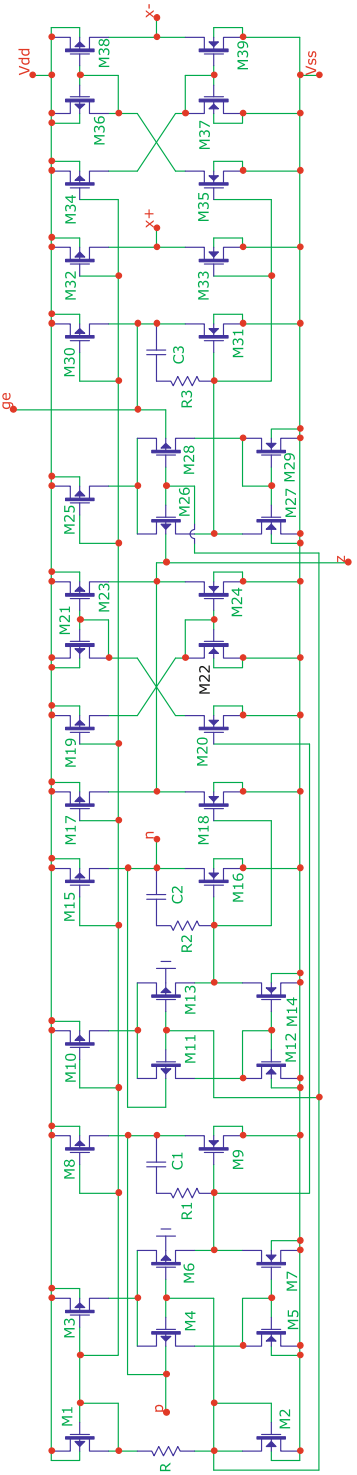

Fig. 2 Proposed BD-CDTA; $R_1 = R_2 = R_3 = 7.45\ \text{k}\Omega$, $C_1 = C_2 = C_3 = 0.5\ \text{pF}$

the classical two-stage topology, with the bulk-driven differential input stage employing a p-channel MOS transistor pair and a current mirror acting as an active load, and with current inverters and circuits for providing copies of the output current.

The negative feedback from the drain of M9 to the inverting voltage input of OTA No. 1 (bulk of M4) is accompanied by the R_1–C_1 circuit necessary for frequency compensation [23]. The same compensation is provided for OTA No. 2 (see the R_2–C_2 compensating circuit). The purpose of the compensation capacitor is to split the parasitic poles of two adjacent OTA stages in order to make the pole of the first stage dominant, whereas the pole of the second stage is pushed at a high frequency. The well-known problem of impaired phase margin due to the zero in the right s-plane is solved here by means of the zero-nulling technique when a resistor in series with the compensation capacitor cancels this zero, being equal to the inverse of the transconductance gain of the second stage [23]. The R and C values were preliminarily proposed according to a routine procedure described in [23]; they were then optimized via PSpice simulation in order to obtain a phase margin of 80 degrees.

For OTA1 and OTA2 in Fig. 1, large transconductances g_m are useful in order to provide small p- and n-input resistance $R_p = R_n = 1/g_m$ of the CDU. The aspect ratios of transistors, affecting the transconductances, i.e., M8, M9, M15, and M16, are designed such that they represent a compromise between the above requirement and the necessity of providing other important parameters such as low offset. The g_m value is approximately 4.41 mA/V; thus, the input resistance of terminals p and n is approximately 227 Ω. Such values are acceptable for most low-power applications of the CDTA with working currents in the microampere range, since such current flowing through the p- or n-terminals causes a negligible voltage drop in the millivolt range.

3 Small-Signal Low-Frequency Error Analysis of the CDTA

The small-signal accuracy of the proposed CDTA is influenced by the parasitic parameters of the OTA stages from which it is composed. The basic layout is given in Fig. 3.

Resistances R_{x1} to R_{x6} appear in the model due to the parasitic resistances of input and output terminals of OTA stages. All of them are of comparatively high values due to the high input and output impedances of the OTA. In most CDTA applications, it is advantageous when x-terminals work to low-impedance loads R_{x+} and R_{x-}. Then the influences of R_{x5} and R_{x6} are negligible. Below, we will derive the already-mentioned fact that the p- and n-terminal resistances are inversely proportional to the transconductances of OTAs No. 1 and 2. Since their values are much smaller than R_{x1} and R_{x2}, R_{x1} and R_{x2} can also be neglected. When designing R_{set} for adjusting the transconductance of the final OTA stage, the influence of R_{x3} should be taken into account. We can conclude that the most important parasitic resistance can be R_{x4},

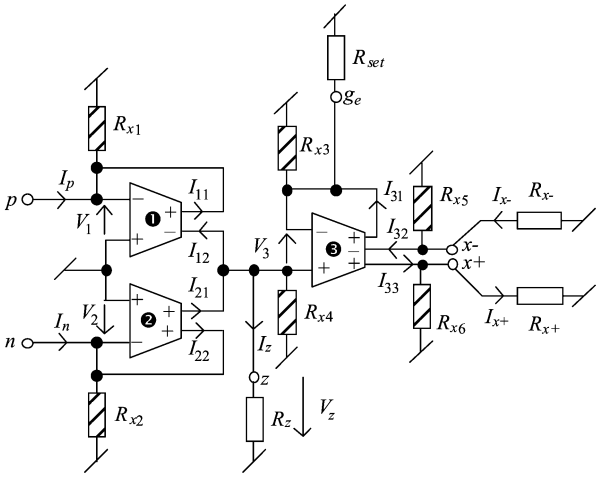

Fig. 3 CDTA model for small-signal low-frequency error analysis

particularly in applications where the capacitive load of the z-terminal is required and when its resistive part, R_z in Fig. 3, is not much higher than R_{x4}.

In addition to the parasitic resistances, the offset and g_m properties of the OTA stages in Fig. 3 can affect the precision of the CDTA significantly. Consider the linearized current versus voltage characteristics of OTA No. i, $i = 1, 2,$ or 3 in Fig. 3 as follows:

$$I_{ij} = g_{m,ij}(V_i + \Delta V_{ij}) = g_{m,ij} V_i + \Delta I_{ij}, \quad \Delta I_{ij} = g_{m,ij} \Delta V_{ij}, \ j = 1, 2, \text{or } 3 \quad (2)$$

where V_i and I_{ij} are voltages and currents defined in Fig. 3, ΔV_{ij} and ΔI_{ij} are the offset voltages and currents, and $g_{m,ij}$ is the transconductance of OTA No. i as a ratio of output current I_{ij} and input voltage V_i.

Then the currents I_p and I_n in Fig. 3 can be described as follows:

$$I_p = \left(g_{m,11} + \frac{1}{R_{x1}} \right)(-V_1) + \Delta I_{11}, \quad (3)$$

$$I_n = \left(g_{m,22} + \frac{1}{R_{x2}} \right)(-V_2) + \Delta I_{22}. \quad (4)$$

Equations (3) and (4) prove that the parasitic conductivities of the p- and n-terminals are given by the transconductances of OTAs No. 1 and 2, increased by parasitic conductances $1/R_{x1}$ and $1/R_{x2}$. In addition, the corresponding input characteristics (input current versus input voltage) show current offsets which are caused by the offset parameters of OTas No. 1 and 2.

Utilizing formula (2), the following equation for I_z can be derived from Fig. 3:

$$I_z = \alpha_p I_p - \alpha_n I_n + \Delta I_z, \quad (5)$$

where the current transfers α_p and α_n, and the current offset ΔI_z are given by the formulas

$$\alpha_p = \frac{1}{1+\frac{R_z}{R_{x3}}} \frac{g_{m,12}}{g_{m,11}+\frac{1}{R_{x1}}}, \tag{6}$$

$$\alpha_n = \frac{1}{1+\frac{R_z}{R_{x3}}} \frac{g_{m,22}}{g_{m,21}+\frac{1}{R_{x2}}}, \tag{7}$$

$$\Delta I_z = \frac{g_{m,12}(\Delta V_{11}-\Delta V_{12})+g_{m,22}(\Delta V_{21}-\Delta V_{22})}{1+\frac{R_z}{R_{x3}}}. \tag{8}$$

Equations (6) and (7) indicate that even if the parasitic resistances approached infinite values, the current transfers α_p and α_n can differ from their ideal unity values due to possible differences in the transconductances from OTA voltage input to individual current outputs. To eliminate this effect, the values of these transconductances should be as close as possible. The offset of current I_z is given by a linear combination of four offset voltages, multiplied by the corresponding transconductances. For fixed values of the offset voltages, the designer can decrease this offset only by decreasing the transconductances.

The currents of the final OTA stage of the CDTA in Fig. 3, namely I_{31}, I_{32}, and I_{33}, can be evaluated as follows:

$$I_{31} = \frac{g_{m,31}}{1+g_{m,31}R'_{\text{set}}} V_z + \frac{g_{m,31}}{1+g_{m,31}R'_{\text{set}}} \Delta V_{31}, \tag{9}$$

$$I_{32} = \frac{g_{m,32}}{g_{m,31}} I_{31} + g_{m,32}(\Delta V_{32}-\Delta V_{31}), \tag{10}$$

$$I_{33} = \frac{g_{m,33}}{g_{m,31}} I_{31} + g_{m,33}(\Delta V_{33}-\Delta V_{31}), \tag{11}$$

where

$$R'_{\text{set}} = \frac{R_{\text{set}}R_{x3}}{R_{\text{set}}+R_{x3}}. \tag{12}$$

If $R_{x-} \ll R_{x5}$ and $R_{x+} \ll R_{x6}$, then (10) and (11) can also be used for evaluating the output currents I_{x-} and I_{x+}. Otherwise, these currents are attenuated via current dividers.

It can be seen from (9) that the transconductance of the CDTA can be adjusted via an external resistor, as described in (1). The large value of its resistance provides a low current offset. Equations (10) and (11) reveal that these g_m and offset values can be further modified from the position of currents $I_{x-} \approx I_{32}$ and $I_{x+} \approx I_{33}$: The transconductance modifications are due to a mismatch of $g_{m,31}$, $g_{m,32}$, and $g_{m,33}$; the offset modifications are described by the last right-hand parts of (10) and (11).

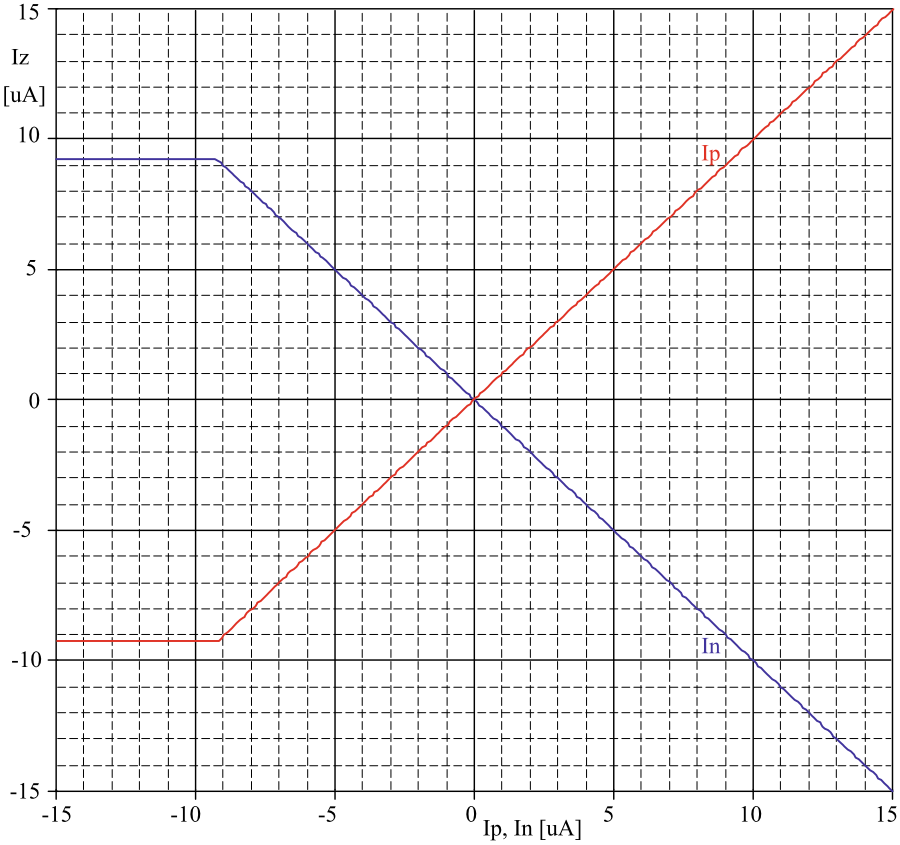

Fig. 4 DC curves I_z versus I_p or I_n, for $V_z = 0$

4 Simulation Results

The simulation results for the CDTA according to Fig. 2 are given in Figs. 4 through 9, and its small-signal parameters are summarized in Table 2.

Figure 4 shows the I_z/I_p and I_z/I_n curves of the current differencing unit (CDU), simulated on the assumption of $V_z = 0$. Note that for negative input currents I_p and I_n, the boundary of linear operation is ca. -9 μA. The current offset ΔI_z is ca. -149 nA. For the bias point $I_p = I_n = 0$, the corresponding small-signal current gains are as follows: $\alpha_p = I_z/I_p = 0.985$, $\alpha_n = I_z/I_n = 1$. The frequency responses of these gains are given in Fig. 5. The cutoff frequencies for the gains α_p and α_n are 17 MHz and 36 MHz, respectively.

The voltage-current characteristic of the p-terminal input gate of the CDTA is shown in Fig. 6. Identical results also hold for the n-terminal. Note that when the input current approaches a value of ca. -9 μA, the clipping property of this curve can cause a significant nonlinear distortion. However, the range of linear operation is suitable for many applications that need extra-low power consumption. For the

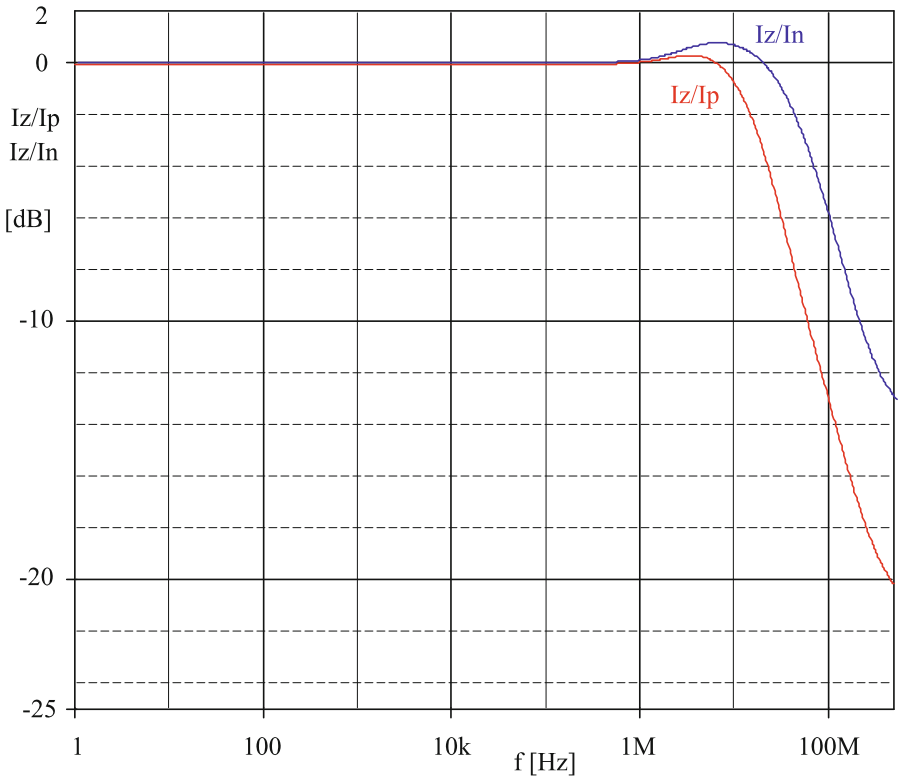

Fig. 5 Frequency responses of current gains I_z/I_p and I_z/I_n for $V_z = 0$

DC bias $I_p = 0$, the small-signal resistances R_p and R_n are 226.6 Ω. The frequency dependence of the impedances of the p- and n-terminals in Fig. 7 shows that the above values are kept up to ca. 100 kHz. Then the impedances increase due to the frequency dependence of the OTA transconductances.

The I_x versus V_z curves in Fig. 8 are analyzed for several values of the external resistance R_{set}. They clearly show the transconductance control via R_{set} as well as the effect of the linearization and increase of the dynamic range with increasing values of R_{set}. A detailed analysis also confirms the conclusion from Sect. 3 that the current offset is decreasing with increasing values of R_{set}. For $R_{\text{set}} = 10$ kΩ, the offset current is only −154 nA. Figure 9 shows the frequency dependences of $g_{m,\text{set}}$ and of the x- and z-terminal impedances. The transconductance bandwidth increases with increasing R_{set}. For example, $R_{\text{set}} = 10$ kΩ yields $g_{m,\text{set}} \approx 99$ μA/V and the −3 dB cutoff frequency is approximately 1.1 MHz. The frequency dependence of the z-terminal impedance shows the value 262 kΩ, with a −3 dB cutoff frequency of about 2 MHz. The low-frequency x-terminal resistance is ca. 1.2 MΩ. The small-signal parameters of the CDTA are summarized in Table 2.

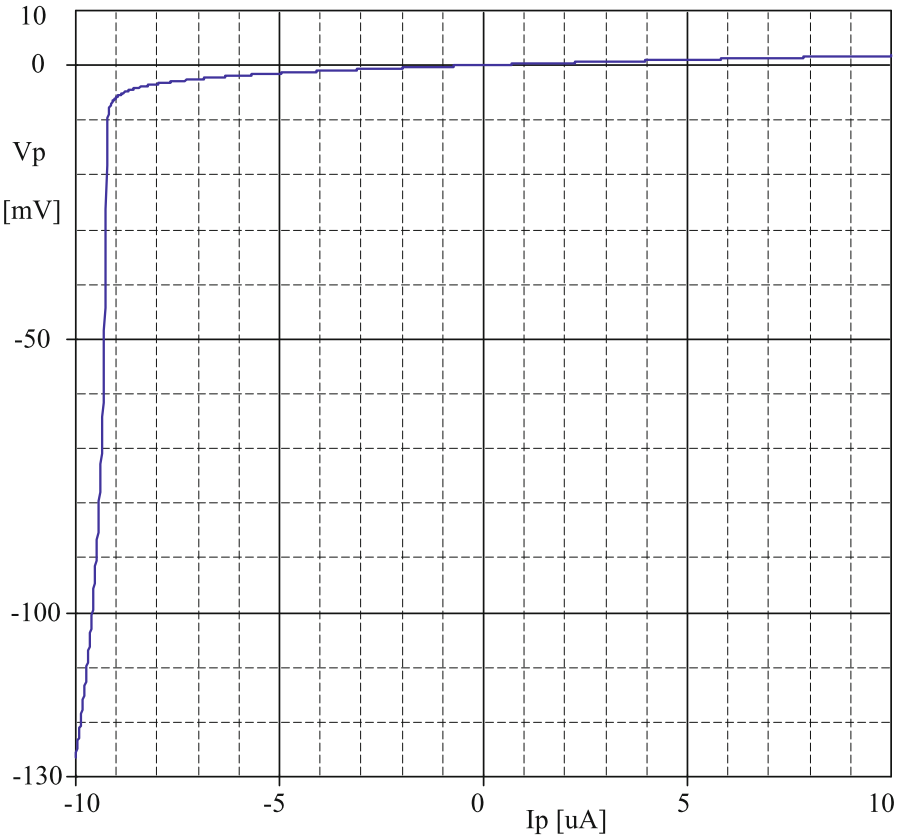

Fig. 6 DC curve V_p versus I_p for evaluating small-signal input resistance of the p-terminal. For the n-terminal, the result is identical

5 Application Example of Bulk-Driven CDTA

To demonstrate the functionality of the proposed bulk-driven CDTA, the low-voltage low-power transadmittance filter [2] in Fig. 10, transforming the input current I_{in} into output voltage V_{out}, was designed and simulated. Since R_1 and R_2 are virtually grounded via the low-impedance p and n inputs of the CDTA, the filter behaves as a conventional ladder filter on the assumption that the CDTA together with C_L and R_{set} simulates the floating inductor, connected in parallel to C_2. The latter statement follows from the fact that I_x currents are proportional to the z-terminal voltage, and that this voltage is caused by the difference current $I_p - I_n$, which flows through C_L:

$$I_x = g_{m,\text{set}} V_z = g_{m,\text{set}} \frac{I_p - I_n}{sC_L} = g_{m,\text{set}} \frac{V_{x-}/R_1 - V_{x+}/R_2}{sC_L}. \tag{13}$$

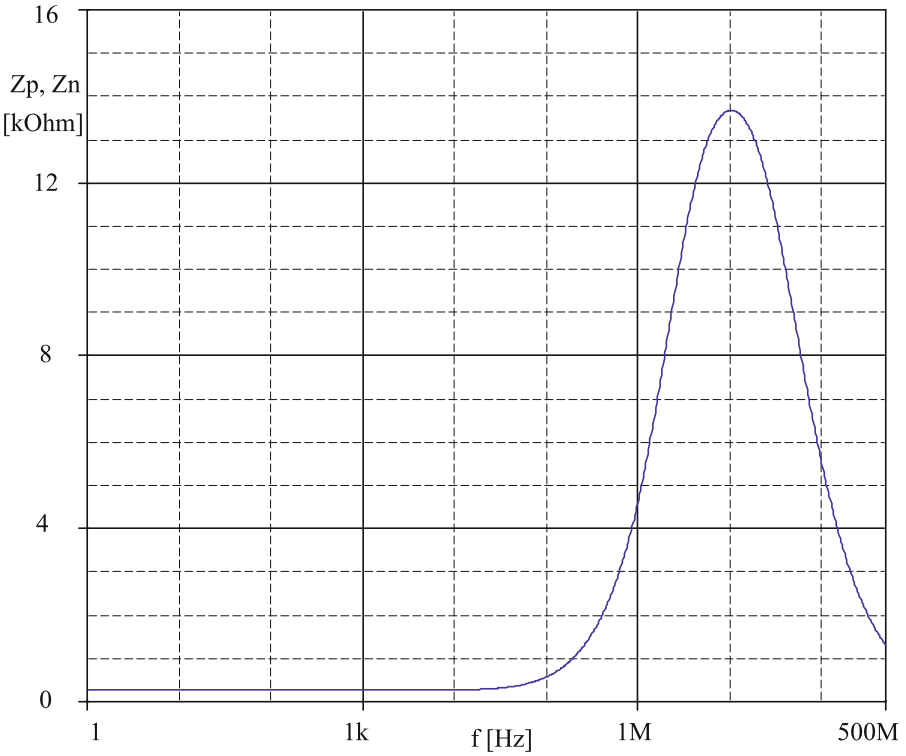

Fig. 7 Frequency dependence of the impedances of p- and n-terminals

Table 2 Parameters of designed BD-CDTA

	BD-CDTA
Supply voltage	±0.6 V
Power consumption	143 μW
3 dB bandwidth of I_z/I_p, I_z/I_n	17 MHz, 36 MHz
DC current swing of I_p, I_n	±9 μA
DC voltage swing of V_z ($R_{\text{set}} = 10\ \text{k}\Omega$)	±100 mV
DC offset of OTA stage ($R_{\text{set}} = 10\ \text{k}\Omega$)	−154 nA
Current gains I_z/I_p, I_z/I_n	0.985, 1
$g_{m,\text{set}}$ ($R_{\text{set}} = 10\ \text{k}\Omega$)	99 μA/V
3 dB bandwidth of $g_{m,\text{set}}$ ($R_{\text{set}} = 10\ \text{k}\Omega$)	1.1 MHz
Node n and p resistances	227 Ω
Node z resistance	262 kΩ
Node x resistances	1.2 MΩ

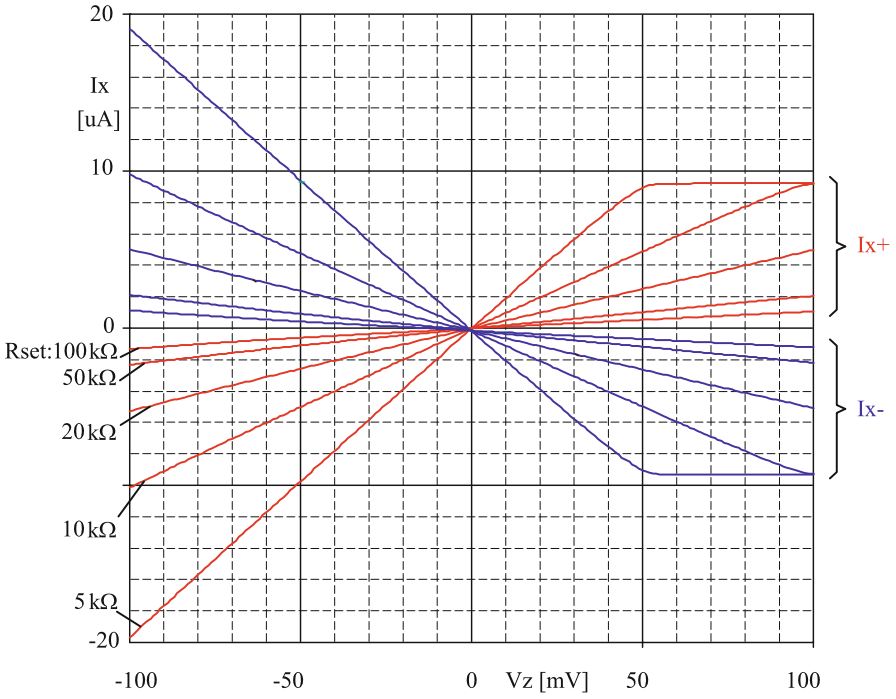

Fig. 8 DC characteristics of OTA No. 3 with R_{set} linearization and transconductance control

For symmetrical termination of the filter, i.e., if

$$R_1 = R_2 = R, \tag{14}$$

(13) can be simplified to the form

$$I_x = \frac{V_{x-} - V_{x+}}{sL}, \tag{15}$$

where

$$L = \frac{C_L R}{g_{m,\text{set}}}. \tag{16}$$

In other words, the CDTA simulates a floating inductor with the inductance defined by (16). The component values in Fig. 10 were designed for the low-pass ladder filter according to Cauer approximation, with a -3 dB cutoff frequency of 50 kHz, a pass-band ripple of 2 dB, and an attenuation of 40 dB for frequencies above 110 kHz.

The frequency response in Fig. 11 simulated in PSpice is in good agreement with the response of the ideal passive RCL ladder filter. The low-frequency trans-simpedance is $R/2 = 5\ \text{k}\Omega$.

In order to verify the transient behavior of the proposed filter, a steady-state transient analysis was performed under filter excitation by a sinusoidal current source

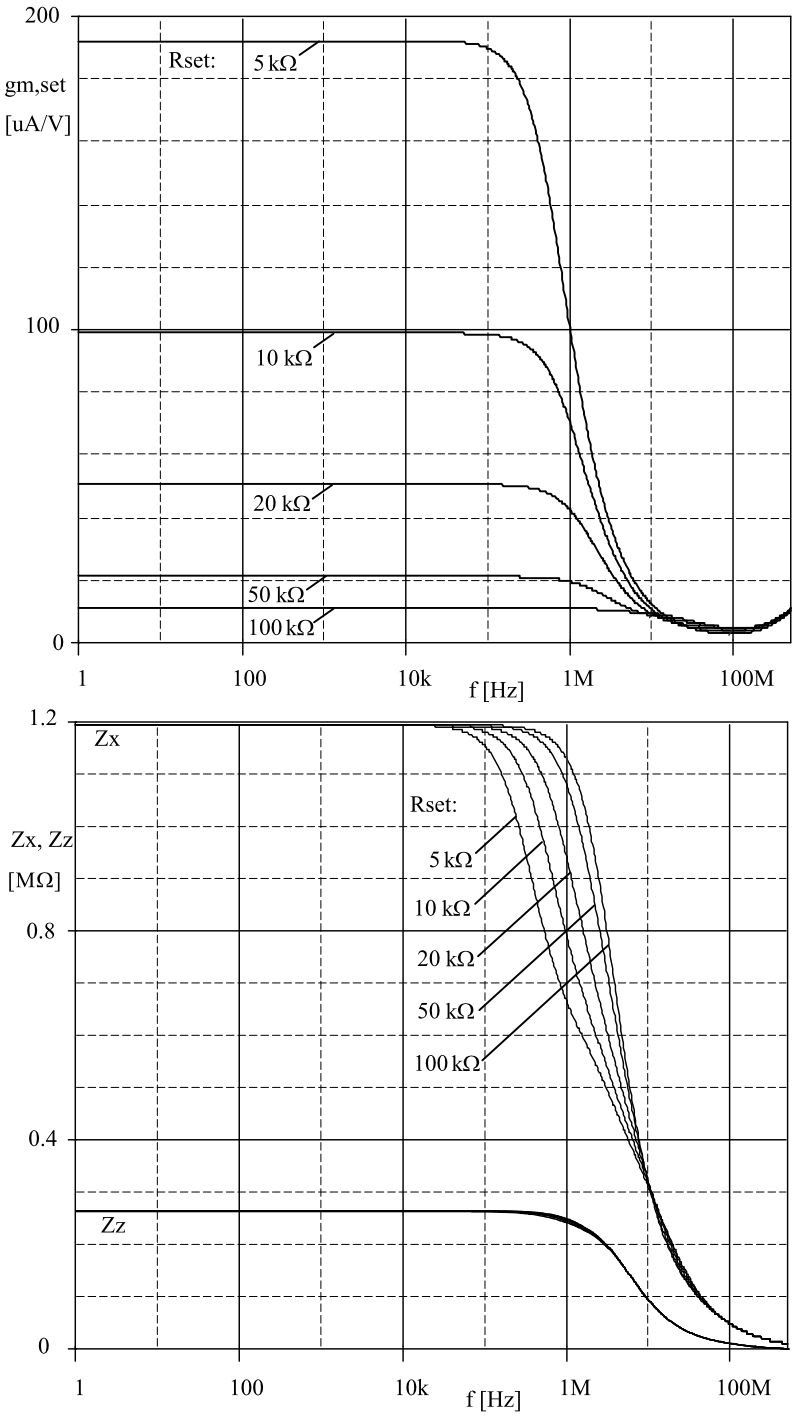

Fig. 9 Frequency responses of transconductances, *x*- and *z*-terminal impedances

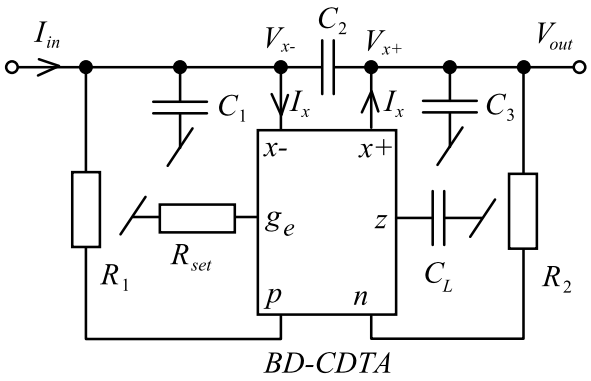

Fig. 10 Low-voltage low-power third-order transadmittance elliptic 50 kHz low-pass filter, $R_1 = R_2 = R_{\text{set}} = 10$ kΩ, $C_1 = C_3 = 804$ pF, $C_2 = 72.6$ pF, $C_L = 234$ pF

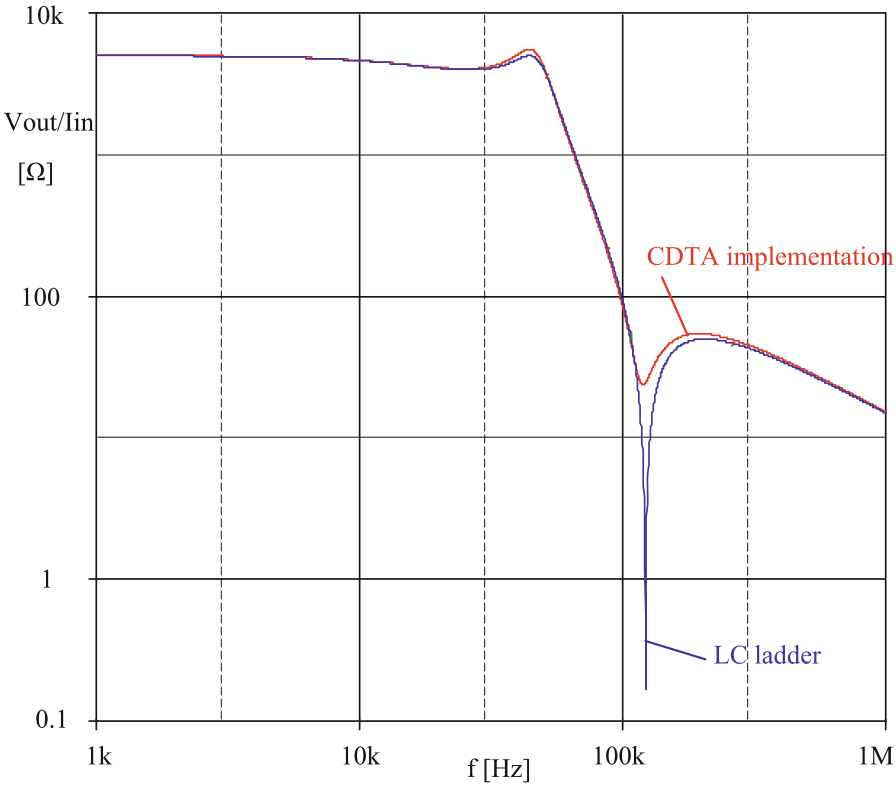

Fig. 11 Simulated frequency response of the filter from Fig. 10 and its comparison with the characteristic of an ideal ladder filter

with an amplitude of 15 μA and a frequency of 10 kHz. The total harmonic distortion (THD) of the output waveform in Fig. 12 labeled "CDTA implementation" is 0.36%. The Fourier analysis also reveals a DC offset voltage of about −1.78 mV.

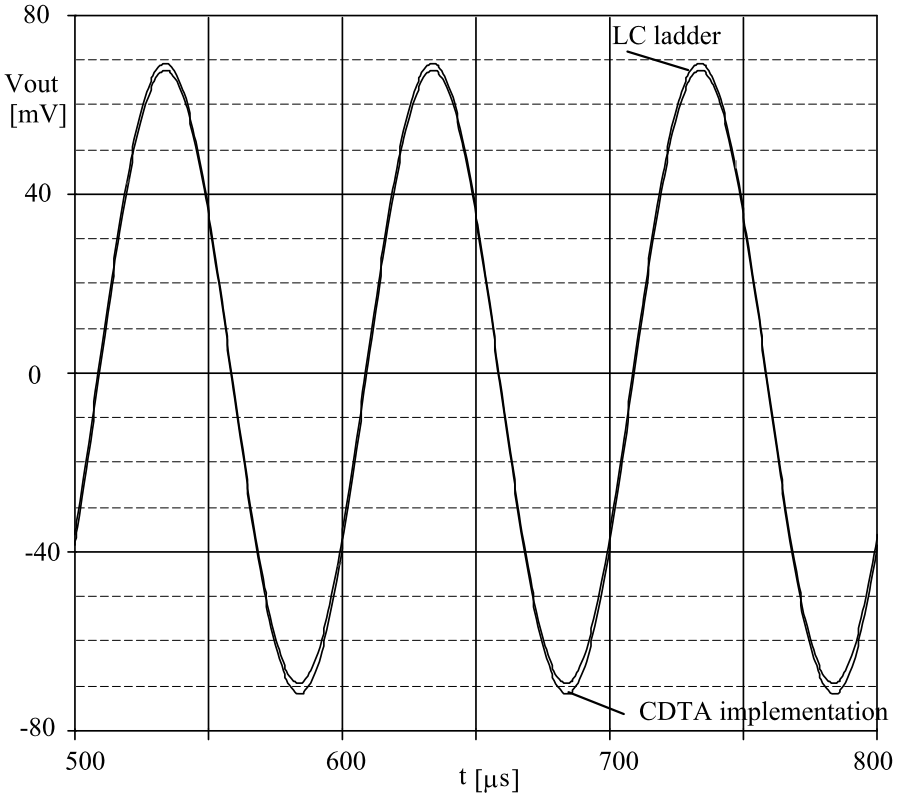

Fig. 12 Steady-state transient analysis with 15 µA/10 kHz sinusoidal input current

The DC V_{out} versus I_{in} characteristic in Fig. 13 clearly shows the limits of linear operation of the filter, which can be approximately described as follows: abs(I_{in}) < 18 µA, abs(V_{out}) < 95 mV. The above-mentioned DC offset is also evident.

Note that the total power dissipation of the filter is 144 µW.

6 Conclusion

This paper demonstrates a way of applying the principle of a bulk-driven MOS transistor to the design of a low-voltage low-power current differencing transconductance amplifier. The main advantages of bulk-driven devices are extra-low supply voltages and power consumption. These features are achieved at the cost of lower bandwidth. That is why the proposed CDTA can be useful in applications in devices for frequency ranges of up to hundreds of kilohertz, where an extra-low power consumption is required. PSpice simulations of the bulk-driven CDTA designed in the 0.25 µm CMOS technology confirm the theoretical analyses.

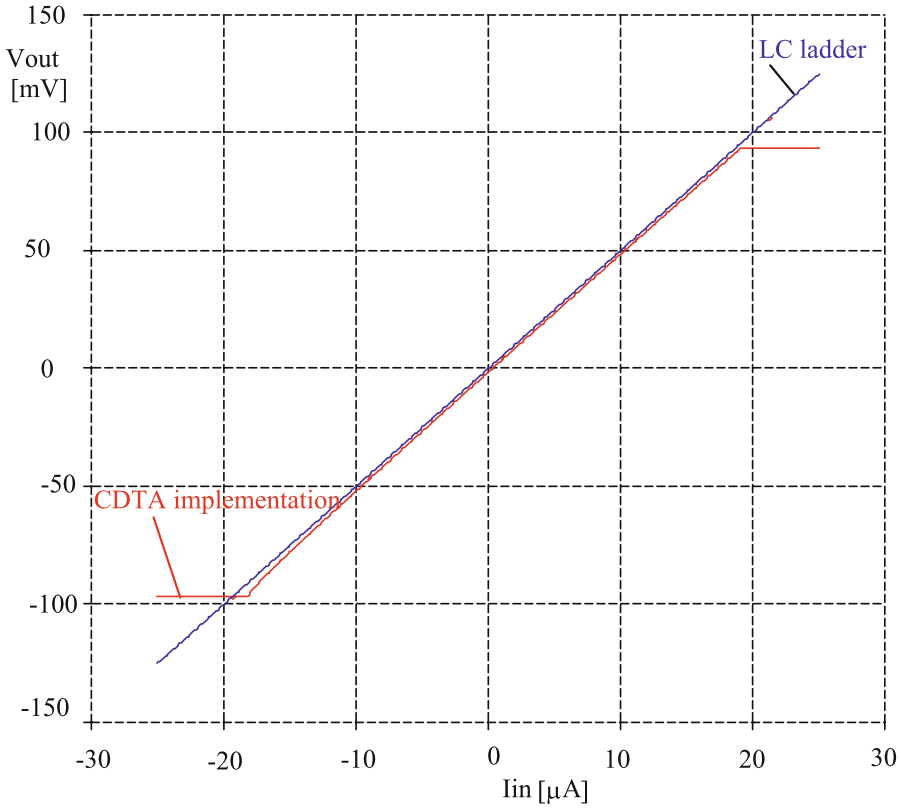

Fig. 13 DC analysis with input current swept from −25 μA to +25 μA

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