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Novel Cascadable All-Pass/Notch Filters Using a Single FDCCII and Grounded Capacitors

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Abstract Four new second-order voltage-mode cascadable all-pass/notch filters are proposed using only a single active element and four passive components. The active element used is a fully differential current conveyor. All the circuits possess high-input and low-output impedance, which is a desirable feature for voltage-mode circuits. A non-ideal and parasitic study is also performed. The proposed circuits are verified through PSPICE simulation results.

Keywords Current conveyor · Active filters · All-pass · Notch

1 Introduction

A voltage-mode circuit with high-input and low-output impedance is of special interest, as no additional buffers are needed for cascading such circuits. Such a circuit can be conveniently used between various voltage-mode blocks without additional hardware. All-pass filters are an important class of analogue signal processing functions with application in communication and instrumentation systems [5, 13, 14]. On

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the other hand, notch filters are used to eliminate a single frequency called the notch frequency.

Numerous all-pass and notch filter realization using different types of active elements such as current conveyors and its different variations are available in the literature [3, 4, 6–11, 15–30]. Some of the available voltage-mode (VM) all-pass/notch filters do enjoy the isolated feature(s) of grounded capacitors, high-input impedance and/or low-output impedance. But a careful survey reveals that none of the reported works realizes a second-order all-pass/notch filter functions using optimum number of active and passive components, grounded capacitors, and providing high-input impedance and low-output impedance feature simultaneously. Though, very recently, first-order all-pass filters based on single FDCCII and grounded passive components have been reported [24, 26].

This paper proposes four new second-order voltage-mode cascadable all-pass/notch filters using one active element, two resistors and two grounded capacitors, which are ideal for IC implementation. Each circuit possesses high-input and low-output impedance. The proposed circuits are based on fully differential second-generation current conveyor (FDCCII), an active element useful for improving the dynamic range in mixed-mode application, where a fully differential signal processing is required [12]. PSPICE simulation results using TSMC 0.35 μm CMOS parameters are given to validate the circuits.

2 Circuit Descriptions

The fully differential second-generation current conveyor (FDCCII) is an eight terminal analog building block with the defining matrix equation of the form

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_{Y4} \\ V_{X+} \\ V_{X-} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 1 & 0 & 0 & 0 & 0 & 0 \\ -1 & 1 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_{Y4} \\ I_{X+} \\ I_{X-} \\ V_{Z+} \\ V_{Z-} \end{bmatrix}. \tag{1}$$

The symbol and CMOS implementation of FDCCII are shown in Fig. 1 [12]. FDCCII is a useful and versatile active element for analog signal processing [6–10, 19, 23, 24, 26].

The four proposed second-order voltage-mode cascadable all-pass/notch filters using a single FDCCII, two resistors and two grounded capacitors are shown in Fig. 2(a)–(d). The four circuits are characterized by following identical voltage transfer function:

$$\frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = k\frac{s^2R_1R_2C_1C_2 + s(R_1C_1 + R_2C_2 - 2R_2C_1) + 1}{s^2R_1R_2C_1C_2 + s(R_1C_1 + R_2C_2 - R_2C_1) + 1}, \tag{2}$$

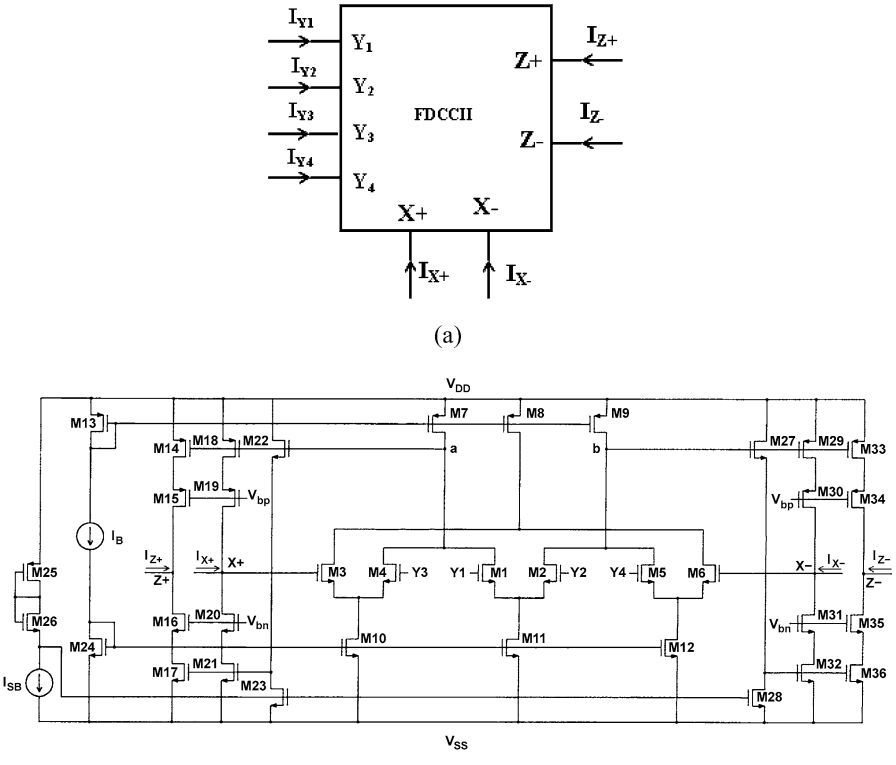

Fig. 1 Fully differential second-generation current conveyor; (**a**) symbol; (**b**) CMOS implementation [12]

where $k = +1$ for circuit-I and circuit-II (Fig. 2(a) and (b)), and $k = -1$ for circuit-III and circuit-IV (Fig. 2(c) and (d)).

From (2), the pole frequency (ω_o) and the quality factor (Q) are given by

$$\omega_o = \left(\frac{1}{C_1 C_2 R_1 R_2}\right)^{\frac{1}{2}}, \tag{3}$$

$$Q = \frac{\sqrt{R_1 R_2 C_1 C_2}}{R_1 C_1 + R_2 C_2 - R_2 C_1}. \tag{4}$$

2.1 All-Pass Section

For realizing the second-order all-pass filter there are two possible designs:

Design 1

$$R_2 = 2R_1 = 2R, \qquad C_1 = C_2 = C.$$

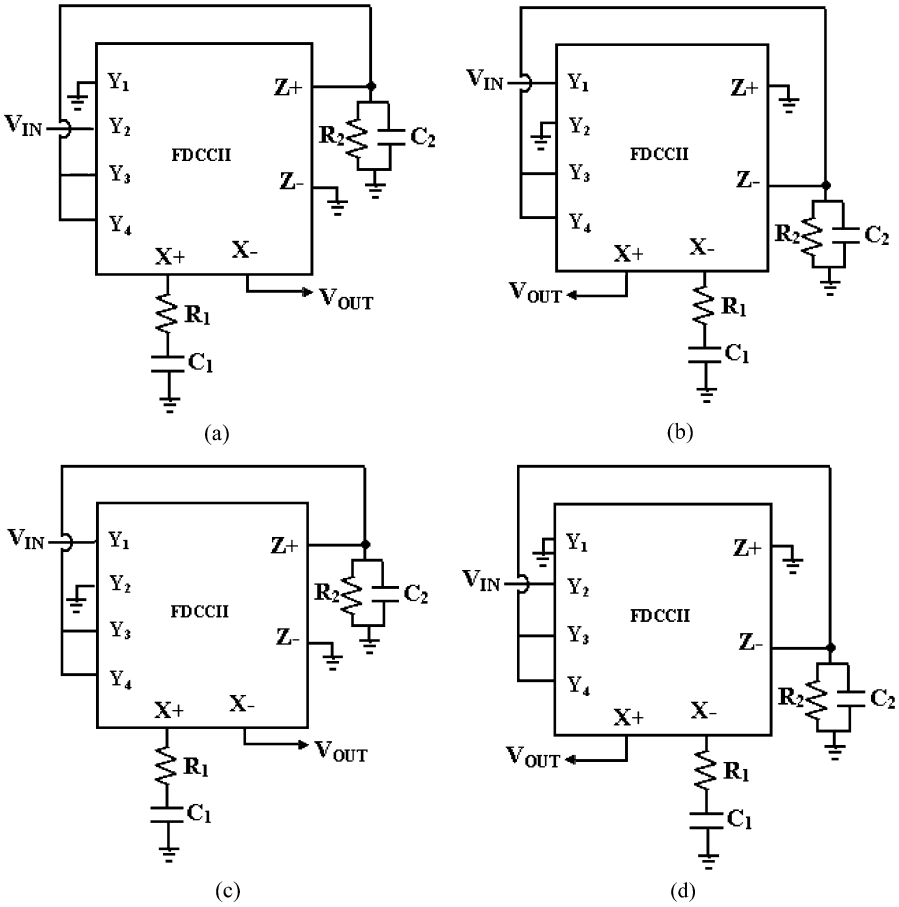

Fig. 2 Proposed second-order cascadable all-pass/notch filters: (**a**) circuit-I; (**b**) circuit-II; (**c**) circuit-III; and (**d**) circuit-IV

With the above condition, (2) becomes

$$\frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = k\frac{s^2 2R^2C^2 - sRC + 1}{s^2 2R^2C^2 + sRC + 1}, \tag{5}$$

where the value of $k = +1$ for circuit-I and circuit-II, representing non-inverting all-pass filter and $k = -1$ for circuit-III and circuit-IV, representing inverting all-pass filter.

Design 2

$$R_2 = R_1 = R, \qquad C_1 = 2C_2 = 2C.$$

With the above condition, (2) becomes

$$\frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = k\frac{s^2 2R^2C^2 - sRC + 1}{s^2 2R^2C^2 + sRC + 1}, \tag{6}$$

where the value of $k = +1$ for circuit-I and circuit-II, representing non-inverting all-pass filter and $k = -1$ for circuit-III and circuit-IV, representing inverting all-pass filter.

2.2 Notch Filter

For realizing the second-order notch filter the following condition must be satisfied:

$$R_2 = R_1 = R, \qquad C_1 = C_2 = C.$$

Equation (2) becomes

$$\frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = k\frac{s^2R^2C^2 + 1}{s^2R^2C^2 + sRC + 1}, \tag{7}$$

where the value of $k = +1$ for circuit-I and circuit-II, representing non-inverting notch filter and $k = -1$ for circuit-III and circuit-IV, representing inverting notch filter.

From (5)–(6), the pole frequency (ω_o) and the quality factor (Q) for second-order all-pass filter are given by

$$\omega_o = \frac{1}{CR\sqrt{2}}, \tag{8}$$

$$Q = \sqrt{2} = 1.414. \tag{9}$$

Similarly, from (7), the pole frequency (ω_o) and the quality factor (Q) for second-order notch filter are given by

$$\omega_o = \frac{1}{CR}, \tag{10}$$

$$Q = 1. \tag{11}$$

The salient features of the proposed circuits are high-input and low-output impedance, single active element and use of grounded capacitors, which are ideal for IC implementation. Since the proposed filter circuits realize only relatively low Q values, namely a maximum of 1.414 for all-pass and 1 for notch, the new circuits are not suited for synthesis of higher-order filters. Moreover, it may also be noted that the realized Q value are fixed, a feature because of filter realizability conditions. This makes the circuits good for fixed Q applications. It is thus to be concluded that the new proposed circuits provide useful active RC second-order all-pass filtering options with minimum components.

3 Parasitic and Non-ideal Analysis

3.1 Parasitic Effects

A study is next carried out on the effects of various parasitic of the FDCCII used in the proposed circuits. These are port Z parasitic in form of $R_Z//C_Z$, port Y parasitic in form of $R_Y//C_Y$ and port X parasitic in form of series resistance R_X [23]. The proposed circuits are reanalyzed taking into account the above parasitic effects. The voltage transfer function (assuming $R_2 \ll R_Y$ or R_Z and $R_X \ll R_1$), for the circuits of Fig. 2(a)–(d), is given as

$$\frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = k\frac{s^2R'R_2C_1(C_2+C_p)+s(R'C_1+R_2(C_2+C_p)-2R_2C_1)+1}{s^2R'R_2C_1(C_2+C_p)+s(R'C_1+R_2(C_2+C_p)-R_2C_1)+1}, \tag{12}$$

where, $R' = R_1 + R_{X+}$, $C_P = C_{Z+} + C_{Y3} + C_{Y4}$ (for Figs. 2(a) and (c)) and $R' = R_1 + R_{X-}$, $C_P = C_{Z-} + C_{Y3} + C_{Y4}$ (for Fig. 2(b) and (d)).

From (12), it is seen that the pole frequency (ω_o) and the quality factor (Q) is

$$\omega_o = \left(\frac{1}{R'R_2C_1(C_2+C_p)}\right)^{\frac{1}{2}}, \tag{13}$$

$$Q = \frac{\sqrt{R'R_2C_1(C_2+C_p)}}{R'C_1+R_2(C_2+C_p)-R_2C_1}. \tag{14}$$

From (12), the parasitic resistance/capacitances merge with the external value. Such a merger does cause a slight deviation in circuit's parameters, which can be eliminated by pre-distorting the element values to be used in the circuit. It is seen that the pole frequency and the quality factor would be slightly deviated (in deficit) due to these parasitics. The deviation is expected to be small for an integrated FDCCII, the actual value would be given in the 'simulation results'.

3.2 Non-ideal Analysis

To account for non-ideal sources, two parameter α and β are introduced where α_i $(i = 1, 2)$ accounts for current transfer gains and β_i $(i = 1, 2, 3, 4, 5, 6)$ accounts for voltage transfer gains of the FDCCII. These transfer gains differ from unity by the voltage and current tracking errors of the FDCCII. More specifically, $\alpha_i = 1 - \delta_i$, $(|\delta_i| \ll 1)$ where current tracking errors are δ_1 (from $X+$ to $Z+$) and δ_2 (from $X-$ to $Z-$). Similarly, $\beta_i = 1 - \varepsilon_i$ $(|\varepsilon_i| \ll 1)$, where voltage tracking errors are ε_1 (from Y_1 to $X+$), ε_2 (from Y_2 to $X+$), ε_3 (from Y_3 to $X+$), ε_4 (from Y_1 to $X-$), ε_5 (from Y_2 to $X-$), and ε_6 (from Y_4 to $X-$), respectively. Incorporating the two sources of error onto ideal input-output matrix relationship of the modified FDCCII leads to

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_{Y4} \\ V_{X+} \\ V_{X-} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \beta_1 & -\beta_2 & \beta_3 & 0 & 0 & 0 & 0 & 0 \\ -\beta_4 & \beta_5 & 0 & \beta_6 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \alpha_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \alpha_2 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_{Y4} \\ I_{X+} \\ I_{X-} \\ V_{Z+} \\ V_{Z-} \end{bmatrix}. \tag{15}$$

The circuits of Fig. 2 are reanalyzed using (15) and the non-ideal voltage transfer functions are found as

Circuit-I:

$$\frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = \beta_5 \frac{s^2 R_1 R_2 C_1 C_2 + s(R_1 C_1 + R_2 C_2 - \alpha_1(\beta_3 + (\beta_2\beta_6/\beta_5))R_2 C_1) + 1}{s^2 R_1 R_2 C_1 C_2 + s(R_1 C_1 + R_2 C_2 - \alpha_1\beta_3 R_2 C_1) + 1} \tag{16}$$

Circuit-II:

$$\frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = \beta_1 \frac{s^2 R_1 R_2 C_1 C_2 + s(R_1 C_1 + R_2 C_2 - \alpha_2(\beta_6 + (\beta_4\beta_3/\beta_1))R_2 C_1) + 1}{s^2 R_1 R_2 C_1 C_2 + s(R_1 C_1 + R_2 C_2 - \alpha_2\beta_6 R_2 C_1) + 1} \tag{17}$$

Circuit-III:

$$\frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = -\beta_4 \frac{s^2 R_1 R_2 C_1 C_2 + s(R_1 C_1 + R_2 C_2 - \alpha_1(\beta_3 + (\beta_1\beta_6/\beta_4))R_2 C_1) + 1}{s^2 R_1 R_2 C_1 C_2 + s(R_1 C_1 + R_2 C_2 - \alpha_1\beta_3 R_2 C_1) + 1} \tag{18}$$

Circuit-IV:

$$\frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = -\beta_2 \frac{s^2 R_1 R_2 C_1 C_2 + s(R_1 C_1 + R_2 C_2 - \alpha_2(\beta_6 + (\beta_5\beta_3/\beta_2))R_2 C_1) + 1}{s^2 R_1 R_2 C_1 C_2 + s(R_1 C_1 + R_2 C_2 - \alpha_2\beta_6 R_2 C_1) + 1}. \tag{19}$$

The sensitivities of pole frequency (ω_o), gain (H) and quality factor (Q) to active and passive components are analyzed for the circuits of Fig. 2(a)–(d) described by (16)–(19) and given in Tables 1 and 2. It is evident that the sensitivity of pole frequency (ω_o), gain (H) and quality factor (Q) to active and passive components is less than or equal to unity in magnitude for $R_1C_1 \leq R_2C_2$. Thus, the four new circuits of Fig. 2 enjoy attractive active and passive sensitivity performance.

Table 1 Sensitivity figure for the proposed circuits of Fig. 2 (a)–(d) with respect to pole frequency (ω_o) and gain (H)

Circuit	$S^{\omega_o}_{\alpha_1,\alpha_2,\beta_1,\beta_2,\beta_3,\beta_4,\beta_5,\beta_6}$	$S^{\omega_o}_{R_1,R_2,C_1,C_2}$	$S^{H}_{\beta_1}$	$S^{H}_{\beta_5}$	$S^{H}_{\beta_4}$	$S^{H}_{\beta_2}$	$S^{H}_{\alpha_1,\alpha_2,\beta_3,\beta_6,R_1,R_2,C_1,C_2}$
Circuit-I	0	−1	0	1	0	0	0
Circuit-II	0	−1	1	0	0	0	0
Circuit-III	0	−1	0	0	1	0	0
Circuit-IV	0	−1	0	0	0	1	0

Table 2 Sensitivity figure for the proposed circuits of Fig. 2 (a)–(d) with respect to quality factor (Q)

Circuit	$S^{Q}_{\beta_1,\beta_2,\beta_4,\beta_5}$	$S^{Q}_{R_1,C_2}$	$S^{Q}_{R_2,C_1}$	$S^{Q}_{\alpha_1,\beta_3}$	$S^{Q}_{\alpha_2,\beta_6}$
Circuit-I	0	$-\frac{(R_1C_1-R_2C_2+\alpha_1\beta_3R_2C_1)}{2(R_1C_1+R_2C_2-\alpha_1\beta_3R_2C_1)}$	$\frac{(R_1C_1-R_2C_2+\alpha_1\beta_3R_2C_1)}{2(R_1C_1+R_2C_2-\alpha_1\beta_3R_2C_1)}$	$\frac{\alpha_1\beta_3R_2C_1}{(R_1C_1+R_2C_2-\alpha_1\beta_3R_2C_1)}$	0
Circuit-II	0	$-\frac{(R_1C_1-R_2C_2+\alpha_2\beta_6R_2C_1)}{2(R_1C_1+R_2C_2-\alpha_2\beta_6R_2C_1)}$	$\frac{(R_1C_1-R_2C_2+\alpha_2\beta_6R_2C_1)}{2(R_1C_1+R_2C_2-\alpha_2\beta_6R_2C_1)}$	0	$\frac{\alpha_2\beta_6R_2C_1}{(R_1C_1+R_2C_2-\alpha_2\beta_6R_2C_1)}$
Circuit-III	0	$\frac{(R_1C_1-R_2C_2+\alpha_1\beta_3R_2C_1)}{2(R_1C_1+R_2C_2-\alpha_1\beta_3R_2C_1)}$	$-\frac{(R_1C_1-R_2C_2+\alpha_1\beta_3R_2C_1)}{2(R_1C_1+R_2C_2-\alpha_1\beta_3R_2C_1)}$	$-\frac{\alpha_1\beta_3R_2C_1}{(R_1C_1+R_2C_2-\alpha_1\beta_3R_2C_1)}$	0
Circuit-IV	0	$\frac{(R_1C_1-R_2C_2+\alpha_2\beta_6R_2C_1)}{2(R_1C_1+R_2C_2-\alpha_2\beta_6R_2C_1)}$	$-\frac{(R_1C_1-R_2C_2+\alpha_2\beta_6R_2C_1)}{2(R_1C_1+R_2C_2-\alpha_2\beta_6R_2C_1)}$	0	$-\frac{\alpha_2\beta_6R_2C_1}{(R_1C_1+R_2C_2-\alpha_2\beta_6R_2C_1)}$

Table 3 0.35 μm level 3 MOSFET parameters

NMOS:
LEVEL = 3 TOX = 7.9E-9 NSUB = 1E17 GAMMA = 0.5827871 PHI = 0.7 VTO = 0.5445549 DELTA = 0 UO = 436.256147 ETA = 0 THETA = 0.1749684 KP = 2.055786E-4 VMAX = 8.309444E4 KAPPA = 0.2574081 RSH = 0.0559398 NFS = 1E12 TPG = 1 XJ = 3E-7 LD = 3.162278E-11 WD = 7.04672E-8 CGDO = 2.82E-10 CGSO = 2.82E-10 CGBO = 1E-10 CJ = 1E-3 PB = 0.9758533 MJ = 0.3448504 CJSW = 3.777852E-10 MJSW = 0.3508721
PMOS:
LEVEL = 3 TOX = 7.9E-9 NSUB = 1E17 GAMMA = 0.4083894 PHI = 0.7 VTO = −0.7140674 DELTA = 0 UO = 212.2319801 ETA = 9.999762E-4 THETA = 0.2020774 KP = 6.733755E-5 VMAX = 1.181551E5 KAPPA = 1.5 RSH = 30.0712458 NFS = 1E12 TPG = −1 XJ = 2E-7 LD = 5.000001E-13 WD = 1.249872E-7 CGDO = 3.09E-10 CGSO = 3.09E-10 CGBO = 1E-10 CJ = 1.419508E-3 PB = 0.8152753 MJ = 0.5 CJSW = 4.813504E-10 MJSW = 0.5

Table 4 Transistor aspect ratios for the circuit shown in Fig. 1

Transistors	W (μm)	L (μm)
M1–M6	60	4.8
M7–M9, M13	480	4.8
M10–M12, M24	120	4.8
M14, M15, M18, M19, M25, M29, M30, M33, M34	240	2.4
M16, M17, M20, M21, M26, M31, M32, M35, M36	60	2.4
M22, M23, M27, M28	4.8	4.8

4 Simulation Results

The proposed circuits were verified using PSPICE simulation. The FDCCII was realized using CMOS implementation as shown in Fig. 1 [12] and simulated using TSMC 0.35 μm, Level 3 MOSFET parameters as listed in Table 3. The aspect ratio of the MOS transistors are listed in Table 4, with the following DC biasing levels: $V_{dd} = -V_{ss} = 1.3V$, $V_{bp} = V_{bn} = 0V$, $I_B = 1.6$ μA and $I_{SB} = 1.4$ μA. The proposed circuit-I and circuit-III shown in Fig. 2(a) and (c), was designed with the passive element values $C_1 = C_2 = 1.5$ nF, $R_1 = 5$ kΩ and $R_2 = 10$ kΩ to obtain second-order all-pass filter. The theoretical designed pole frequency from (3) substituting the above component value is found to be 15.01 kHz. The phase and gain plots for circuit-I are shown in Fig. 3. The phase is found to vary with frequency 0° to −360° with a value of −180°at the pole frequency, and the simulated pole frequency was found to be 14.927 kHz, which is close to the theoretical value. Similarly, the phase and gain plots for circuit-III are shown in Fig. 4. The phase is found to vary with frequency 180° to −180° with a value of 0° at the pole frequency, and the simulated pole frequency was found to be 14.874 kHz, which is close to the theoretical value.

Next, the circuits of Fig. 2(a) and (c) has been designed as notch filter by taking the values of passive elements $C_1 = C_2 = 10$ nF, and $R_1 = R_2 = 1$ kΩ to obtain a theoretical pole frequency of 15.92 kHz. Figure 5 shows the phase and gain response

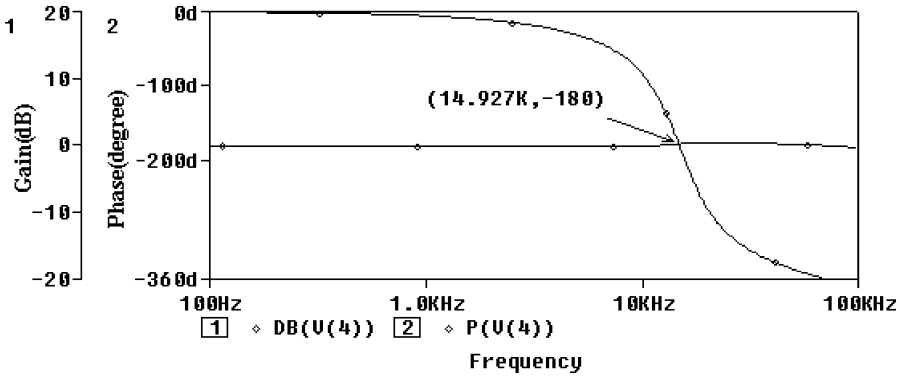

Fig. 3 Gain and phase responses of the all-pass filter obtained for circuit-I of Fig. 2(a)

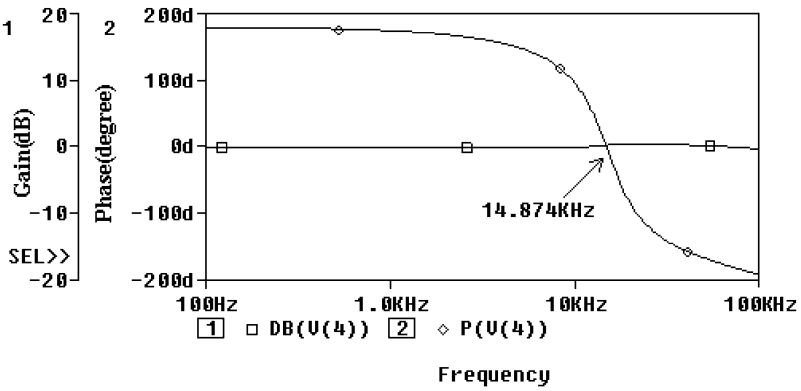

Fig. 4 Gain and phase responses of the all-pass filter obtained for circuit-III of Fig. 2(c)

of circuit-I and Fig. 6 shows the phase and gain response of circuit-III. The simulated notch frequency was found to be 15.48 kHz for both circuit-I and circuit-III of Fig. 2, which is close to the theoretical value.

5 Integration Aspects

The integration aspect of the new proposed circuit is next explored. As far as the active element is concerned, its implementation in CMOS technology is available. The passive elements in form of resistor and capacitor should also be compatible in CMOS technology. The resistor can be replaced by active-MOS resistor with added advantage of tunability through external voltage [1]. Similarly, there are techniques of implementing capacitor in MOS technology [2]. Since the used capacitor is in grounded form, it is further favorable as far as implementation is concerned. Thus the proposed circuit is quite suitable for IC implementation.

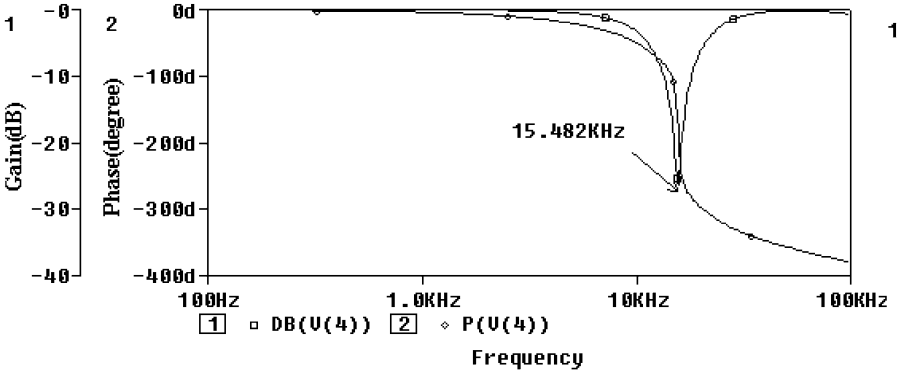

Fig. 5 Gain and phase responses of the notch filter obtained for circuit-I of Fig. 2(a)

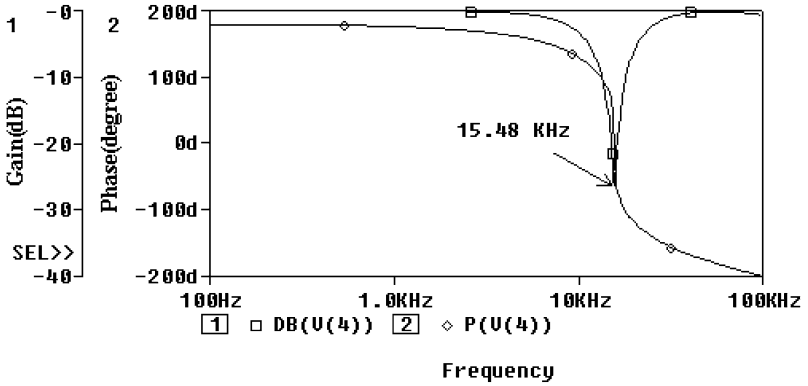

Fig. 6 Gain and phase responses of the notch filter obtained for circuit-III of Fig. 2(c)

6 Conclusion

This paper has presented four new second-order voltage-mode cascadable all-pass/notch filters, employing one FDCCII, two resistors and two grounded capacitors. The salient features of the proposed circuits are high-input and low-output impedance, single active element and use of grounded capacitors, which are suitable for integrated circuit implementation. The proposed circuits are verified through PSPICE simulations using TSMC 0.35 μm CMOS parameters. IC implementation of these circuits for commercial use is an open area for further study.

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