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Novel Voltage-Mode All-Pass Filter Based on Using DVCCs

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Abstract In this paper, a novel design for realizing a voltage-mode (VM) all-pass filter utilizing two differential voltage current conveyors (DVCCs) is proposed. Also, the suggested filter uses a canonical number of passive elements (one grounded capacitor and one resistor) without requiring any element matching condition. The proposed filter has high input and low output impedances, which make it suitable for cascading. The effects of the nonidealities of the DVCCs on the proposed design are investigated. As an application, a quadrature oscillator is designed using the proposed VM all-pass filter and an integrator. The proposed filter and oscillator circuits are simulated using the SPICE simulation program to confirm the theory.

Keywords All-pass filter · Differential voltage current conveyor · Oscillator

1 Introduction

First-order all-pass filters are most often used for matching phase in systems where phase is important, for producing delays in circuits that need to delay a signal, and for creating 90° shifts for quadrature modulators. The literature discusses a rich collection of various circuits for realizing voltage-mode (VM) first-order all-pass filters [1–3, 6–23]. However, most of the previously reported circuits need at least one matching constraint to realize the transfer function (TF) of a first-order all-pass filter

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[1, 2, 6–8, 11–14, 16, 19–23]. The recently published all-pass filters in [17] employ two floating resistors and one grounded capacitor together with a fully differential current conveyor (FDCCII) without requiring a matching condition. However, it has neither high input impedance nor low output impedance, which is a need in cascading systems. In addition, the FDCCII is an eight-terminal active element, which has a more complex internal structure compared with other active elements.

Differential voltage current conveyors (DVCCs) [5] and differential difference current conveyors (DDCCs) [4] are versatile active elements which can simplify the design of active filters. Although the recently proposed DVCC-based VM all-pass filters in [13, 14] employ grounded capacitors and resistors, which are advantageous in the reduction of parasitic impedance effects as well as in easy integration in VLSI systems, they still suffer from the need of passive component matching.

The DDCC-based all-pass filters in [3, 9, 10, 18] are good design examples where a canonical number of passive and active elements (one resistor, one capacitor, and single DDCC) are employed and no matching constraint is required. However, all of these filters do not possess high input impedance and/or low output impedance. Recently, a resistorless VM all-pass filter employing two DVCCs and a single grounded capacitor has been reported [15]. Although the proposed circuit in [15] does not require a matching condition and provides low output impedance, it still suffers from a lack of high input impedance.

In this paper, we propose a new all-pass filter which uses only two positive-type DVCCs (DVCC+), one resistor, and one grounded capacitor. The proposed filter does not need a matching condition to realize the all-pass filter TF and enjoys both high input and low output impedance features. The nonideality analysis of the proposed filter is given. In addition, the parasitic impedance effects of the active elements on the proposed filter are investigated. As an application, a quadrature oscillator employing the proposed filter connected to an integrator in a closed loop is presented. The performance of the proposed filter is verified using the SPICE program.

2 Proposed All-Pass Filter

The DVCC+, whose electrical symbol is shown in Fig. 1, is a four-terminal active device which can be described by the following matrix equation:

$$\begin{bmatrix} I_{Y_1} \\ I_{Y_2} \\ V_X \\ I_{Z+} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_{Y_1} \\ V_{Y_2} \\ I_X \\ V_{Z+} \end{bmatrix} \tag{1}$$

In Fig. 1, the port labeled X represents a low-impedance current input, ports Y_1 and Y_2 are high-impedance voltage inputs, and the $Z+$ terminal is the high-impedance current output. The DVCC+ can be used to construct basic current processing blocks such as amplifier, integrator, differentiator, summer, and subtractor. From (1), it can be seen that the voltage and current gains of the DVCC+ are ideally equal to unity. However, a nonideal DVCC+ can be represented by

$$I_{Y_1} = I_{Y_2} = 0, \qquad V_X = \beta_1 V_{Y_1} - \beta_2 V_{Y_2}, \qquad I_{Z+} = \alpha I_X, \tag{2}$$

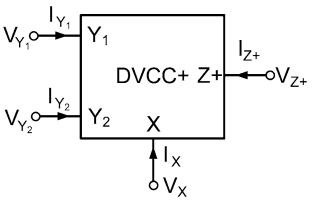


Fig. 1 Electrical symbol of the DVCC+

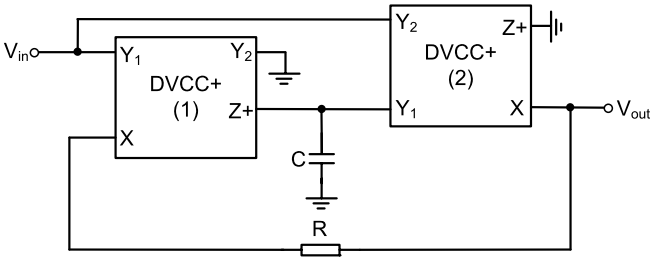


Fig. 2 The proposed all-pass filter

where β_k $(k = 1, 2)$ and α are the nonideal voltage and current gains of the DVCC+, respectively.

Using two DVCC+s and a canonical number of passive elements (one resistor and one capacitor), a VM all-pass filter can be obtained, as shown in Fig. 2. The input of the proposed filter is connected to the Y terminals of the DVCC+s and its output is taken from the X terminal of the second DVCC+. Therefore, the proposed filter has high input and low output impedances. Moreover, the filter does not require passive element matching conditions.

Assuming an ideal DVCC+, routine analysis of the circuit in Fig. 2 gives the following TF:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1 - sCR}{1 + sCR}. \tag{3}$$

From (3), the phase of the filter is found as

$$\varphi(\omega) = -2\tan^{-1}(\omega CR). \tag{4}$$

Therefore, an all-pass filter with positive unity gain is obtained. The pole frequency of the introduced filter is calculated as

$$f_0 = \frac{1}{2\pi CR}. \tag{5}$$

Note that by interchanging the resistor and capacitor in Fig. 2, an all-pass filter with a negative unity gain can be obtained as

$$\frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{1 - sCR}{1 + sCR} \tag{6}$$

which has a phase response in the frequency domain as

$$\varphi(\omega) = 180^\circ - 2\tan^{-1}(\omega C R). \tag{7}$$

However, the interchange of the capacitor and resistor in Fig. 2 results in an extra pole due to the series connection of C and R_{x1} (the parasitic resistances at terminal X of the first DVCC+). This extra pole degrades the high-frequency response performance of the proposed filter [25].

Taking into account the nonideal voltage and current gains of the DVCC+, the TF of the filter in Fig. 2 converts to

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{\alpha_1\beta_{11}\beta_{12} - s\beta_{22}CR}{\alpha_1\beta_{12} + sCR} \tag{8}$$

where β_{1n}, β_{2n}, and α_n $(n = 1, 2)$ are the voltage and current gains associated with the nth DVCC+. Assuming that all of the nonideal gains are constant in our frequency range of interest, the phase response of the filter is given as

$$\varphi(\omega) = -\tan^{-1}\left(\frac{\beta_{22}CR\omega}{\alpha_1\beta_{11}\beta_{12}}\right) - \tan^{-1}\left(\frac{CR\omega}{\alpha_1\beta_{12}}\right). \tag{9}$$

From (8) and (9), it can be realized that the nonideal gains of the DVCC+ slightly alter the magnitude and phase responses of the filter. Consequently, the pole frequency of the presented filter is found as

$$f_0 = \frac{\alpha_1\beta_{12}}{2\pi CR}. \tag{10}$$

The proposed filter has high input and low output impedances, a property which makes it attractive for cascading. In fact, the proposed filter can be connected to the output of another circuit without a loading effect, and no buffer is required for connecting a load to the proposed filter.

One can compare the proposed filter with the best prior solution proposed by Horng et al. [9]. Horng's filter is shown in Fig. 3. Although the filter in Fig. 3 employs only one DDCC together with one resistor and one grounded capacitor, and provides low output impedance, it suffers from a lack of high input impedance. In contrast, the proposed filter in Fig. 2 enjoys both high input and low output impedances at the cost of using two DVCCs.

Finally, we mention that the floating resistor of the proposed filter can be realized by using electronically controllable CMOS-based floating resistors [24].

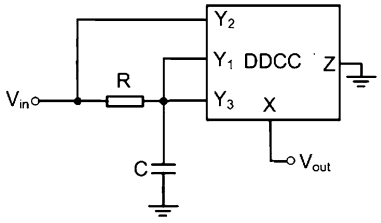


Fig. 3 Previously published all-pass filter [9]

3 Frequency-Dependent Gains and Stability Analysis

Practically, the voltage and current gains of the DVCC+ are frequency-dependent parameters which can be modeled as

$$\beta_{1n}(s) = \frac{\beta_{01n}}{1 + s\tau_{v1n}}, \qquad \beta_{2n}(s) = \frac{\beta_{02n}}{1 + s\tau_{v2n}}, \qquad \alpha_n(s) = \frac{\alpha_{0n}}{1 + s\tau_{in}} \tag{11}$$

where β_{01n}, β_{02n} and α_{0n} denote the low-frequency voltage and current gains of the nth DVCC+. Here, $\tau_{v1n} = 1/\omega_{\beta 1n}$, $\tau_{v2n} = 1/\omega_{\beta 2n}$ and $\tau_{in} = 1/\omega_{\alpha n}$, where $\omega_{\beta 1n}$, $\omega_{\beta 2n}$ and $\omega_{\alpha n}$ are, respectively, pole frequencies of the voltage gains and current gain of the nth DVCC+, ideally equal to infinity. Reanalysis of the proposed filter results in the modified TF of (8) as

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{a_0 - a_1 s - a_2 s^2 - a_3 s^3 - a_4 s^4}{(1 + s\tau_{v11})(1 + s\tau_{v22})[\alpha_{01}\beta_{012} + sCR + s^2 CR(\tau_{i1} + \tau_{v12}) + s^3 CR\tau_{i1}\tau_{v12}]}, \tag{12}$$

where

$$\begin{aligned} a_0 &= \alpha_{01}\beta_{011}\beta_{012}, \\ a_1 &= CR\beta_{022} - \alpha_{01}\beta_{011}\beta_{012}\tau_{v22}, \\ a_2 &= CR\beta_{022}(\tau_{i1} + \tau_{v11} + \tau_{v12}), \\ a_3 &= CR\beta_{022}(\tau_{i1}(\tau_{v11} + \tau_{v12}) + \tau_{v11}\tau_{v12}), \\ a_4 &= CR\tau_{i1}\tau_{v11}\tau_{v12}\beta_{022}. \end{aligned} \tag{13}$$

From (12) it can be seen that extra poles appear in the denominator of the TF of the filter. If the Routh-Hurwitz stability criterion is applied to the denominator of (12) for the proposed filter, the following constraints are obtained:

$$\begin{cases} s^3, & CR\tau_{i1}\tau_{v12} > 0, \quad CR, \\ s^2, & CR(\tau_{i1} + \tau_{v12}) > 0, \quad \alpha_{01}\beta_{012}, \\ s^1, & \frac{CR(\tau_{i1}+\tau_{v12}) - \tau_{i1}\tau_{v12}\alpha_{01}\beta_{012}}{\tau_{i1}+\tau_{v12}} > 0, \\ s^0, & \alpha_{01}\beta_{012} > 0. \end{cases} \tag{14}$$

From (14) it can be seen that all the coefficients are always greater than zero, except the coefficient given below:

$$\frac{CR(\tau_{i1} + \tau_{v12}) - \tau_{i1}\tau_{v12}\alpha_{01}\beta_{012}}{\tau_{i1} + \tau_{v12}} > 0. \tag{15}$$

From (15), the following inequality should be satisfied for stable all-pass filter responses:

$$R > \frac{1}{C}\frac{\tau_{i1}\tau_{v12}\alpha_{01}\beta_{012}}{\tau_{i1} + \tau_{v12}}. \tag{16}$$

As an example, if $\tau_{v12} = \tau_{i1} = 1 \times 10^{-9}$ sec/rad, $C = 50 \times 10^{-12}$ F, and low-frequency nonideal gains are equal to unity, $R > 10\ \Omega$ is obtained for stable all-pass responses. Fortunately, the proposed all-pass filter is always stable because $R = 10\ \Omega$ is much less than the X terminal parasitic resistance values of the DVCC+s, as will be shown shortly.

4 Parasitic Impedance Effects

Considering the parasitic impedances of the DVCC+, the matrix relationship of (1) is converted to

$$\begin{bmatrix} I_{Y_1} \\ I_{Y_2} \\ V_X \\ I_{Z+} \end{bmatrix} = \begin{bmatrix} sC_{y1} + \frac{1}{R_{y1}} & 0 & 0 & 0 \\ 0 & sC_{y2} + \frac{1}{R_{y2}} & 0 & 0 \\ \beta_1 & -\beta_2 & R_x & 0 \\ 0 & 0 & \alpha & sC_{z+} + \frac{1}{R_{z+}} \end{bmatrix} \begin{bmatrix} V_{Y_1} \\ V_{Y_2} \\ I_X \\ V_{Z+} \end{bmatrix}. \tag{17}$$

Here R_x, R_y, R_{z+}, C_y and C_{Z+} are the parasitic resistances and capacitances at their relevant terminal. As an example, considering only the Z and Y terminal parasitic impedances of the all-pass filter in Fig. 2, the TF of (3) turns to be

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{\frac{a-b}{d} - (b-c)s}{\frac{a+b}{d} + (b+c)s}. \tag{18}$$

where a and b are found as

$$\begin{aligned} a &= (R_{z1+} \| R_{y12}) + R_{x2}, \\ b &= R + R_{x1}, \\ c &= R_{x2}, \\ d &= (R_{z1+} \| R_{y12})(C + C_{z1+} + C_{y12}). \end{aligned} \tag{19}$$

Here R_{x1} and R_{x2} denote the parasitic resistances at the X terminals of the first and second DVCC+s. Similarly, C_{y12} is the parasitic capacitor at the Y_1 terminal of the second DVCC+ and C_{Z1+} is the parasitic capacitor at the $Z+$ terminal of the first DVCC+. It is observed from (18) that the new resonance frequency due to the Z and Y terminal parasitic impedances is found as $f_0 = (a+b)/[2\pi d(b+c)]$. For realizing an ideal all-pass filter, one should select $b^2 = ac$ or equivalently $(R + R_{x1})^2 = [(R_{z1+} \| R_{y12}) + R_{x2}]R_{x2}$.

If taking into account only the X terminal parasitic impedances of the all-pass filter in Fig. 2, the TF of (3) is expressed as follows:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1 - sC(R + R_{x1} - R_{x2})}{1 + sC(R + R_{x1} + R_{x2})}. \tag{20}$$

Therefore, the value of R must be selected much higher than R_{x1} and R_{x2} to obtain an ideal all-pass filter.

5 Simulation Results and Discussion

To confirm the theoretical results, the proposed VM all-pass filter is simulated with the SPICE program using 0.18 μm TSMC CMOS technology parameters as given in Table 1. The CMOS implementation of the DVCC+ is shown in Fig. 4, which is obtained from the circuit proposed in [4] by grounding the gate of transistor M_7. For the DVCC+ of Fig. 4, the DC power supply voltages of ±1.5 V and bias voltage of $V_B = 0.95$ V are selected. All of the bulks of the NMOS and PMOS transistors of the DVCC+ of Fig. 4 are respectively connected to the most negative and positive DC power supply voltages. The dimensions of the CMOS transistors employed in the DVCC+ are depicted in Table 2. Additionally, $R_x = 0.474$ kΩ and the parameters of the nonideal gains of the DVCC+ in Fig. 4 are calculated as $\alpha_o \cong 0.993$, $\beta_{o1} \cong \beta_{o2} \cong 0.996$, $f_\alpha = 854$ MHz, $f_{\beta 1} = 1.1$ GHz, and $f_{\beta 2} = 971$ MHz.

The passive elements are selected as $R = 5$ kΩ and $C = 50$ pF to obtain a phase shift of 90° at 636.6 kHz. The magnitude and phase responses of the filter are shown in Fig. 5.

Table 1 Parameters of the CMOS transistors of the DVCC+ used in SPICE simulations

0.18 μm TSMC CMOS parameters
.MODEL N NMOS (LEVEL = 7
+VERSION = 3.1 TNOM = 27 TOX = 4.1E-9 XJ = 1E-7 NCH = 2.3549E17
+VTH0 = 0.3725327 K1 = 0.5933684 K2 = 2.050755E-3 K3 = 1E-3 K3B = 4.5116437
+W0 = 1E-7 NLX = 1.870758E-7 DVT0W = 0 DVT1W = 0 DVT2W = 0
+DVT0 = 1.3621338 DVT1 = 0.3845146 DVT2 = 0.0577255 U0 = 259.5304169
+UA = −1.413292E-9 UB = 2.229959E-18 UC = 4.525942E-11 VSAT = 9.411671E4
+A0 = 1.7572867 AGS = 0.3740333 B0 = −7.087476E-9 B1 = −1E-7
+KETA = −4.331915E-3 A1 = 0 A2 = 1 RDSW = 111.886044 PRWG = 0.5
+PRWB = −0.2 WR = 1 WINT = 0 LINT = 1.701524E-8 XL = 0 XW = −1E-8
+DWG = −1.365589E-8 DWB = 1.045599E-8 VOFF = −0.0927546
+NFACTOR = 2.4494296 CIT = 0 CDSC = 2.4E-4 CDSCD = 0 CDSCB = 0
+ETA0 = 3.175457E-3 ETAB = 3.494694E-5 DSUB = 0.0175288 PCLM = 0.7273497
+PDIBLC1 = 0.1886574 PDIBLC2 = 2.617136E-3 PDIBLCB = −0.1
+DROUT = 0.7779462 PSCBE1 = 3.488238E10 PSCBE2 = 6.841553E-10
+PVAG = 0.0162206 DELTA = 0.01 RSH = 6.5 MOBMOD = 1 PRT = 0
+UTE = −1.5 KT1 = −0.11 KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9 UB1 = −7.61E-18
+UC1 = −5.6E-11 AT = 3.3E4 WL = 0 WLN = 1 WW = 0 WWN = 1 WWL = 0
+LL = 0 LLN = 1 LW = 0 LWN = 1 LWL = 0 CAPMOD = 2 XPART = 0.5
+CGDO = 8.53E-10 CGSO = 8.53E-10 CGBO = 1E-12 CJ = 9.513993E-4 PB = 0.8
+MJ = 0.3773625 CJSW = 2.600853E-10 PBSW = 0.8157101 MJSW = 0.1004233
+CJSWG = 3.3E-10 PBSWG = 0.8157101 MJSWG = 0.1004233 CF = 0
+PVTH0 = −8.863347E-4 PRDSW = −3.6877287 PK2 = 3.730349E-4
+WKETA = 6.284186E-3 LKETA = −0.0106193 PU0 = 16.6114107
+PUA = 6.572846E-11 PUB = 0 PVSAT = 1.112243E3 PETA0 = 1.002968E-4
+PKETA = −2.906037E-3

Table 1 (*Continued*)

0.18 μm TSMC CMOS parameters
.MODEL P PMOS (LEVEL = 7
+VERSION = 3.1 TNOM = 27 TOX = 4.1E-9 XJ = 1E-7 NCH = 4.1589E17
+VTH0 = −0.3948389 K1 = 0.5763529 K2 = 0.0289236 K3 = 0 K3B = 13.8420955
+W0 = 1E-6 NLX = 1.337719E-7 DVT0W = 0 DVT1W = 0 DVT2W = 0
+DVT0 = 0.5281977 DVT1 = 0.2185978 DVT2 = 0.1 U0 = 109.9762536
+UA = 1.325075E-9 UB = 1.577494E-21 UC = −1E-10 VSAT = 1.910164E5
+A0 = 1.7233027 AGS = 0.3631032 B0 = 2.336565E-7 B1 = 5.517259E-7
+KETA = 0.0217218 A1 = 0.3935816 A2 = 0.401311 RDSW = 252.7123939 PRWG = 0.5
+PRWB = 0.0158894 WR = 1 WINT = 0 LINT = 2.718137E-8 XL = 0 XW = −1E-8
+DWG = −4.363993E-8 DWB = 8.876273E-10 VOFF = −0.0942201 NFACTOR = 2
+CIT = 0 CDSC = 2.4E-4 CDSCD = 0 CDSCB = 0 ETA0 = 0.2091053
+ETAB = −0.1097233 DSUB = 1.2513945 PCLM = 2.1999615 PDIBLC1 = 1.238047E-3
+PDIBLC2 = 0.0402861 PDIBLCB = −1E-3 DROUT = 0 PSCBE1 = 1.034924E10
+PSCBE2 = 2.991339E-9 PVAG = 15 DELTA = 0.01 RSH = 7.5 MOBMOD = 1
+PRT = 0 UTE = −1.5 KT1 = −0.11 KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9
+UB1 = −7.61E-18 UC1 = −5.6E-11 AT = 3.3E4 WL = 0 WLN = 1 WW = 0 WWN = 1
+WWL = 0 LL = 0 LLN = 1 LW = 0 LWN = 1 LWL = 0 CAPMOD = 2 XPART = 0.5
+CGDO = 6.28E-10 CGSO = 6.28E-10 CGBO = 1E-12 CJ = 1.160855E-3
+PB = 0.8484374 MJ = 0.4079216 CJSW = 2.306564E-10 PBSW = 0.842712
+MJSW = 0.3673317 CJSWG = 4.22E-10 PBSWG = 0.842712 MJSWG = 0.3673317
+CF = 0 PVTH0 = 2.619929E-3 PRDSW = 1.0634509 PK2 = 1.940657E-3
+WKETA = 0.0355444 LKETA = −3.037019E-3 PU0 = −1.0227548 PUA = −4.36707E-11
+PUB = 1E-21 PVSAT = −50 PETA0 = 1E-4 PKETA = −5.167295E-3

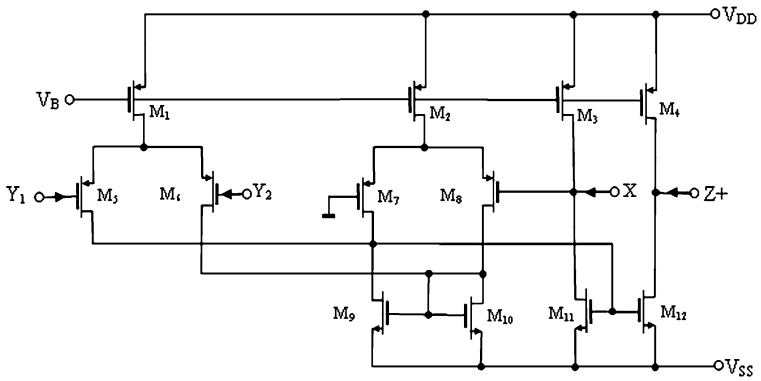


Fig. 4 Internal structure of the DVCC+

The time-domain response of the proposed VM all-pass filter for a sinusoidal input signal with 50 mV peak amplitude is shown in Fig. 6. The discrepancy between ideal and simulated results can be attributed to the nonideal gain and parasitic impedance

Table 2 Transistor aspect ratios of the DVCC+ circuit shown in Fig. 4

PMOS transistors	$W(\mu m)/L(\mu m)$
$M_1, M_2, M_5, M_6, M_7, M_8$	7.2/0.18
M_3, M_4	14.4/0.18
NMOS transistors	$W(\mu m)/L(\mu m)$
$M_9, M_{10}, M_{11}, M_{12}$	4.32/0.18

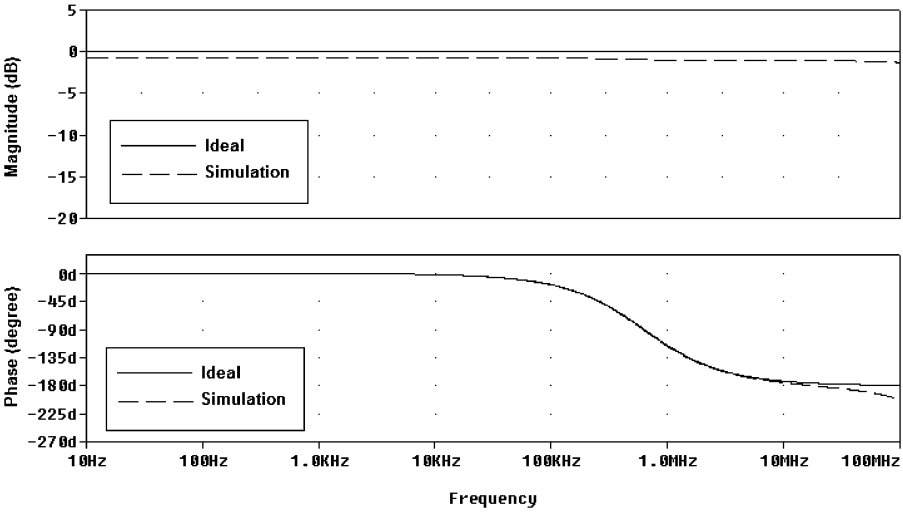


Fig. 5 The magnitude and phase responses of the introduced all-pass filter design

effects of the DVCC+s, especially X terminal parasitic resistor effects. The variation of the total harmonic distortion (THD) versus the applied sinusoidal input voltage for the proposed all-pass filter at its pole frequencies is given in Fig. 7. It can be seen that the THD values of the proposed filters remain below 5% for sinusoidal input signals up to 140 mV peak-to-peak. The total power dissipation of the proposed filter is found to be 0.3 mW.

6 Application of the Proposed Filter

To illustrate the utility of the proposed first-order all-pass filter, it is connected in cascade to an integrator in a closed loop to construct a quadrature oscillator, as shown in Fig. 8. Since the proposed filter has high input and low output impedances, no buffer is required to connect it to the integrator circuit. It can be seen that the proposed oscillator employs only three DVCC+s and four passive components. Analysis of the proposed oscillator circuit assuming ideal DVCC+s yields the following characteris-

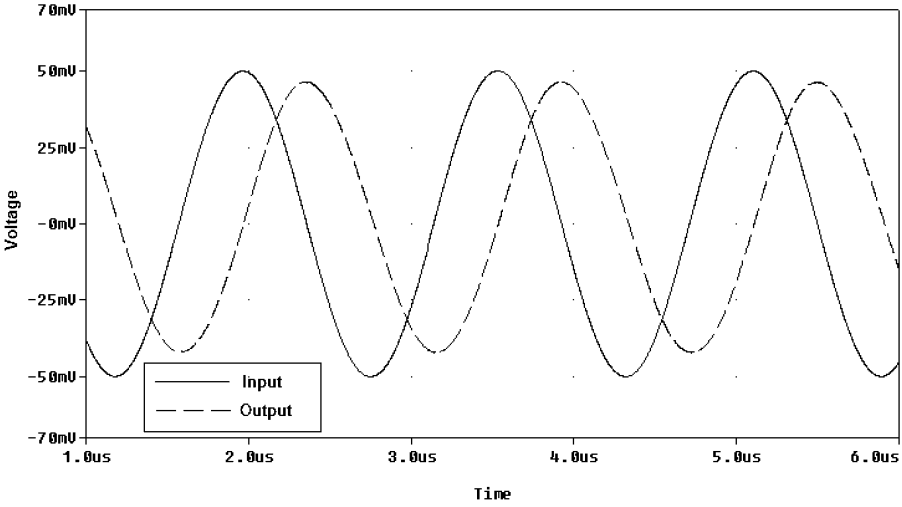
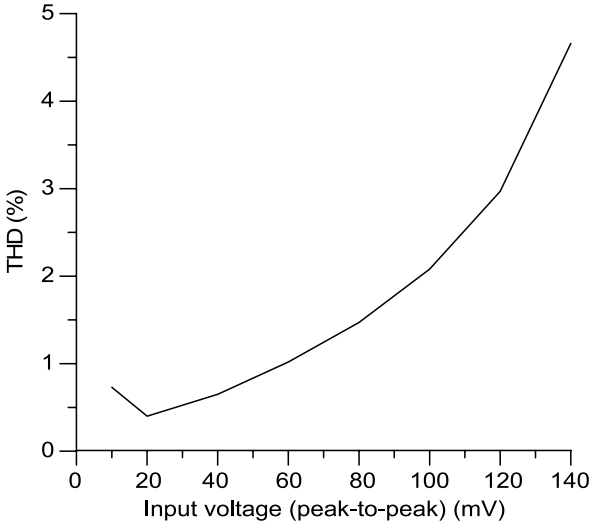


Fig. 6 Time-domain response of the proposed all-pass filter at 636.6 kHz

Fig. 7 THD variation of the proposed all-pass filter against applied input voltage



tic equation:

$$s^2 + \left(\frac{1}{C_1R_1} - \frac{1}{C_2R_2}\right)s + \frac{1}{C_1C_2R_1R_2} = 0. \tag{21}$$

Replacing $s = j\omega$ in (21) gives the frequency of oscillation (FO) and condition of oscillation (CO) as

$$\text{FO:} \quad \omega_o = \frac{1}{\sqrt{C_1C_2R_1R_2}}, \tag{22a}$$

$$\text{CO:} \quad C_1R_1 \geq C_2R_2. \tag{22b}$$

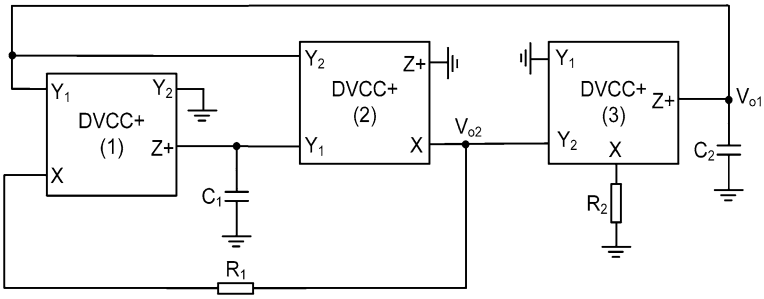


Fig. 8 Quadrature oscillator using the proposed all-pass filter and an integrator

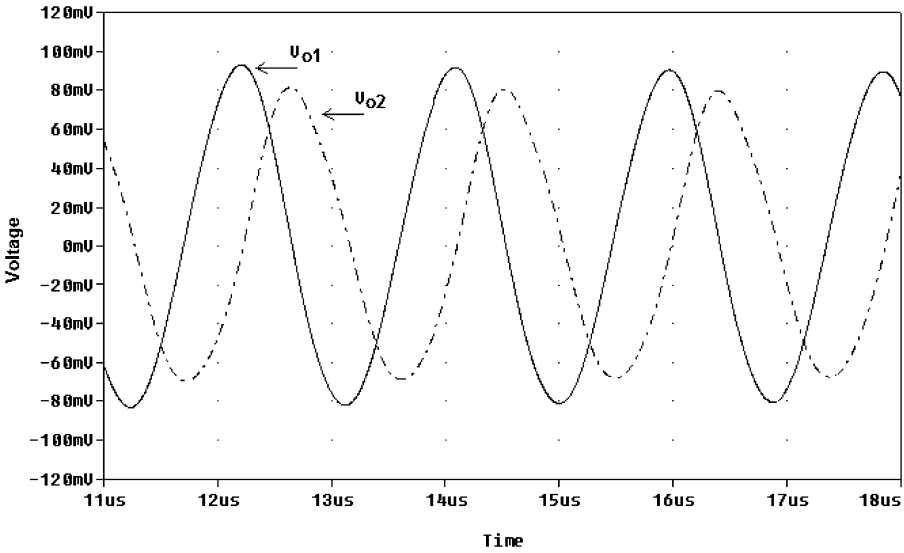


Fig. 9 Outputs of the proposed quadrature oscillator

The proposed oscillator circuit is tested using the following design: $C_1 = C_2 = 50$ pF, $R_1 = 6.25$ kΩ, and $R_2 = 5$ kΩ, for sustained oscillation with a frequency of 569.4 kHz. The simulation results are shown in Fig. 9, where the phase difference between two outputs V_{o1} and V_{o2} is 90°. The total power dissipation of the proposed oscillator is found as 0.47 mW.

7 Conclusion

In this paper, a novel VM first-order all-pass filter employing two DVCC+s as active elements and a minimum number of passive elements is proposed. The filter has high input and low output impedances, a feature which makes it suitable for cascading without requiring buffers. In addition, no passive component matching constraint is required for the proposed filter. The theoretical analysis is verified with

the SPICE simulation program. The discrepancy between simulation and theoretical results arises from the effects of nonideal gains and parasitic impedances of the DVCC+s.

References

1. U. Çam, O. Çiçekoğlu, M. Gülsoy, H. Kuntman, New voltage and current mode first-order all-pass filters using single FTFN. Frequenz **54**(7–8), 177–179 (2000)
2. O. Cicekoglu, H. Kuntman, S. Berk, All-pass filters using a single current conveyor. Int. J. Electron. **86**(8), 947–955 (1999)
3. H.P. Chen, K.H. Wu, Grounded-capacitor first-order filter using minimum components. IEICE Trans. Fund. **E89-A**(12), 3730–3731 (2006)
4. W. Chiu, S.I. Liu, H.W. Tsao, J.J. Chen, CMOS differential difference current conveyors and their applications. IEE Proc. Circ. Dev. Syst. **143**, 91–96 (1996)
5. H.O. Elwan, A.M. Soliman, Novel CMOS differential voltage current conveyor and its applications. IEE Proc. Circ. Dev. Syst. **144**(3), 195–200 (1997)
6. S.J.G. Gift, The application of all-pass filters in the design of multiphase sinusoidal systems. Microelectron. J. **31**, 9–13 (2000)
7. M. Higashimura, Y. Fukui, Realization of all-pass networks using a current conveyor. Int. J. Electron. **65**(2), 249–250 (1988)
8. J.W. Horng, Current conveyors based allpass filters and quadrature oscillators employing grounded capacitors and resistors. Comput. Electr. Eng. **31**(1), 81–92 (2005)
9. J.W. Horng, C.L. Hou, C.M. Chang, Y.T. Lin, I.C. Shiu, W.Y. Chiu, First-order all-pass filter and sinusoidal oscillators using DDCCs. Int. J. Electron. **93**(7), 457–466 (2006)
10. M.A. Ibrahim, H. Kuntman, O. Cicekoglu, First-order all-pass filter canonical in the number of resistors and capacitors employing a single DDCC. Circ. Syst. Signal Process. **22**(5), 525–536 (2003)
11. I.A Khan, S. Maheshwari, Simple first order all-pass section using a single CCII. Int. J. Electron. **87**(3), 303–306 (2000)
12. S. Maheshwari, New voltage and current-mode APS using current controlled conveyor. Int. J. Electron. **91**(12), 735–743 (2004)
13. S. Maheshwari, High input impedance VM-APSs with grounded passive elements. IET Circ. Dev. Syst. **1**(1), 72–78 (2007)
14. S. Maheshwari, High input impedance voltage-mode first-order all-pass sections. Int. J. Circ. Theory Appl. **36**(4), 511–522 (2008)
15. S. Maheshwari, A canonical voltage-controlled VM-APS with a grounded capacitor. Circ. Syst. Signal Process. **27**, 123–132 (2008)
16. S. Maheshwari, I.A Khan, Novel first order all-pass sections using a single CCIII. Int. J. Electron. **88**(7), 773–778 (2001)
17. S. Maheshwari, I.A. Khan, J. Mohan, Grounded capacitor first-order filters including canonical forms. J. Circ. Syst. Comput. **15**, 289–300 (2006)
18. B. Metin, O. Cicekoglu, K. Pal, DDCC based all-pass filters using minimum number of passive elements, in 50th Midwest Symposium on Circuits and Systems (MWSCAS 2007) (2007), pp. 518–521
19. K. Pal, Realization of current conveyor all-pass networks. Int. J. Electron. **50**(2), 165–168 (1981)
20. N. Pandy, S.K. Paul, All-pass filters based on CCII- and CCCII-. Int. J. Electron. **91**(8), 485–489 (2004)
21. A.M. Soliman, Realization of operational-amplifier allpass network. Electron. Lett. **9**, 67–68 (1973)
22. A.M. Soliman, Generation of current conveyor based all-pass filters from op-amp based circuits. IEEE Trans. CAS-II **44**(4), 324–330 (1997)
23. A. Toker, S. Ozcan, H. Kuntman, O. Cicekoglu, Supplementary all-pass sections with reduced number of passive elements using a single current conveyor. Int. J. Electron. **88**(9), 969–976 (2001)
24. G. Wilson, P.K. Chan, Floating CMOS resistor. Electron. Lett. **29**, 306–307 (1993)
25. E. Yuce, S. Minaei, Universal current-mode filters and parasitic impedance effects on the filter performances. Int. J. Circ. Theory Appl. **36**, 161–171 (2008)