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Automatic Synthesis of VFs and VMs by Applying Genetic Algorithms

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Abstract An automatic synthesis method is introduced to design voltage followers (VFs) and voltage mirrors (VMs) by performing evolutionary operations. It is shown that the nullor element is useful to introduce a new genetic representation to codify the behavior of the VF by a chromosome divided by four genes: small-signal (genSS), synthesis of the nullor by MOSFET (genSMos), bias (genBias), and synthesis of current mirrors (genCM). Further, it is shown that the behavior of the VM can be codified by evolving the chromosome of the VF. The proposed synthesis method uses SPICE to evaluate the fitness of the VF and VM. Finally, we show the synthesis of several VFs and VMs which are designed using standard CMOS technology of 0.35 μm. The applications and evolution of the VF and VM to synthesize more complex devices such as current conveyors (CCs) and inverting CCs are briefly discussed.

Keywords Evolutionary electronics · Genetic algorithms · Circuit synthesis · VF · VM · Nullor

1 Introduction

Analog circuit design is very amenable to evolutionary techniques [10, 20], where in contrast to digital design, there is no solid set of design rules or procedures to automate analog circuit synthesis [14, 16, 17, 24, 27, 31, 32]. As already shown in [10, 14, 16, 17, 20, 24, 32], analog synthesis is a challenging problem because the analog design process is characterized by a combination of experience and intuition, and requires creativity to deal with the large number of free parameters and the sometimes

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obscure interactions between them. Furthermore, genetic algorithms (GAs) are quite useful for analog synthesis. They start from high-level descriptions and operate on the principle of "survival of the fittest," so that they have the capability to generate new design solutions from a population of existing solutions, discarding the solutions which have an inferior performance or fitness.

Actually, in [16] there is introduced a new kind of genetic representation called analog genetic encoding (AGE), which permits the simultaneous evolution of the topology and sizing of the networks. In [24] and [17] it is given a solution for analog and radio frequency (RF) circuit sizing optimization problems, and a SPICE-based multi-objective evolutionary algorithm for sizing analog blocks. To reduce the search space, the method in [32] starts with idealized elements which are replaced by metal oxide semiconductor field-effect transistors (MOSFETs). Following this direction, this work introduces a novel genetic representation to synthesize analog circuits from high-level descriptions using nullors [15], and a refinement process is executed to synthesize complementary metal oxide semiconductor (CMOS) compatible voltage followers (VFs) and voltage mirrors (VMs) by exploiting their regularity, symmetry and modularity.

As already shown in [15], the nullator, the norator and the nullor are pathological elements which have been quite useful for the development of novel analysis, synthesis and design methodologies, and they can be used to represent a wide variety of different active devices [21]. For instance, the nullator (O) can be used to describe the ideal behavior of the VF [27], and the norator (P) to describe the current follower (CF) [31]. The interconnection of a VF with either a CF or current mirrors (CMs) generates current conveyors (CCs) [2, 15, 21–23, 25, 31]. On the other hand, Os and Ps fail to represent the positive type second-generation CC (CCII+) and the inverting CC (ICC) [3]. Therefore, to derive the nullor representation of the CCII+ and ICC, the VM and the CM were introduced in [4, 33, 34].

The VF, CF, VM and CM find applications in filtering [3, 4, 33, 34], and single resistance controlled oscillators (SRCOs) [11, 26]. The combination of a VF with CMs generates the CCII+, and it can be cascaded with a VF to design a current feedback operational amplifier (CFOA) [5, 6]. The ICCs are derived by using the VM [3], and they can be used to implement filters [7, 13, 18] and oscillators [28]. Henceforth, this paper introduces an automatic synthesis method to design VFs and VMs by applying GAs.

2 Genetic Representation of the VF and VM

The proposed GA highlights the usefulness of the nullor to codify the behavior of the VF. In Fig. 1 are shown three descriptions of the VF using one, two and four Os [27, 31]. In Fig. 2 are shown the three combinations to form O–P pairs, which are synthesized by MOSFETs as shown in Fig. 2(d).

The generation of an O–P pair can be codified by two bits to create the small-signal gene (genSS) described in Table 1. The combinations 00 and 11 are referred to Fig. 2(a), where 00 means that during the synthesis of the O–P pair, the source (S) of the MOSFET is associated to node i, while 11 means association to node j. The

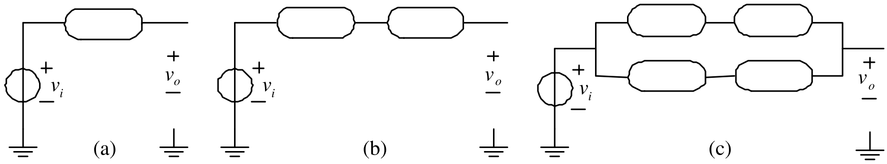

Fig. 1 Modeling the ideal behavior of the VF using nullators

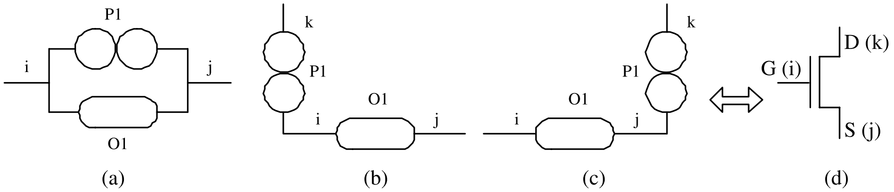

Fig. 2 Addition of a P-element: (**a**) Between nodes i and j, (**b**) at node i, and (**c**) at node j. (**d**) Synthesis of an O–P pair by a MOSFET

Table 1 Codification of genSS from Fig. 2

a0	a1	Union
0	0	Node i (Fig. 2(a))
0	1	Node i (Fig. 2(b))
1	0	Node j (Fig. 2(c))
0	0	Node j (Fig. 2(a))

synthesis of an O–P pair by a MOSFET can be codified using one bit to create the gene for synthesis of the MOSFET (genSMos), which describes the kind of transistor. Thus, when genSMos = '0' the O–P pair is synthesized by an N-MOSFET, and when genSMos = '1' by a P-MOSFET.

The addition of biases generates four combinations in each P element, which can be codified by two bits to create the bias gene (genBias), as described in Table 2. The combination 00 means that the drain (D) of the MOSFET is connected to Vdd, while a current bias (Iss) is connected between S and Vss. For the combination 01, D is connected to Vss, and a current bias (Idd) is connected between Vdd and S. For 10, Idd is between Vdd and D, and Iss is between S and Vss. 11 is similar to 10 by interchanging Iss and Idd.

Finally, the gene for synthesis of CMs (genCM) codifies the synthesis of Idd and Iss by CMs. For instance, if four CMs are available genCM has two bits: 00 for simple, 01 for simple cascode, 10 for Wilson, and 11 for improved Wilson CM.

From Table 3, 22 bits are used to codify a VF from Fig. 1(c). In Fig. 3(a) is shown the description of genSS and genBias for the combination 560828. In Fig. 3(b) is shown genSMos and genCM. As a result, the genetic representation for Fig. 3(b) is

Table 2 Addition of current biases

genBias	genBias	Connection	Connection
a3	a4	Drain	Source
0	0	Vdd	Iss
0	1	Vss	Idd
1	0	Idd	Iss
1	1	Iss	Idd

Table 3 Number of bits for each VF-chromosome consisting of four genes

#MOSFETs	genSS	genSMos	genBias	genCM	Chromosome
1	2	1	2	2	7 bits
2	4	2	4	2	12 bits
4	8	4	8	2	22 bits

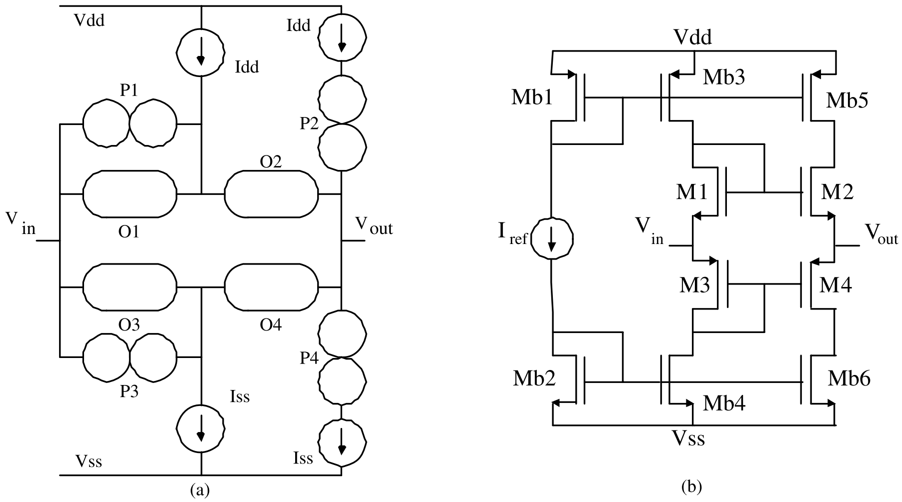

Fig. 3 (**a**) Description of a VF from Fig. 1(c), and (**b**) synthesis of the O–P pairs by MOSFETs, and of the current biases by simple CMs

codified by (1).

$$\text{Chromosome}_{\text{VF}} = \underbrace{00100010}_{\text{genSS}}\ \underbrace{0011}_{\text{genSMos}}\ \underbrace{10101111}_{\text{genBias}}\ \underbrace{00}_{\text{genCM}} \tag{1}$$

The topological description of a generic VM is shown in Fig. 4 [3, 7, 13, 18, 28], where it is appreciated that the VF is embedded within two complementary MOSFETs. Furthermore, the genetic representation of the VM increments (1)

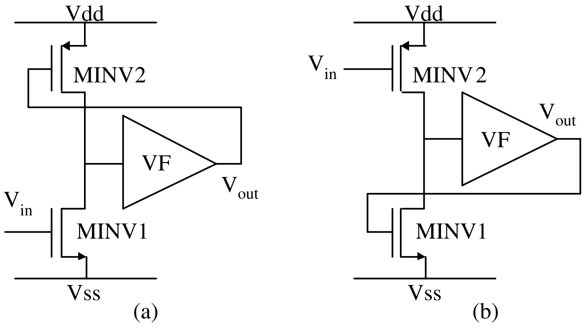

Fig. 4 VM description with (**a**) N-MOSFET and (**b**) P-MOSFET as the input

by one bit to describe if the input is connected to the MOSFET N or P. In this manner, a gene of inversion (genInv) is added to Table 3 to codify the VM as shown by (2).

$$\text{Chromosome}_{\text{VM}} = \underbrace{00100010}_{\text{genSS}}\ \underbrace{0011}_{\text{genSMos}}\ \underbrace{10101111}_{\text{genBias}}\ \underbrace{00}_{\text{genCM}}\ \underbrace{1}_{\text{genInv}} \tag{2}$$

3 Proposed Synthesis System

The proposed GA is sketched in Fig. 5. It begins with the creation of random solutions described by (1) to synthesize VFs, or (2) to synthesize VMs, called the initial population (spontaneous generation). This generation and the subsequent ones are evaluated three times. First, the initial population is passed through a first fitness which selects individuals whose input or output port is not connected to Vdd or Vss [27]. If an individual accomplishes this fitness, it is a valid VF topology and then the system decodes genSS, genSMos and genBias to generate a SPICE netlist (File 1) by adding the standard CMOS technology of 0.35 µm. If any topology is valid, the system generates a new population. MOSFETs are sized using [30], and the VFs are evaluated using SPICE.

A second selection is performed to select the VFs accomplishing Fitness 1 given by (3), where $k1$ can be provided by the user and its default value is 0.7. Again, if any VF is selected the system eliminates drastically all individuals and creates a new generation. If a VF is selected, the system decodes genCM by synthesizing all current biases (Idd and Iss) by CMs to generate a SPICE netlist (File 2). MOSFETs of the CMs are sized using [30] to evaluate the VF at the full transistor level using SPICE.

$$V_o > k1 \times V_i \tag{3}$$

Finally, a third selection is performed to select the VFs accomplishing Fitness 2 given by (4). Again $k2$ can be provided by the user and its default value is 0.9. If at least one CMOS VF accomplishes (4), the system finishes its search, i.e. it evaluates by

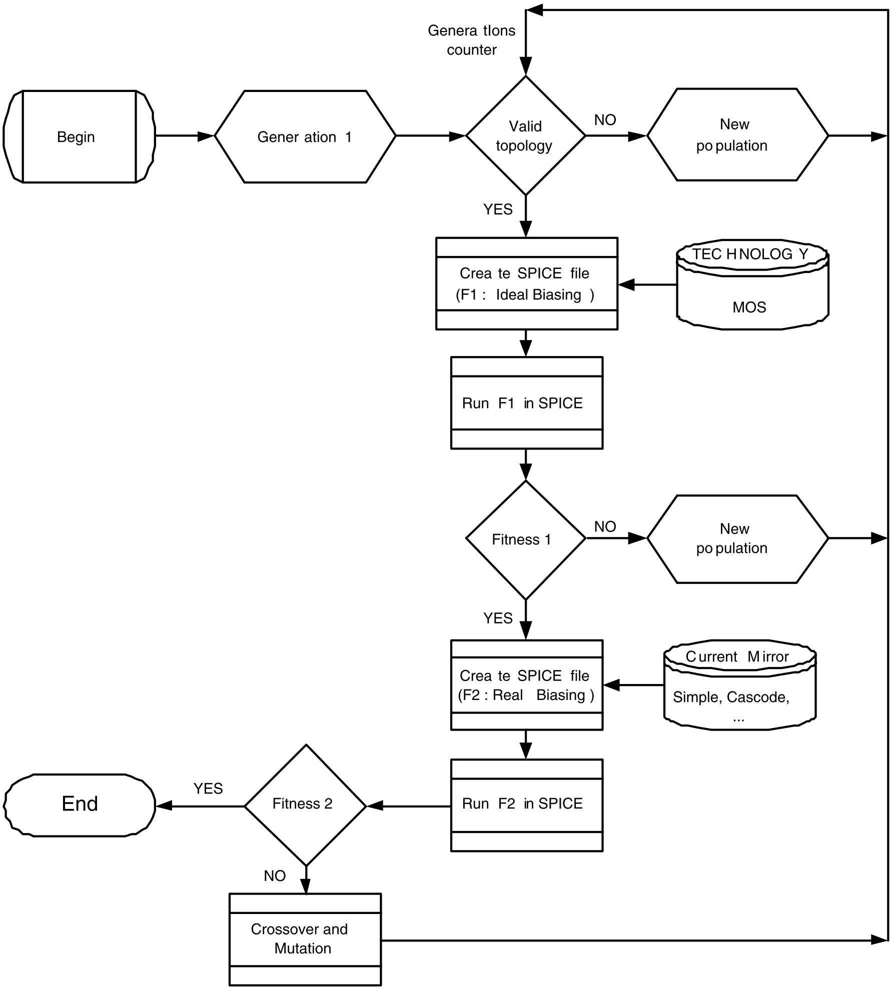

Fig. 5 Flow graph of the proposed synthesis system

elitism. Otherwise, crossover and mutation operations are performed to create a new generation.

$$V_o > k2 \times V_i \tag{4}$$

In the proposed GA, a VF is codified with ordered genes (genSS, genSMos, genBias, genCM). Therefore, if the parent VFs consist of (genSS1, genSM1, genB1, genCM1) and (genSS2, genSM2, genB2, genCM2), the standard 'one-point crossover' operation creates 14 new individuals [10]. However, to preserve an average number of individuals in the current population, only 2 to 4 new chromosomes are created by applying equal probability. Further, a chromosome is mutated randomly by changing the value of one bit. Also, in some cases after the crossover operation, some individuals do not have variation with the mutation operation.

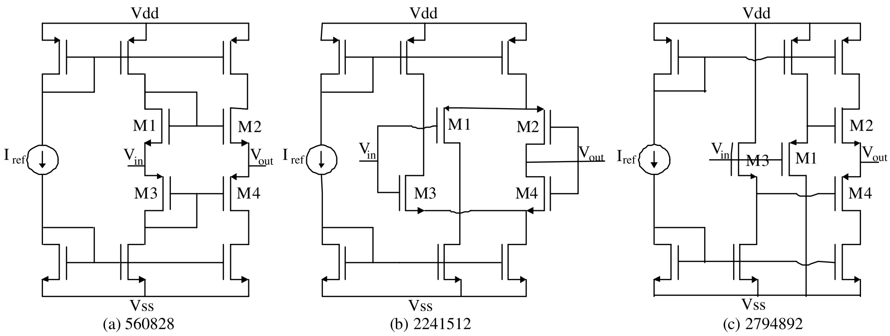

Fig. 6 Three known VFs synthesized from Fig. 1(c)

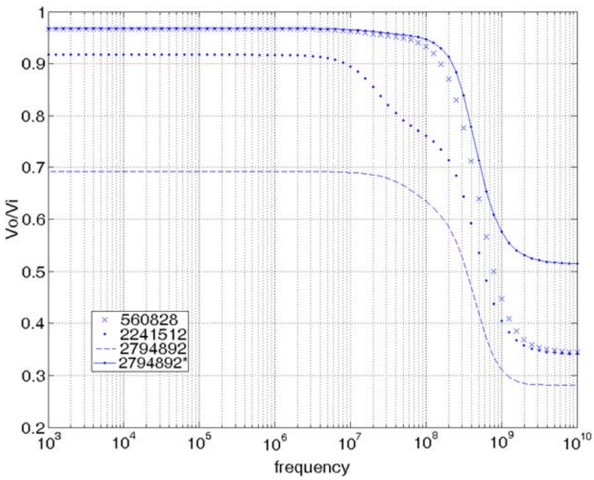

Fig. 7 Frequency response of the VFs from Fig. 6

4 Synthesis of VFs and VMs

The execution of the proposed GA beginning from Fig. 1(c) generates the three known CMOS VFs shown in Fig. 6. In each VF is shown its corresponding number of combinations. The VF in Fig. 6(a) has been used in [8, 9, 19, 30], the VF in Fig. 6(b) in [3], and the one in Fig. 6(c) in [5, 6] in its bipolar version to design the CCII+ and the CFOA.

When the sizes are $(W/L) = 30$ for all N-MOSFETs and 50 for all P-MOSFETs, with $L = 1.4$ μm, the frequency response is shown in Fig. 7. The gain below 0.7 corresponds to Fig. 6(c). However, when the bulk of M1–M4 has been connected to its corresponding source terminal, the gain is enhanced above 0.95. In this manner, these three VFs were selected when $k1 = 0.65$ and $k2 = 0.95$ in (3) and (4), respectively.

By beginning from Fig. 1(c), six new VFs are shown in Fig. 8. Table 4 shows the characteristics of the nine VFs simulated with $\text{Vdd} = 1.65$, $\text{Vss} = -1.65$, and $\text{Iref} = 100$ μA and using a load capacitor of 0.1 pF. The sizes are: $L = 1.4$ μm, $(W/L) = 30$

Table 4 SPICE simulation results for the VFs in Figs. 6 and 8

VF Chromosome	560828	2241512	2794892	110381	1369000	1633983	1715676	2959967	3711904
Gain	0.968	0.907	0.968	1.326	0.973	0.937	0.948	0.744	0.971
BW MHz	449	313	572	37	241	20	120	4	337
Rin Ω	30.695k	1E+20	1E+20	32.154k	31.548k	354.341k	316.68k	3.405M	36.441k
Rout Ω	972	2.74k	1.029k	2.891k	1.818k	13.601k	2.911k	128.568k	842
Power mW	1.67	1.66	1.658	1.308	1.516	1.642	1.485	1.317	1.721
Offset mV	3.78	25.2	−301	376	16.9	failed	34.7	failed	8.66
SettlingT ns	2.76	8.4	2.83	15.7	7.55	25.3	8.36	3.71	3.44
SlewRate $\frac{V}{\mu s}$	410	450	1700	86	180	350	6100	failed	4300
Dynamic Range V	−0.517 to 0.594	−0.632 to 0.499	−0.339 to 0.899	−0.907 to 0.374	−0.655 to 0.516	−0.605 to 0.630	−0.652 to 0.505	0.374 to 0.683	−0.641 to 0.543
Noise $\frac{\mu V}{\sqrt{Hz}}$	175.508	289.837	200	218.59	214.183	773.65	390.907	3247.8	204.607

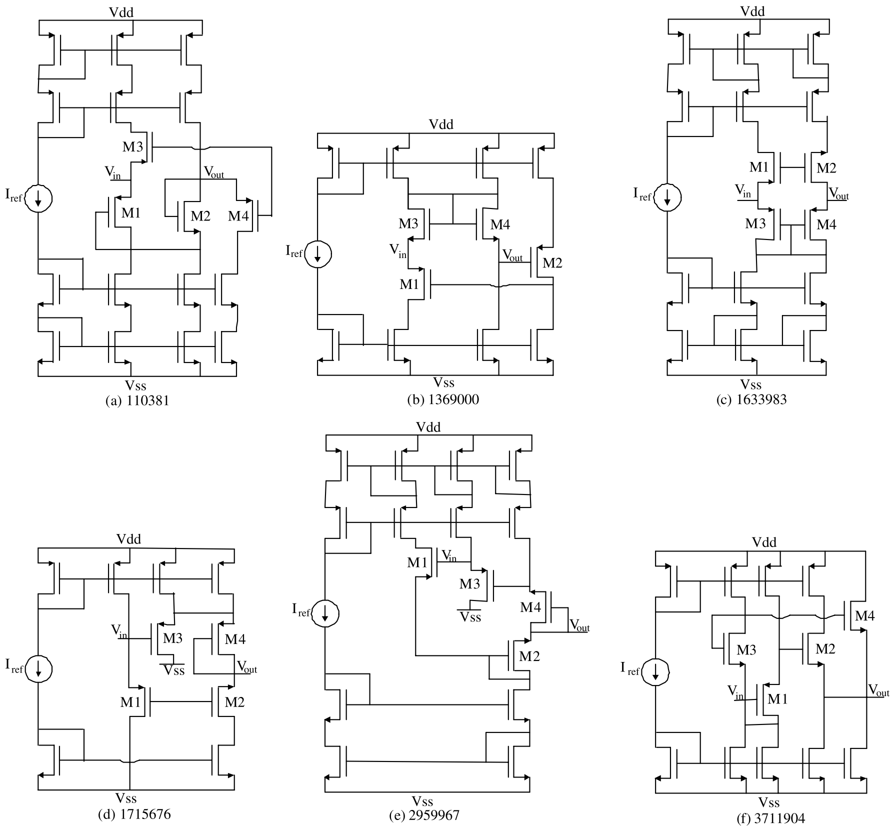

Fig. 8 Six new VFs synthesized from Fig. 1(c)

for all N-MOSFETs and 50 for all P-MOSFETs. By setting $k1 = 0.65$ and $k2 = 0.74$ the best VF is the individual 560828.

The behavior of the useful VFs can be optimized for high-frequency applications using the method introduced in [8, 19], and in noise by applying the method given in [9]. Most important is the fact that the VFs can be evolved to design VMs. When the GA is forced to synthesize VMs using the VFs in Fig. 6 and Fig. 8, the SPICE simulation results using the description from Fig. 4(a) are shown in Table 5. In this case, $(W/L) = 54$ for MINV1 and $(W/L) = 418$ for MINV2, with $L = 1.4$ μm, but now the Fitness 1 and 2 given by (3) and (4) are modified to $V_o < k1 \times V_i$ and $V_o < k2 \times V_i$, respectively. Therefore, $k1 = -0.7$ and $k2 = -0.94$. From Table 5, the practical VMs are the individuals embedding the VFs 560828, 2241512, 110381, 1369000, 1715676 and 3711904. All these six VMs improved BW, Rin, Rout and noise, so that the better VMs embed the VFs 1715676 and 3711904, and since from Table 4 the individual 2959967 has bad SPICE characteristics, it is not suitable to evolve to a VM. Most importantly, as introduced in Sect. 1, the VFs and VMs can be evolved to design practical CCs, like the ones synthesized in [1], by applying GAs.

Table 5 SPICE simulation results for the VMs from Fig. 4(a)

Embedded VF Chromosome	560828	2241512	2794892	110381	1369000	1633983	1715676	2959967	3711904
Gain	−0.940	−0.970	−0.889	−1.01	−0.978	−0.968	−0.986	−0.209μ	−0.963
BW MHz	571	566	560	295	438	28	498	failed	646
Rin Ω	1E+20	1E+20	1E+20	1E+20	1E+20	1E+20	1E+20	1E+20	1E+20
Rout Ω	57.9	89.3	148	356	332	3286	128	2061	42.2
Power mW	10.628	10.656	10.203	10.413	10.364	10.62	10.325	3.088	10.722
Offset mV	−0.193	−0.193	−0.182	−0.206	−0.169	−0.192	−0.164	failed	−0.198
SettlingT ns	16.8	11.2	9.4	25.2	11	8.7	13.4	failed	7.21
SlewRate $\frac{V}{\mu s}$	65	130	55	49	100	200	90	failed	190
Dynamic Range V	−0.583 to 0.480	−0.667 to 0.456	−0.459 to 0.498	−0.819 to 0.533	−0.667 to 0.441	−0.776 to 0.508	−0.662 to 0.511	0.408 to 0.591	−0.672 to 0.477
Noise $\frac{\mu V}{\sqrt{Hz}}$	111.11	112.481	123.087	81.392	92.348	339.789	113.441	110640	125.47

From the characteristics shown in Table 4, the ordering from the best to the worst synthesized VF is: 560828, 3711904, 2794892, 2241512, 1369000, 1715676, and 110381. They can be used to design CCs [2, 19], and input stages for CFOAs [12]. In fact, in [12] the VFs 560828 and 2794892, shown in Fig. 6(a) and (c), were used in its bipolar version. Finally, from the characteristics shown in Table 5, the ordering from the best to the worst synthesized VM embeds the VFs: 3711904, 1715676, 1369000, 560828, 2241512, 2794892, and 110381. They can be used, e.g., to design novel ICCs [29].

5 Conclusions

An automatic system has been introduced to synthesize VFs and VMs by GAs. The system was programmed in MATLAB, and it interfaces with SPICE to evaluate the behavior of the VFs and VMs by using standard CMOS technology of 0.35 μm. The main contribution is the introduction of a new genetic representation of unity-gain cells (VFs and VMs, for instance), using the ideal properties of the nullator (O) and norator (P). In this manner, a CMOS VF topology was codified by using four kinds of genes: genSS, genSMos, genBias and genCM, as shown by (1). Furthermore, a CMOS VM topology was codified by augmenting the length of (1) by one bit associated to genInv, as described by (2). The proposed GA evaluates three fitness functions: valid topologies, valid biased topologies using (3), and valid CMOS topologies using (4). At each evaluation a new population may be created, but the system finishes its search process when a CMOS VF accomplishes the third fitness, i.e. when $V_o < k \times V_i$ for VFs, and $V_o < k \times V_i$ for VMs, where k can be provided by the user. Three known VFs were synthesized and six new VFs were created. The characteristics of the nine VFs were computed using SPICE. The VFs were evolved to synthesize VMs, so that practical VM topologies were derived. Finally, from the results provided in Tables 4 and 5, one can decide on the suitability of the proposed GA to synthesize VFs and VMs, which are practical for analog signal processing applications.

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