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A Canonical Voltage-Controlled VM-APS with a Grounded Capacitor

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Abstract A new canonical first order voltage-mode all-pass section (VM-APS) employing a single grounded capacitor as the only passive element and two differential voltage current conveyors as the active elements is proposed. The circuit, with its attractive features of resistorless realization, voltage-controlled pole frequency and low impedance voltage output is a novel and unique offering to the field and an addition to the rich literature on the subject. PSPICE simulations are carried out in 0.5 μ CMOS technology to validate the utility of the proposed circuit.

Keywords All-pass filters · Voltage-mode · Analog signal processing · Tunable circuits

1 Introduction

First order all-pass sections (APSs) are one of the important analog signal processing circuits which have been extensively researched in the technical literature due to their numerous applications in communication and instrumentation systems [1, 3, 5–10, 12, 13, 15]. Most of the recent research on the subject has focused on one or more of the following advantageous features:

(i) Use of a single active element ([1, 7–9], three circuits of [13]).
(ii) Use of a minimum number of passive elements [6–9].
(iii) Employment of a grounded capacitor [6, 10, 13].
(iv) A canonical structure ([6–10], one circuit of [13]).
(v) No matching condition requirements [6, 7, 10].

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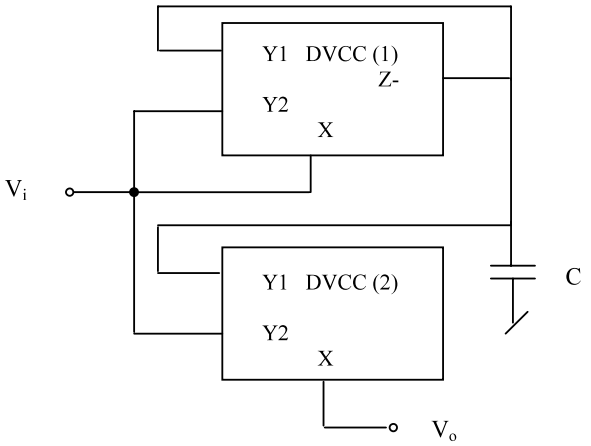

Fig. 1 Proposed resistorless canonical voltage-controlled VM-APS

(vi) Tunable circuit realization [9, 12].
(vii) Resistorless circuit [9, 12].

Note that none of the reported circuits fulfills more than four or five (in one case) of the above listed seven features. This paper presents a new first order VM-APS which caters to six of the above listed features. The new circuit with two active elements exhibits all the features listed from (ii) to (vii), thus offering a novel and unique addition to the field and to the rich literature on the subject [1, 5–13, 15]. When compared to the two active element based tunable circuit realizations [9, 12], the new circuit is canonical (unlike [12]) and uses a grounded capacitor (unlike [9, 12]). A non-ideal analysis of the circuit is also given. The proposed circuit is verified through simulations using real device CMOS parameters.

2 Proposed Circuit

2.1 Ideal Analysis

The new voltage-controlled canonical APS with a single grounded capacitor as the only passive element employing two differential voltage current conveyors is shown in Fig. 1. A differential voltage current conveyor (DVCC) was first introduced by Pal [14] and further developed by Elwan and Soliman [2]. An early application of the active element was reported by Gupta and Senani [4]. A DVCC with only a Z− output is characterized by the following equation:

$$V_X = V_{Y_1} - V_{Y_2}, \qquad I_{Z-} = -I_X, \qquad I_{Y_1} = I_{Y_2} = 0, \tag{1}$$

where the suffixes refer to the respective terminals. The difference of the Y_1 and Y_2 terminal voltages is conveyed to the X terminal; the current inputted at the X terminal is conveyed to the Z− terminal with inverse polarity (for the Z+ terminal, the polarity remains the same). In fact, a DVCC is only an extension of a second generation current conveyor (CCII) with differential input capability. The DVCC is characterized by

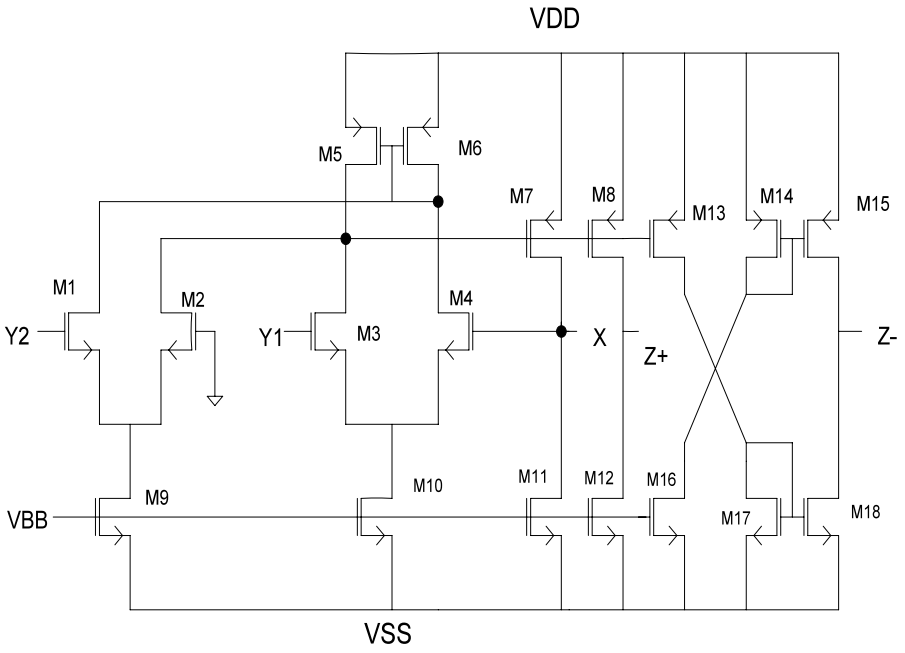

Fig. 2 DVCC implementation

high input resistance at the Y_1 and Y_2 terminals, high output resistance at the Z+ and Z− terminals and a low resistance at the X terminal. The CMOS implementation of the DVCC [2] is shown in Fig. 2. The X terminal resistance is actually dependent on the biasing voltage V_{BB} and shows moderate variation with it. Keeping this in consideration, the ports Y to X relationship is modified to $V_X = (V_{Y_1} - V_{Y_2}) + I_X R_X$. This property is actually utilized in the proposed APS. The circuit of Fig. 1 is analyzed for its transfer functions as given below:

$$\frac{V_o}{V_i} = -\frac{s - 1/R_X C}{s + 1/R_X C}. \tag{2}$$

Equation (2) is the standard voltage transfer function for a first order all-pass filter with unity gain and frequency dependent phase $\Phi = -2\tan^{-1}(\omega R_X C)$. Here, R_X is the X terminal resistance which depends on the biasing voltage V_{BB}. Note that the proposed circuit uses a single capacitor in grounded form, which is ideal for integration in MOS technology. Moreover no resistor is required, which also favors microminiaturization. The pole frequency of the APS ($\omega_o = 1/R_X C$) is controllable through bias voltage V_{BB}. This feature is also a desirable one for the circuit's feasibility in IC form. The circuit possesses low output resistance as the output is at the X terminal, which shows a low resistance for practical values of V_{BB}, as will be evident during the simulations. Another feature to be noted is that DVCC(2) has unused Z terminals. Therefore, these stages need not be implemented when integrating the circuit.

2.2 Non-Ideal Analysis

The non-ideal DVCC (with only Z− output) is characterized by the following relationship:

$$\beta_1 V_{Y_1} - \beta_2 V_{Y_2} = V_X, \qquad I_{Y_1} = I_{Y_2} = 0, \qquad I_{Z-} = -\alpha I_X, \tag{3}$$

where $\beta_i,\ i = 1, 2$ is the voltage transfer gain from Y_1 and Y_2 to the X terminal of the DVCC and α is the current transfer gain of the DVCC from the X to the Z− terminal. These transfer gains differ from unity by the voltage and current tracking errors of the DVCC. More specifically, $\alpha = (1 - \delta)$ and $\beta = (1 - \varepsilon)$, where δ is the current transfer error (tracking error) of the DVCC and ε is the voltage transfer error (tracking error) of the DVCC. Analysis of the circuit using this description yields the following voltage transfer function:

$$\frac{V_o}{V_i} = -\beta_{22} \frac{s - \alpha[(1 + \beta_{12})\frac{\beta_{21}}{\beta_{22}} - \beta_{11}]\frac{1}{R_X C}}{s + \alpha\beta_{11}\frac{1}{R_X C}}. \tag{4}$$

Here, α is the current transfer gain from the X to the Z− terminal of DVCC(1), β_{11} is the voltage transfer gain from Y_1 to X of DVCC(1), β_{12} is the voltage transfer gain from Y_2 to X of DVCC(1), β_{21} is the voltage transfer gain from Y_1 to X of DVCC(2), and β_{22} is the gain from Y_2 to X of DVCC(2). It is easily verified that for the ideal case these gains are unity and (4) reduces to the ideal (2). However, the non-idealities do affect the filter gain as it now depends on β_{22}. Similarly, the pole frequency is also affected as it now becomes $\omega_o = \alpha\beta_{11}/R_X C$. The sensitivity analysis shows that the sensitivity of the pole frequency to the non-idealities is unity in magnitude, thus ensuring a good sensitivity performance. It is further noted that the voltage and current transfer gains are unity up to high frequencies, determined by the process parameters and the technology used, and thereafter show a first order roll-off. These gains have thus been taken as real for working frequencies.

2.3 Effect of R_X of DVCC(2)

The proposed circuit utilizes the controllable nature of R_X of DVCC(1). But the same R_X of DVCC(2) may pose deviations in the circuit characteristics. Since the output is at the X terminal of DVCC(2), the output may actually change on loading. But for loads ($R_L \gg R_X$), the deviation is very negligible. It is evident from the circuit that the output would be given by the following relationship on connecting a load (R_L):

$$V_{output} = [R_L/(R_{X_2} + R_L)]V_o, \tag{5}$$

where R_{X_2} is the output resistance of the X terminal of DVCC(2) and V_o is the output as shown in Fig. 1. Equation (5) clearly shows that the deviation would occur only for small loads, as R_{X_2} is quite small.

Table 1 0.5 μ CMOS parameters used in simulation

NMOS :

LEVEL = 3 UO = 460.5 TOX = 1.0E-8 TPG = 1 VTO = 0.62 JS = 1.8E-6 XJ = 0.15E-6 RS = 417 RSH = 2.73 LD = 0.04E-6 ETA = 0 VMAX = 130E3 NSUB = 1.71E17 PB = 0.761 PHI = 0.905 THETA = 0.129 GAMMA = 0.69 KAPPA = 0.1 AF = 1 WD = 0.11E-6 CJ = 76.4E-5 MJ = 0.357 CJSW = 5.68E-10 MJSW = 0.302 CGSO = 1.38E-10 CGDO = 1.38E-10 CGBO = 3.45E-10 KF = 3.07E-28 DELTA = 0.42 NFS = 1.2E11

PMOS:

LEVEL = 3 UO = 100 TOX = 1.0E-8 TPG = 1 VTO = −0.58 JS = 0.38E-6 XJ = 0.1E-6 RS = 866 RSH = 1.81 LD = 0.03E-6 ETA = 0 VMAX = 113E3 NSUB = 2.08E17 PB = 0.991 PHI = 0.905 THETA = 0.120 GAMMA = 0.76 KAPPA = 2 AF = 1 WD = 0.14E-6 CJ = 85E-5 MJ = 0.429 CJSW = 4.67E-10 MJSW = 0.631 CGSO = 1.38E-10 CGDO = 1.38E-10 CGBO = 3.45E-10 KF = 1.08E-29 DELTA = 0.81 NFS = 0.52E11

Table 2 Device dimensions used

Transistors	W (μm)	L (μm)
M1, M2, M3, M4	0.8	0.5
M5, M6	4	0.5
M9, M10	14.4	0.5
M7, M8, M13, M14, M15	10	0.5
M11, M12, M16, M17, M18	45	0.5

3 Simulation Results

The proposed VM-APS was simulated using the 0.5 μ CMOS parameters listed in Table 1 and device dimensions as listed in Table 2. The supply voltage used was ±2.5 V. First, the R_X variation with the bias voltage V_{BB} was studied. The results are shown in Fig. 3, which suggests a moderate variation of R_X with V_{BB}. The APS circuit of Fig. 1 was next designed with $C = 10$ nF, and $V_{BB} = -1.5$ V. The gain and phase plots are shown in Fig. 4, where a pole frequency of 200 kHz is obtained. This is close to the theoretical value of 196 kHz as obtained from the R_X value from Fig. 3. Next the circuit is inputted with a sinusoidal signal of 200 KHz; the input and −90° phase-shifted outputs are shown in Fig. 5. Next, the pole frequency control through the bias voltage (V_{BB}) is shown in Fig. 6. The pole frequency is found to vary over a wide range with V_{BB}. This further confirms the practical utility of the proposed circuit. Further, the effect of R_{X_2} on the circuit performance is studied by connecting a load R_L to the circuit. The results for three values of R_L (1, 10 and 100 kΩ) are shown on the same plot, in the form of the output wave shapes, in Fig. 7. The three wave shapes are in very small deviation, thus justifying the discussion of Sect. 2.3. The DC transfer characteristic of the proposed circuit is shown in Fig. 8, where good linearity and symmetry are found from −0.5 to 0.5 V.

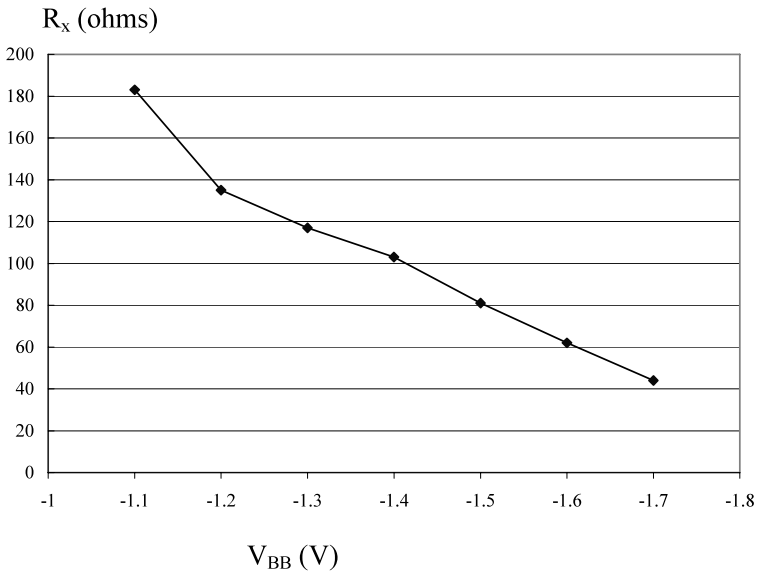

Fig. 3 R_X variation with bias voltage V_{BB}

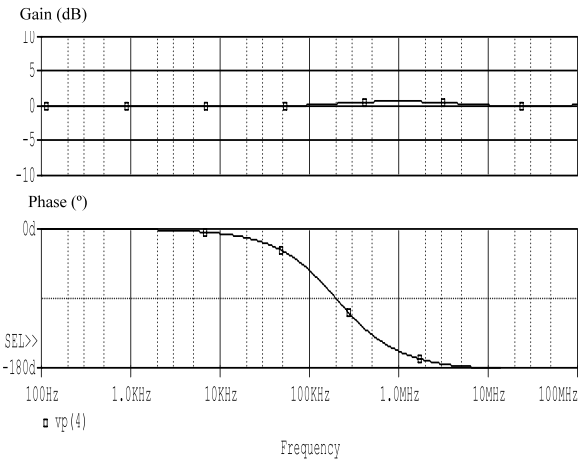

Fig. 4 Gain (in dB) and phase (in deg) plots for the proposed circuit

4 Typical Applications and a New One

First order all-pass filters have found many applications. One such application is as a phase shifter, as discussed previously. Such a circuit (phase shifter) finds numerous applications in communication systems. The APSs have application in phase equalization as well. Other possible applications are in realizing multiphase sinusoidal oscillators [3] and quadrature oscillators [9, 11]. Here, a new application of the proposed APS in clock generation is given, where by using additional DVCCs, a four phase clock is generated. The circuit schematic is shown in Fig. 9. The input

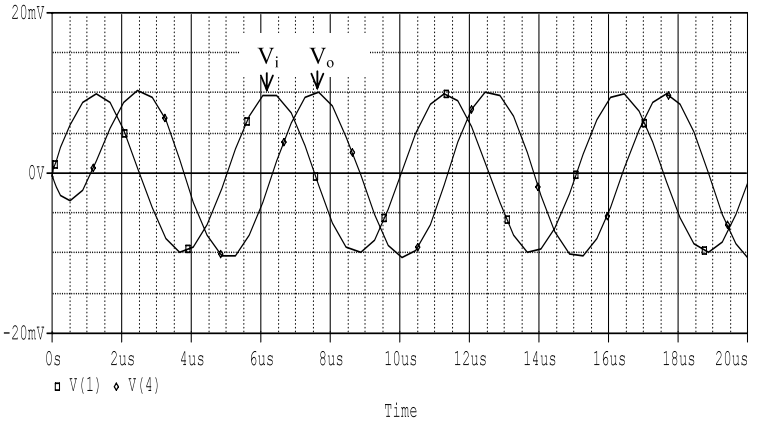

Fig. 5 Input and output waveforms for the circuit at 200 kHz

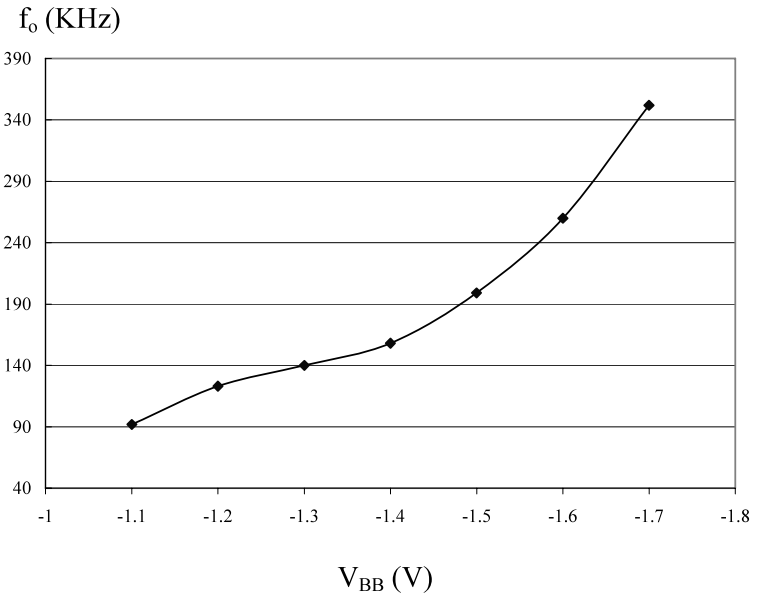

Fig. 6 Pole frequency variation with the bias voltage V_{BB}

and the phase-shifted output of the APS is passed through DVCC(3) and DVCC(4), which work as a saturated amplifier or simply a comparator. The gain of the amplifiers (DVCC(3) and DVCC(4)) is R_Z/R_X, where R_X is the X terminal resistance and R_Z is the Z terminal resistance of the DVCCs. Note that the Z terminals exhibit a high output resistance, sufficient to saturate the amplifier. The output levels depend on the supply voltage (V_{DD} and V_{SS}). No additional resistors are being used, thus the new scheme is compatible with monolithic implementation. The four clock outputs generated are at a progressive phase shift of 90°. To verify this, the APS was used

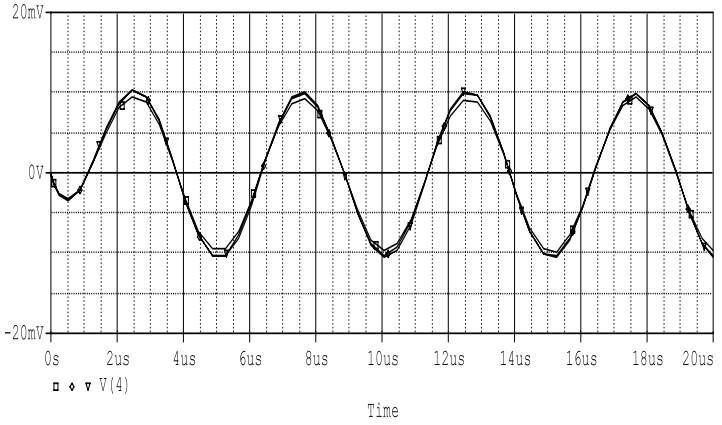

Fig. 7 Output waveforms for varying load (R_L)

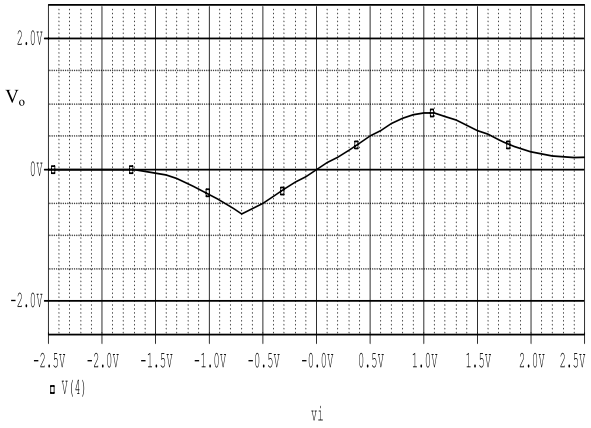

Fig. 8 DC transfer characteristic of proposed circuit

with the same design as given earlier. DVCC(3) and DVCC(4) both had Z+ and Z− output stages, so as to generate four phases. The results are shown in Fig. 10 and very well justify this new application. The clock frequency is 200 kHz, which is consistent with our preceding results for the APS. The outputs can also be made unidirectional by employing appropriate clipper or rectifier circuits. The phase difference between the wave shapes can be varied by controlling the bias voltage (V_{BB}) of the APS.

5 Conclusion

This paper presents a new voltage mode first order all-pass filter with several desirable features: use of a grounded capacitor as the only passive element, resistorless realization, low output impedance, voltage-controllable pole frequency, and compatibility with CMOS implementation. The new circuit is a unique addition to the field

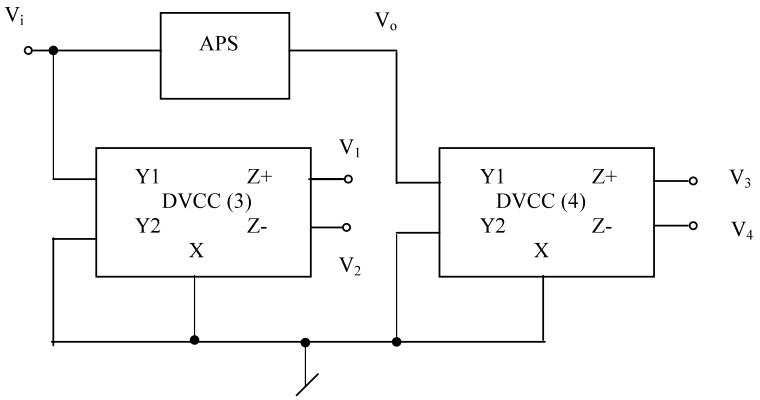

Fig. 9 Application of APS in 4-phase clock generation

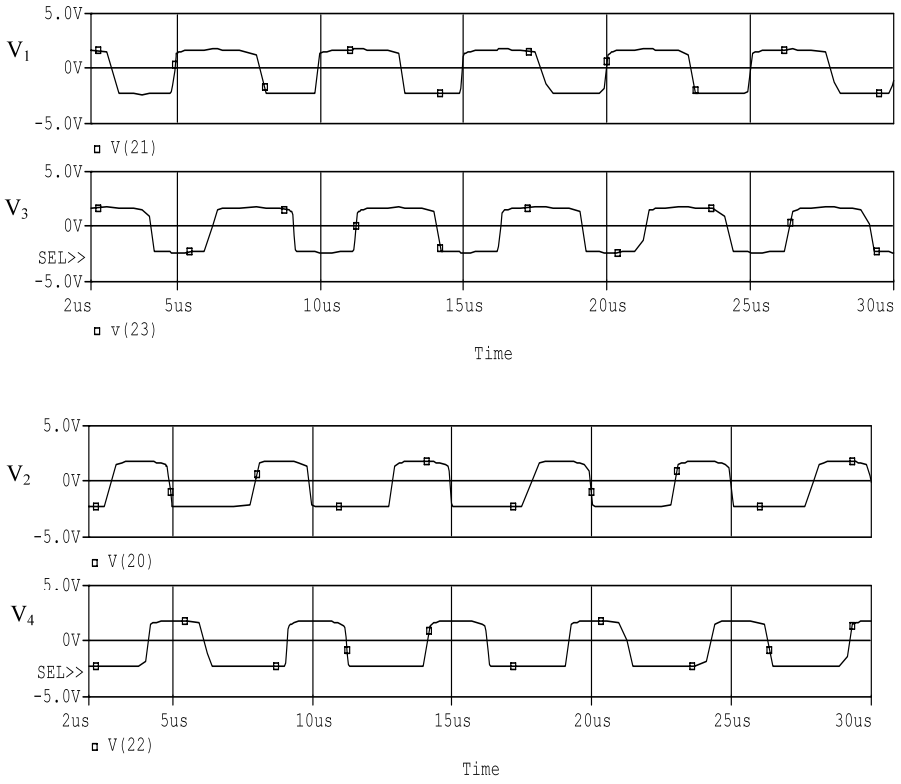

Fig. 10 4-phase clock wave shapes at 0.2 MHz of Fig. 9

with its already vast literature [1, 5–13, 15]. PSPICE simulation results are included to verify the proposed circuit. A new application in four phase clock generation is also given.

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