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DEEP LEVEL TRANSIENT SPECTROSCOPY TECHNIQUES AND SYSTEMS

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We briefly review the physical background on which Deep Level Transient Spectroscopy is based and we present the basic design and operation principles of a high performance and low cost microcomputer based DLTS system. Detailed examples are given of the system's use in the study of platinum silicides methods of preparation and in the study of defects in MOCVD grown $Al_xGa_{1-x}As$.

Introduction

It is common knowledge that crystal periodicity defects give rise to localized electronic states in semiconductor materials that are situated at more or less deep levels inside the gap. Such defects are important for the quality and reliability of the various electronic and optoelectronic devices. A sensitive and reliable method for determining the various deep level parameters (activation energy, capture cross-section, etc.) is Deep Level Transient Spectroscopy (DLTS) introduced by Lang [1]. In the following we review briefly the theoretical principles on which the method is based and thereafter we describe a microcomputer based DLTS system of high performance and very low cost. Closing we present as examples of the system capabilities and performance our latest results on two different research projects; the first one aiming at the study of Pt-silicides prepared by rapid thermal annealing (RTA) and the second one aiming at the study of deep levels in $Al_xGa_{1-x}As$ grown by MOCVD.

Theory

Deep Level Transient Spectroscopy consists in observing how the population of a thermally (or optically) stimulated centre inside the semiconductor energy gap returns to equilibrium after being excited. Son one has to study the capacitance transient responses of the experimental device, which usually is a Schottky diode or a strongly asymmetrical p^+-n or n^+-p junction. A train of repetitive pulses applied on a reverse biased junction permits the deep levels to be filled with carriers which are consequently thermally released giving rise to an exponential (in principle) capacitance transient. The DLTS signal is the difference between the transient

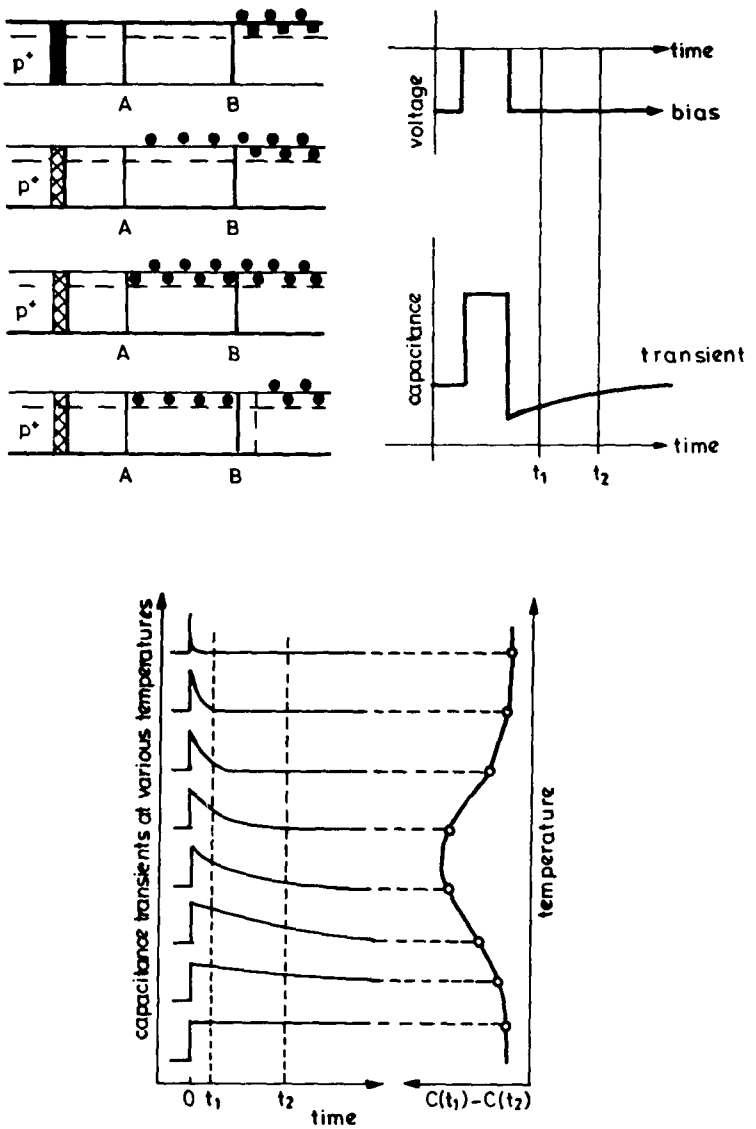

Fig. 1. Schematic presentation of the DLTS peak formation principle

amplitude at two sampling times preselected; as shown in Fig. 1 during a thermal scan there appears one peak for each trap level detected.

The basic idea of the method is the rate window concept; this rate window can be expressed in terms of the transient emission rate giving rise to the maximum

DLTS signal output, namely

$$e_{\max} = \ln(t_2/t_1)/(t_2 - t_1), \tag{1}$$

where $e_{\max}$ is the emission rate of the transient and t_1, t_2 are the preselected sampling times. The more different the sampling times t_1 and t_2 are the more accurate the emission rate estimation is.

The relation between the emission rate and the activation energy ΔE is

$$e_{\max} = (\sigma\langle v\rangle N/g) \cdot \exp(-\Delta E/kT) = A \cdot T^2 \cdot \exp(-\Delta E/kT), \tag{2}$$

where $\langle v\rangle$ is the mean thermal velocity of carriers, g is the degeneracy factor, k is the Boltzmann constant, T is the temperature, N is the effective density of states, σ is the capture cross-section and A is a temperature independent constant.

According to relations (1) and (2) the activation energy can be obtained from the slope and the capture cross-section from the intercept of an Arrhenius plot.

The trap concentration N_T can be determined by

$$N_T = 2\Delta C(0) \cdot [N_D - N_A]/C(N), \tag{3}$$

where $C(N)$ is the capacitance of the reverse-biased diode, $\Delta C(0)$ is the difference between the capacitance after the pulse $C(0)$ and the static capacitance $C(N)$, while N_D and N_A are the donor and acceptor concentrations, respectively. In relation (3) one assumes $C(N) \gg \Delta C(0)$, uniform doping and a step-junction.

From the above relations varying according to the signals applied to the junction it is also possible to determine the spatial distribution across the junction and the activation energy dependence on the electric field strength of the traps.

System description

The major disadvantage of the DLTS method is the long time needed for a single spectrum in relation to the big number of spectra necessary for a reliable determination of the trap parameters. It very soon became obvious that automatization would help towards decreasing the time necessary for and improving the reliability of defects characterization. So in the early eighties there started appearing in the market and the literature a number of microcomputer assisted systems [2, 3]. Some of these systems are already rather old while others make extensive use of highly sophisticated and not commercially available circuits. Two years ago we have designed and constructed a simple, low cost, and good performance system [4].

Design principles

The structure of the system is shown in Fig. 2. The whole set-up consists of (1) the measuring system and (2) the microcomputer that controls the measuring system and collects the data.

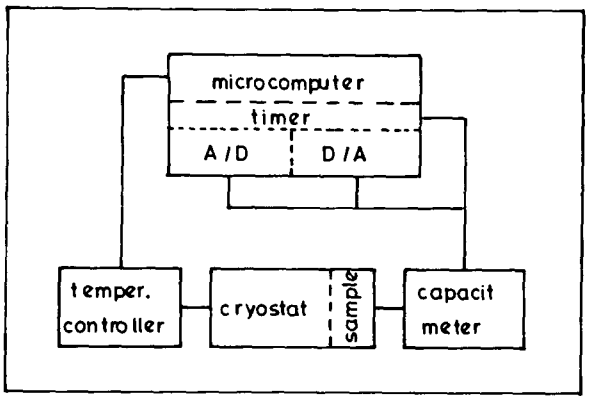

Fig. 2. Block diagram of the microcomputer based DLTS system

The measuring system consists of: (a) A cryostat; an Oxfords DN1754 liquid nitrogen cryostat running with an Oxfords ITC-4 temperature controller and permitting temperature scans in the range 80–500 K; (b) A capacitance meter; the very familiar to the kind of measurements Boonton 72B.

The control system consists of an IBM PC/XT Compatible Microcomputer, with its well-known advantages, and an add-on card (SMM-PCL714). We have avoided the use of home-made circuits or interfaces in order to make the system easily installable in Laboratories without experimental technical support. With no change in the hardware the system is capable of carrying out various modes of DLTS measurements and also of performing C–V, dC/dV–V, C–T and Transient Digitizing Measurements.

The software is organized in logical blocks that can be activated in various sequences. The data handling and evaluation is not part of the main program permitting greater flexibility. The system is capable of continuous upgrading without any compatibility problems with the already existing parts; a very attractive feature taking into account the continuous appearance of new add-on cards and software.

Software description

For simplicity the software developed is written in Basic although a number of subroutines are written in Assembly to minimize the time necessary for each measurement. Its main routines are:

C–V routines: The standard routine permits the estimation of the $C = f(V)$ function in the 0.0 V to 10.0 V reverse bias range typically in less than 10 s. That

makes C–V measurements possible at various temperatures during a continuous temperature scan. A second routine permits the estimation of the function $dC/dV = f(V)$ in the same region. Both routines give the option of using an external bias source.

DLTS and C–T routines: The program for the DLTS spectra is divided in two main sections; the junction pulsing and data collection section and the input/change of measurement parameters section. The whole procedure for data collection follows the routine: The timer triggers the DAC's to provide the appropriate train of pulses. It also triggers the ADC to read the capacitance values at the preselected times. This measuring cycle is repeated to reduce noise and an average capacitance value for each preselected time is stored. Just before and after this cycle the temperature is recorded and the main value is also stored. Operation is repeated for the next pulse and the whole procedure continues until the end of the temperature scan. The program permits the user a direct and independent estimation of all measuring parameters for all the twelve possible pulses that can be applied to the junction during one temperature scan. Data collected are stored as a spreadsheet. Typical time necessary for a temperature scan between 80 K and 300 K is 50 min (temperature step 0.5 K, pulse period 10 ms and 500 repetitive measurements) varying with the pulse and sampling parameters. Data for the C–T characteristic can be collected either independently or during the DLTS temperature scan.

Digital analysis of a transient: A major problem in the DLTS technique is the possible existence of temperature gradients between the sample and the temperature measuring element. As a method giving more accurate results the Constant Temperature Capacitance Transient Analysis has been proposed being more efficient for single-exponential transients. The system collects data permitting the analysis of the capacitance transient in 16 different temperatures and for a typical digitizing step of 100 μs that can be reduced down to 10 μs.

The software package is contained in a floppy diskette and it is readily available with the corresponding user's manual to anyone. Continuing we present briefly results of two different projects in which the system described has been used for electrical characterization measurements.

Silicides project

Thin-film silicides are important in integrated circuits technology an platinum silicide has shown very promising properties in low-ohmic or high-barrier Schottky contacts in MOS and bipolar devices. Silicides are usually formed by conventional furnace annealing (CFA), and the preparation procedure is the subject of a continuous study. Independent of silicon substrate, doping type, Pt deposition technique, etc. the reaction between Pt and Si proceeds first forming Pt_2Si and then PtSi. Oxygen ambient can cause the formation of an oxide layer under the surface of platinum, inhibiting the complete reaction between the Pt and Si.

Recently Rapid Thermal Annealing (RTA) techniques have been used for silicidation of Pt films on polysilicon or single-crystal Si substrates. The advantages

of the RTA technique are shorter processing times and lower contamination in respect to CFA: the presence of oxygen in the ambient does not prevent the silicide formation. We have studied [5] the morphology of the platinum and iron silicide layers formed by RTA and CFA and the formation of electrically active defects in the Si substrate using X-Ray Diffraction, Scanning and Transmission Electron Microscopy (SEM-TEM) and Electrical Characterization Measurements. The PtSi/Si diodes prepared by RTA have shown an overall better performance.

Samples were prepared by electron beam deposition of 80 nm thick films on ⟨100⟩-oriented n-type Si with a doping concentration of about 2×10^{16} cm^{-3}. After the film deposition platinum silicides were formed by annealing the samples at various temperatures. With CFA the samples were annealed at a temperature varying from 350 to 550 °C for 30 min. RTA was carried out at 350 °C and 550 °C for 30 s.

Low-angle X-Ray Diffraction (XRD) data obtained from samples annealed by CFA and RTA have shown an incomplete reaction between Pt and Si in the case of CFA. The annealing process leaves an appreciable amount of unreacted Pt in the silicide films. In the case of RTA the spectrum shows only peaks which correspond to PtSi indicating a complete consumption of the Pt for silicide formation.

Transmission and Scanning Electron Microscopy techniques have been employed to investigate the PtSi films formed. In both cases we have observed more or less the same morphology. For CFA a large number of intense rings is observed indicating the existence of an appreciable amount of uncreacted Pt layers above the silicide film, while for the sample annealed by RTA few weak rings are observed indicating a small amount of unreacted Pt.

Electrical Characterization measurements on the samples, performed by the system described, have proved that for the as-deposited Schottky contacts the donor concentration obtained from the $1/C^2$ vs V plots agrees with the donor concentration $N_d = 2 \times 10^{16}$ cm^{-3} of the Si substrate. After thermal treatment by RTA the donor concentration obtained (1×10^{16} cm^{-3}) is about the same indicating that no deep levels of high concentration are introduced in the Si substrate after silicidation by RTA. For the CFA treated samples $1/C^2$ vs V plots show a decreasing donor concentration down to 4×10^{15} cm^{-3}. This decrease can be explained by the presence of acceptor-like interface states extending rather deeply towards the semiconductor bulk.

DLTS measurements on Pt/n-Si contacts, as-deposited or annealed by RTA, have failed to detect any trap with concentration over 1×10^{12} cm^{-3}, which is the low-limiting detection sensitivity of our experimental setup. These results indicate that silicidation by RTA does not introduce deep levels in the Si band gap, a conclusion in agreement with our C–V measurements. Figure 3 shows DLTS spectra obtained from Pt/n-Si contacts annealed by CFA at 550 °C. There appears a peak and the corresponding Arrhenius plot is given in Fig. 4. From this plot activation energy and capture cross-section have been estimated equal to $\Delta E = 0.11$ eV and $\sigma = 4.8 \times 10^{18}$ cm^2, respectively. The detected trap level is a new trap since the reported Pt-dominant acceptor levels in n-type Si lie between 0.19 and 0.26 eV. Profiling measurements proved that the detected trap is an "interface trap" since

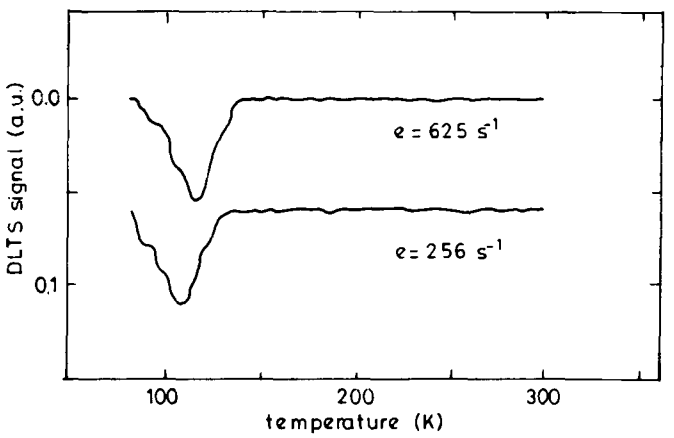

Fig. 3. Typical DLTS spectra for the PtSi/Si interface trap

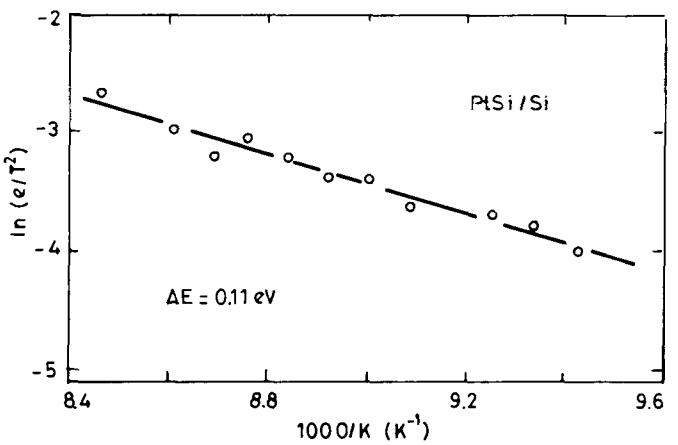

Fig. 4. Arrhenius plot for the PtSi/Si interface trap

its concentration reduces rapidly with depth from the interface with a value equal to $N_t = 2 \times 10^{13}$ cm^{-3} close to the interface. At elevated temperatures Pt diffuses relatively fast in Si via the kick-out mechanism. The concentration of the electrically active Pt in Si after the heat treatment is comparable to the value expected from earlier solid solubility data [6].

$Al_xGa_{1-x}As$ project

$Al_xGa_{1-x}As$ is a very promising new material for optoelectronic devices and it is the subject of an extensive study during the last ten years in respect to all its properties. The task of our project was to investigate the existence and properties of majority carrier traps in Si-doped (10^{16} cm^{-3}) MOCVD grown material. Samples were Au-Schottky diodes. Experiments included mainly C–T and DLTS Measurements. The results are briefly summarized in the following:

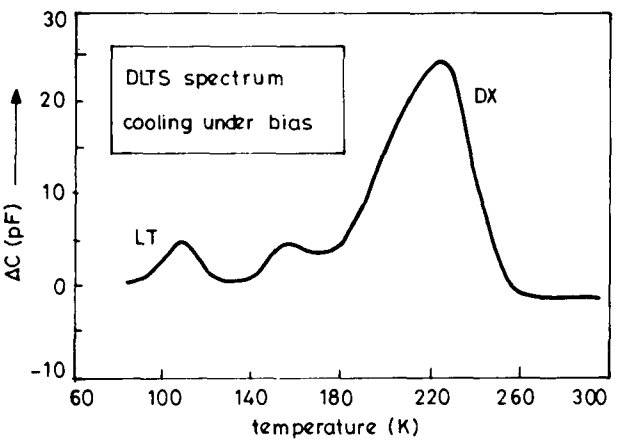

Fig. 5. DLTS spectrum for the Au-$Al_xGa_{1-x}As$ Schottky diodes

a) Conventional DLTS for majority carriers gave the spectrum shown in Fig. 5. The main peak corresponds to the DX centre and the activation energy calculated is 0.47 eV. The closely adjacent peak has an activation energy of 0.39 eV and we believe that corresponds to one of the defects that constitute the DX centre [7]. Our interest focuses on the far left peak which we call LT peak or LT trap.

b) The defect that corresponds to that peak has an activation energy of $\Delta E = 0.22$ eV, a capture cross-section of $\sigma = 2 \cdot 10^{15}$ cm^2 and a concentration of $N_T = 8 \cdot 10^{14}$ cm^{-3}. It is peculiar that the appearance of this peak depends on the conditions of carrying out the DLTS experiment; when the cooling down from 300 K to 90 K was done under no bias the LT peak was not appearing on the spectra, while it was there when the cooling down was done under constant reverse bias. After a series of detailed measurements we have received the group of spectra shown in Fig. 6 where in all cases the sample was cooled down under reverse bias and the bias was interrupted at the temperature indicated. The peak shift of the temperature indicates a field effect dependence of the LT trap activation energy which seems to be consistent with the Poole–Frenkel effect. Far to our knowledge a trap with

similar characteristics has been observed by Wu et al [8] and by Jia et al [9], who also notice a peculiar behaviour in respect to photoexcitation.

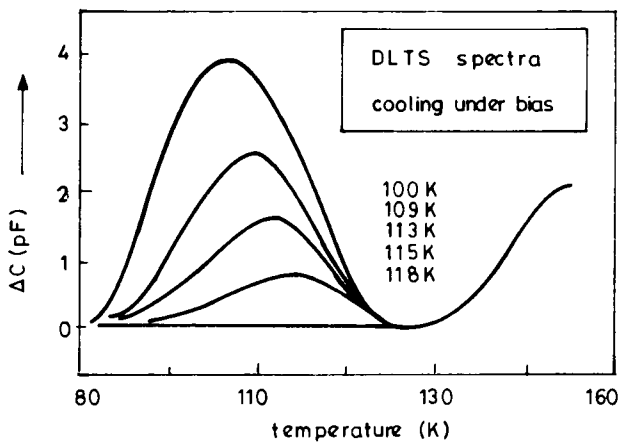

Fig. 6. DLTS spectra; bias interrupted at temperature indicated

In order to give a satisfactory explanation of the LT trap behaviour we reconsidered the DX centre properties attributing to it a major role for this behaviour. The critical feature of the DX centre is its capture cross-section for electrons which is temperature stimulated [10]. As a result at temperatures lower than 110 K the electron capture rate by the DX centre is negligible and begins to increase thereafter. Taking that into account the explanation for the appearance or not of the LT peak goes as follows: At 300 K under zero bias the DX centre is totally empty of electrons because its emission rate at this temperature is extremely high, much higher than the corresponding capture rate. Applying a reverse bias to the junction, e.g. 3 V, we form an additional depletion region in which the DX centres are also empty. When the sample is cooled from 300 K to 90 K under reverse bias the DX centres are staying empty and when the reverse bias is interrupted free electrons are entering the conduction band of the additional depletion region, but the DX centres cannot capture them because their capture cross-section at so low temperatures is extremely low. So there exist enough electrons for the LT trap to be captured and consequently released at higher temperatures giving rise to the LT peak.

If the reverse bias is applied at 300 K and eliminated at e.g. 150 K the free electrons entering the depletion region can be captured by the DX centres, because they have enough energy to overcome the capture barrier. Due to that the availability of free electrons for the LT trap is almost zero, because the DX centres concentration is comparable to the doping concentration. So there exist not enough electrons for the LT trap to be captured and then released to give rise to the LT

peak. This effect holds for all temperatures down to 120 K, which explains the progressive appearance of the LT peak between 108 K and 118 K.

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