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APPLICATION OF COMMERCIAL FIELD-EFFECT TRANSISTORS IN Si(Li) SPECTROMETERS

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The first stage of the charge sensitive preamplifier of the high energy resolution Si(Li) X-ray spectrometers is a cooled junction Field-Effect Transistor (FET) exhibiting low level of noise. The spectrometer manufacturers use selected FET chips mounted into low dielectic loss material. Noise measurements have been performed for selection of low cost commercial FETs of type 2N4416 from different series of Texas Instruments factories. The FETs were encapsulated and mounted into a teflon block. The measurements have been carried out in a high impedance gate mode in time domain. The noise measurement arrangement, the results of selection of FETs and some observations on generation-recombination (GR) noise of FETs are described.

Introduction

For the first stage of the Si(Li) spectrometer application the 2N4416 FET chips have been found most suitable [1], [2]. In order to eliminate the noise of borosilicate glass header spectrometer manufacturers mount the preselected chips into low dielectric loss material into boron nitride or teflon. For the first stage of static or pulsed drain feedback charge sensitive preamplifier commercial FETs are used in our laboratory encapsulated and mounted into a teflon block. The feedback capacitor is also mounted in the same block [3]. The selection of FETs can be carried out in time domain or frequency domain. Detailed analytical and experimental discussion, further their advantages and disadvantages are given by Llacer [4]. The noise of the FETs is influenced by several factors: the geometry of the chip, the number and activitation energy of impurities in gate–channel junction and the quality of the surface of the chip, the material of the capsulation. The noise of the FET strongly depends also on the device working parameters: on drain current, drain voltage, chip temperature and input capaticance. Our measurements have been carried out in high impedance gate mode, as the first stage of a static drain-feedback preamplifier. The working parameters of the FET (the drain current, drain voltage, input capacitance) were chosen close to the working condition in the Si(Li) spectrometer. In order to eliminate the noise of the test Si(Li) detector it was replaced by a cooled teflon capacitor.

The noise measurement configuration

Figure 1 shows the noise measurement configuration. The FET and the charge injector capacitor (C_i) is mounted into a detector cyrostat. The capacitance of C_i is 1.1 pF which value corresponds to the capacitance of a single grooved 20 mm^2 active area 5 mm thick Si(Li) detector at high voltage bias. The noise of the cooled teflon has been found low [5], therefore this arrangement allows to measure the noise of the FET without important additional noise. To keep the microphonics at low level the connecting wires must be short and rigid. The 10^{-5} Pa pressure in the cryostat is maintained by a 1 l/s titanium getter ion pump.

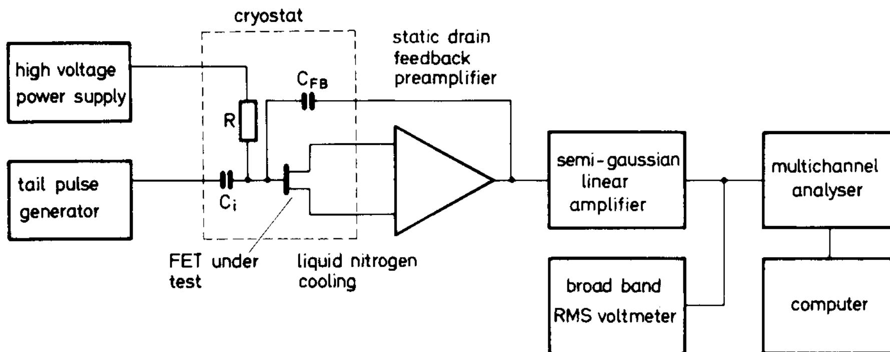

Fig. 1. Schematic diagram of the noise measurement configuration

The temperature of the capacitor and the teflon block without FET power dissipation is 87.5 K. The chip temperature was varied with its selfheating. The drain current was settled with a current generator in the preamplifier and the drain voltage was trimmed with the gate current forced by the high voltage (0–1 kV) connected on the teflon block (R). The noise was filtered with a semi-gaussian linear-amplifier of [9] peaking time constans in the range of 0.46–80 μs. The transfer function of the linear amplifier and its noise indices are [6], [3]:

$$H(p) = \frac{p\left(\frac{p}{\tau} + \frac{9}{4\tau^2}\right)^2}{\left(p + \frac{1}{\tau}\right)\left(p^2 + \frac{9}{4\tau} + \frac{9}{4\tau^2}\right)^2};$$

$$\text{delta noise index: } < N_\Delta^2 > = 1.92/\tau_p,$$

$$\text{step noise index: } < N_s^2 > = 0.98\tau_p$$

$$f^\alpha, \alpha = \pm 1 \text{ noise index: } < N_{-1s}^2 > = 6.81.$$

For the calibration of the system long decay time constant (1000 μs) pulses were fed to the capacitor C_i. The amplitude of pulses measured by the multichannel analyser corresponds to the pulses of energy $E = uC_i\bar{\varepsilon}/q$, where u is the amplitude of the pulses, $\bar{\varepsilon}$ the average energy required to produce one hole–electron pair. The calibration and the measurement of the line width was carried out at 11.8 μs peaking time, for the other peaking time constant settlings, the FWHM were calculated from the RMS voltage readings. The FWHM^2 versus peaking time has the general form of:

$$\mathrm{FWHM}^2 = A\tau_p + B/\tau_p + C + D(2E/\tau_p + \tau_p/2E),$$

where $A = 2.355^2\bar{\varepsilon}^2/q < N_s^2 > I_g$, I_g is the gate current, $B = 2.355^2\bar{\varepsilon}^2/q^2 2kTr_s < N_\Delta^2 > C_{in}^2$, r_s is the equivalent resistance in series with the FET gate, which generates noise equivalent to the white noise in the channel, T is the temperature of the chip, C_{in} is the input capacitance,

$$C = 2.355^2\bar{\varepsilon}^2/q^2 A_\alpha C_{in}^2,$$

where $2A_\alpha$ is the value of the power spectrum of the $1/f$ noise at 1 Hz,

$$D = 2.355^2\bar{\varepsilon}^2/q^2 K_g < N_{GR}^2 > C_{in}^2,$$

where K_g is a proportionality constant for the generation recombination noise, $< N_{GR}^2 >$ is the GR noise index, $E = \tau_g$ is the GR noise generation time.

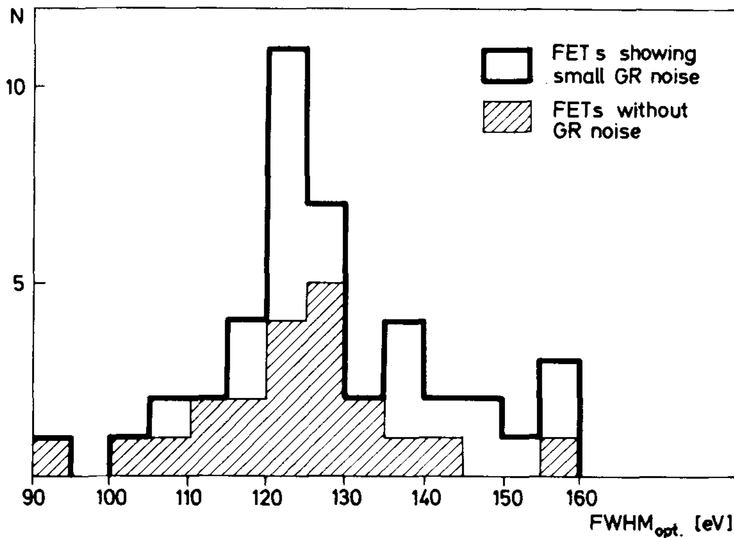

Fig. 2. Distribution of the minimum FWHM of FETs measured at optimum working parameters

140 FETs have been tested. For searching the optimum working parameters of the FETs FWHM versus peaking time curves were measured at different drain currents in the range of 3 mA–9 mA while the drain voltage was kept between 5–7 V. The $A \ldots E$ noise parameters have been calculated using least squares fit.

Results of the measurements

Figure 2 shows the distribution of the minimum FWHM measured at optimum chip dissipation and peaking time. 30% of the FETs exhibited relatively low noise, their minimum FWHM was less than 170 eV, 7% of the FET belonged to the group of FWHM less than 130 eV. 55% of the relatively low noise FETs showed small generation–recombination noise.

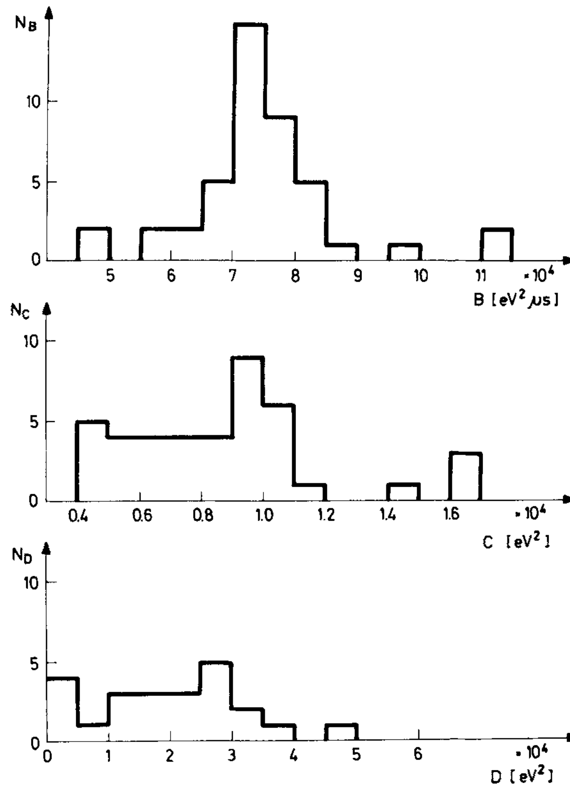

Fig. 3. Distribution of the noise parameters B, C and D of the FETs showing low noise

Figure 3 shows the distribution of the calculated most important noise parameters: B, C and D of the FETs having FWHM less than 170 eV at optimum. In 2 cases the least squares fit gave too low values for $B(< 5000\text{eV}^2)$ because of the fold back of the $\text{FWHM}^2(\tau_p)$ curve at low peaking time constants. The GR noise of FETs is discussed in the next Section.

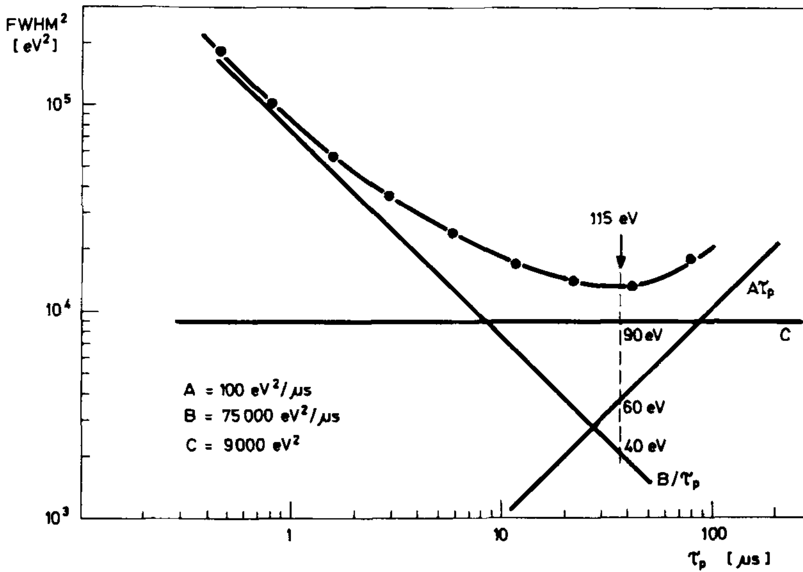

Fig. 4. FWHM^2 versus peaking time and the calculated noise components of a FET without GR noise

Figure 4 shows that the FWHM^2 versus peaking time and the noise components of one of the best FET did not exhibit GR noise. The largest influence on the noise performance of the FET at optimum dissipation and peaking time is made by the f^α noises: 61%, while the contribution of the step noise is 27%, the shot noise is 12%. The values of the noise parameters are: $A = 100\ \text{eV}^2\mu\text{s}$, $B = 7400\ \text{eV}^2\mu\text{s}$, $C = 9000\ \text{eV}^2$.

The generation-recombination noise of the FETs

A great part (84%) of the tested FETs exhibited small or large GR bumps. The typical value for noise parameter D proportional to the number of trap centres in the gate–channel junction is 100 000-200 000 eV^2. In some cases the FWHM versus peaking time curve exhibited a regular figure and it was possible to determine

the activation energy of the GR centres. The measurement of the activation energy (E_{gr}) of the GR centres is based on the variation of the position of the GR bump (parameter E) versus chip temperature: $d(\ln \tau g)/d(l/T) = -E_{gr}/k$, k is the Boltzmann factor [5]. The chip temperature was calculated from the power dissipation of the FET and the thermal resistance of the teflon capsulation and from the zero power temperature of the FET.

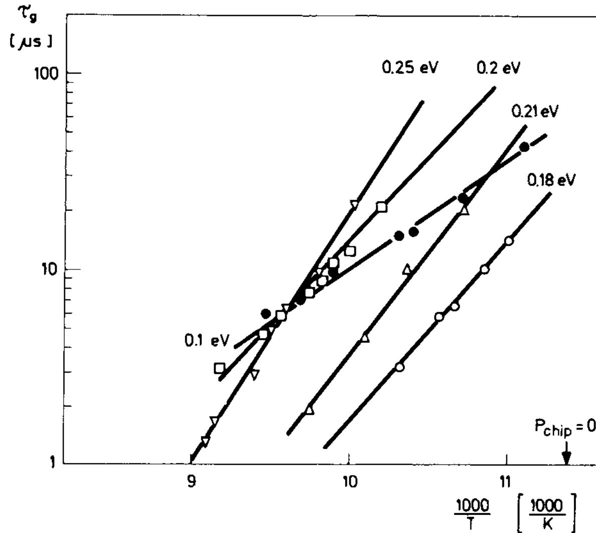

Fig. 5. GR noise generation time versus $1000/T$ of the groups of FETs exhibiting GR noise

Figure 5 shows that five different groups of GR noise were observed. In a series of FETs made before 1980 in the USA, two groups have been found. Most of the FETs exhibiting low noise showed small GR bump. The typical value for parameter D at optimum working parameters is 20000 eV^2. By proper chip temperature the GR bump is shifted to the low peaking time constant, and its contribution at the optimum peaking time is low, about 50 eV. The GR noise of this type is caused by GR centres of activation energy 0.18 eV. Figure 6 shows the FWHM$^2(\tau_p)$ and the noise components of a FET belonging to this group. In this case the value for parameter D is larger than the average, $D = 55000$ eV^2.

FETs from the same series showing poor noise performance (200–500 eV) exhibited frequently large GR bump from GR centres of activation energy 0.1 eV. The typical value for parameter D is 150 000 eV^2 (see Fig. 7). In another series marked E8035, one part of the FETs showed no or very little GR noise, in the other part the activation energies of 0.2 eV and 0.25 eV have been observed. The values

for parameter D were between 20 000 and 50 000 eV^2. Figures 5 and 8 show that in this case the position and the value of parameter D varies strongly with chip temperature. The GR centre levels of 0.18 eV and 0.25 eV were observed earlier by J. Llacer [5], while Hiatt identified activation energy 0.19 eV in specially made transistors [9].

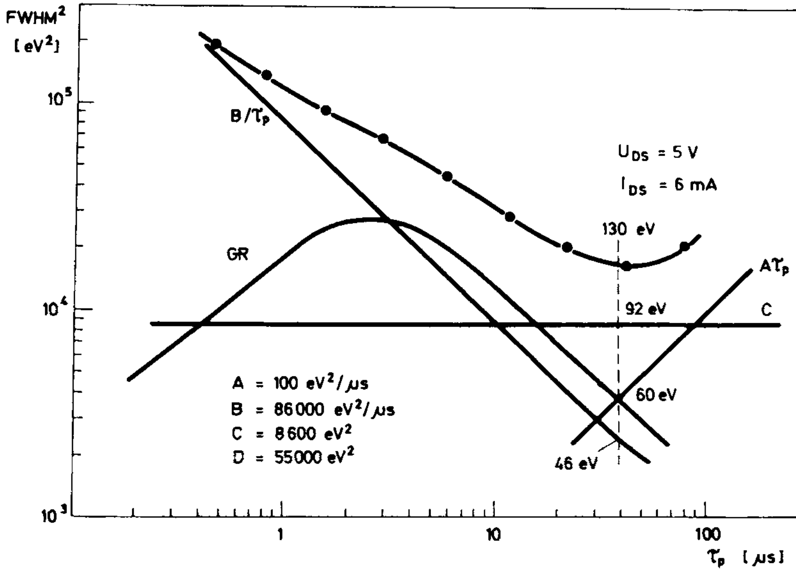

Fig. 6. FWHM^2 versus peaking time of a FET exhibiting GR noise from 0.18 eV activation energy centers

Applicability of the commercial FETs in Si(Li) spectrometers

Si(Li) X-ray spectrometers have been built with detector cryostat [7] and Si(Li) detectors of grooved type, with 20 mm^2 active area and 4–5 mm thickness prepared in our laboratory [3], and with the selected FETs under 135 eV noise level at optimum. The energy resolution of the spectrometers at 5.9 keV measured with NV–809 pulsed drain–feedback charge sensitive preamplifier and NZ-870 time variant filter signal processor [7], [8] with noise indices: $< N_s^2 >= 1.9/\tau_p$, $< N_\Delta^2 >= 0.6\tau_p, < N_{-1s}^2 >= 4$ is between 150–180 eV; the electronic noise is 90–130 eV. FETs not exhibiting GR noise with noise parameters $A \approx 100$ eV$^2/\mu s, B \approx$ 75000 eV$^2 \mu s, C \approx$ 10000 eV^2 have been found most suitable. Some of the FETs belonging to the group of 0.18 eV, 0.21 eV, 0.25 eV activation energy with noise parameter $D \leq 30000$ eV^2 were also used. FETs belonging to the group of 0.1 eV

and 0.2 eV or to the other groups with large value of D are unusable for the first stage of Si(Li) spectrometers.

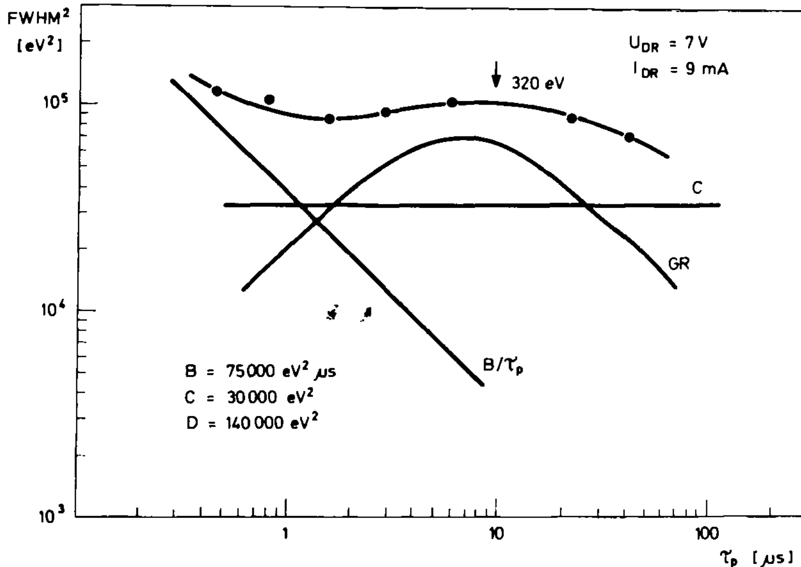

Fig. 7. FWHM^2 versus peaking time of a FET showing large GR noise from GR centres of 0.1 eV

Conclusions

Time domain noise measurements were performed in high impedance gate mode, without Si(Li) test detector for selection of commercial field-effect transistor chips mounted into teflon block. This arrangement has the advantage that the FET noises were measured close to the working condition of the FET in Si(Li) spectrometer without important additional noise. With the measurement of the FWHM^2 versus peaking time at different FET working parameters the optimum working conditions were searched. Less than 15% of the FETs has been found useful for high energy resolution Si(Li) spectrometer application.

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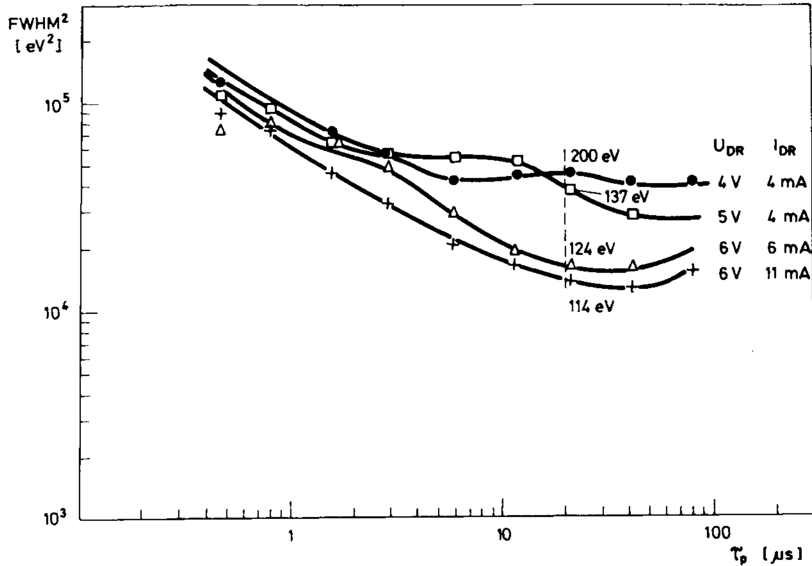

Fig. 8. FWHM^2 versus peaking time curves measured at different power dissipation of a FET having GR noise 0.2 eV activation energy centers

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