Channel Arrangement for optical communication subsystems with 12 parallel channels*

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(Received 27 December 2005)

This paper devoted to report the design and the achievement of an optical communication subsystem with 12 parallel channels in one chip. The system is capable of transmitting 10 Gbps bidirectional date over hundreds of meters. It can provide error detection and correction by using 8B/10B encoding and Cyclical Redundancy Checking (CRC) encoding when only single-channel fails. The design scheme has already passed the simulation in FPGA. This technique is useful to enhance the capability and the reliability of the very short reach (VSR) transmission systems.

CLC number: TN913.7 **Document code:** A **Article ID:** 1673-1905(2006)04-0296-03

Due to the increased operation in transmissions of image data, video and audio data, requirement for higher transmission speed has been accelerated. For which, no metal-media but optical fibers can be competent. Statistical data reported by AT&T indicated that more than 75% of the length of intra office links is within 100 meters. The techniques on high speed of VSR optical transmission become more important in recent years. There are some 100-megabit even gigabit optical Ethernet PC cards which were fabricated abroad using one fiber[1]. If we take the parallel optical transmission technologies, we can speed up the system significantly. Our team had manufactured a kind of 16-channel VCSEL transmission module[2] and a kind of 12-channel VSR transmitter[3]. We also achieved hybrid optoelectronic integrated photodetector arrays[4]. We designed and constructed a VSR evaluation system based on FPGA recently. It can deduce the size of system hardware, make the design more flexible and cut down the time on design remarkably by using field programmable gate array (FPGA). This paper emphasizes research on VSR optical communication system solutions for efficiency and reliability. In this paper we will describe the scheme of VSR parallel optical communication system firstly. Then, we will explain the channel arrangement including error detection and correction. We will also verify our scheme by the emulator at last.

The optical interconnection systems include multiple layers of the OSI protocol stack, which can be applied to IP routers, MPLS, ATM, and Frame Relay switches, as well as optical cross connects (OXC's) and transport platforms, such as wavelength division multiplexing (WDM) systems[5]. Optical Internetworking Forum (OIF) has studied a variety of possible interfaces for OC-192 VSR applications[6]. We prefer to use the implementation agreement (VSR4-01. 0)[7] to build up our system as shown in Fig. 1.

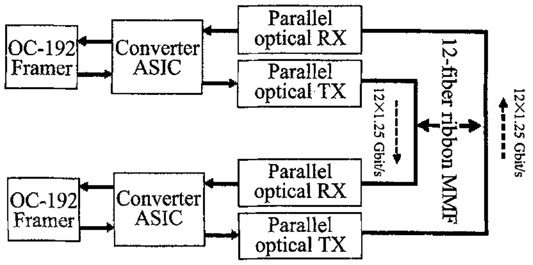

Fig. 1 The VSR4-01.0 system link in this letter

A piece of FPGA will perform all tasks of the converter ASIC in Fig. 1. It will convert the 16-channel 622Mb/s data to the 12-channel 1.244 Gb/s data and in reverse. The functional block diagram of the transmitter has been described in Fig. 2. The 12-channel 1.244 Gb/s data are carried along a fiber ribbon, which has twelve optical fibers. Each fiber carries a separate channel. Channels 0 to 9 are data channels and are used to transmit the OC-192 frame. Channel 10 is a protection channel to carry the XOR bit data from channels 0 to 9 and to protect against single-channel failures, the most common failure mode of fiber optics transmission systems. For example, to call the result of the XOR operation across the ten data channels in the transmitter XOR (10). That is, if channel 7 fails, the receiver logic will

* This work is supported by the National Nature Science Foundation of China (No. 60502005) and the National "863" Project of China (No. 2005AA311030)

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detect this and compute the XOR of the remaining nine data channels (0 through 6 and 8 through 9). The result of this operation can be called from XOR(9). The data bit stream for the missing channel 7 is recovered as the result of XORing XOR(10) with XOR(9). So the data from channel 7 can be recovered at the receiver by extracting it from the protection channel. Channel 11 is the Error Detection Channel (EDC), which carries the CRC information of the other eleven channels and the EDC channel itself. This channel carries calculated CRCs of channels 0 through 10. The data in each channel is divided into "virtual blocks" that are 24 bytes long. The first virtual block of a frame is aligned with the frame delimiter to ensure consistent wrap-around. A 16-bit CRC is calculated for each virtual block in each channel. The CRC is the 16-bit CCITT CRC ($x^{16}+x^{12}+x^5+1$). The eleven 16-bit CRCs are then transmitted serially in the EDC channel with the MSB first. The final two bytes of the EDC channel's virtual block are consist of its own 16-bit CRC calculated over the other eleven 16-bit CRCs. The receiver uses the CRCs to determine whether any error occurred during transmission.

At the receiver, once the channels have been re-aligned, the opposite mapping is done to reassemble the OC-192 frame. The functional block diagram of the receiver has been described in Fig. 3.

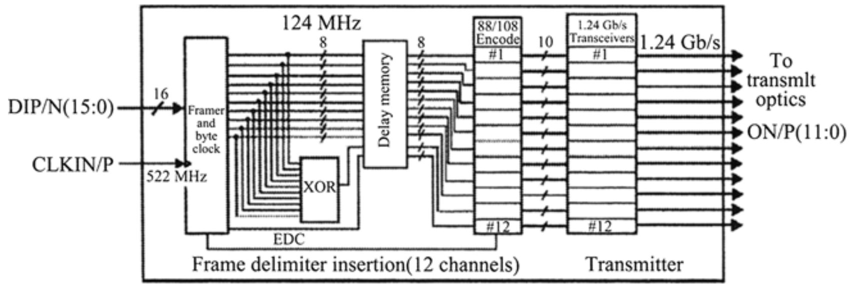


Fig. 2 Function diagram of the transmitter with 12 channels

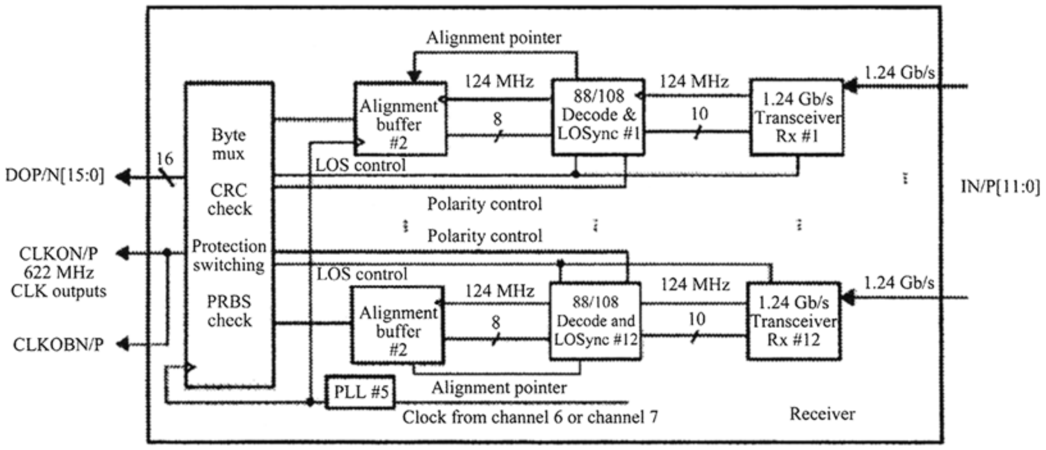
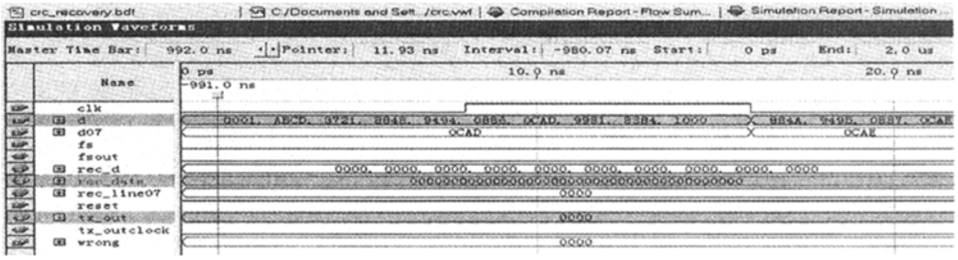


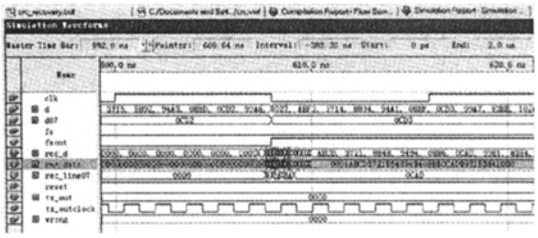
Fig. 3 Function diagram of the receiver

We implement the functions of the 12-channel arrangement in the FPGA. At the transmitter, the XOR bit data from channels 0 to 9 are used to obtain the protection channel data of channel 10 and channel 11 is defined as the Error Detection Channel (EDC). If we disconnect 7th channel of the 10 data channels at the transmitter, we could miss some data, like "OCAD" in Fig. 4, on input ports of the receiver. But, we can recover the right data of this channel and get the same data on the output ports of data-recovery unit. The simulation results are described in Fig. 4. When the data of d07 among the node d is missed at the transmitter shown in Fig. 4(a), we can recover the missed data and obtain the same waveform as the node d after more than 620 ns delay at the node rec_data. But the recovered data in Fig. 4 (b) includes some signal prickles. The data of tx_out in Fig. 4(c) is the last recovered data, in which the signal prickle had eliminated by LVDS_TX module at the receiver. This simulation shows that the data can be clearly and correctly recovered by this system when only one data channel fails.

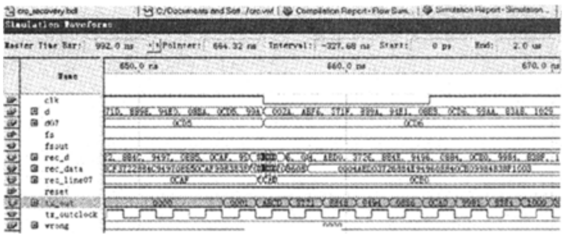
In this paper, a scheme of parallel optical transmission system is described. It can transmit OC-192 SONET frame with error correction. It may be expected that this parallel optical transmission system will play a significant role in the domain of high speed data transmission systems in the near future. We will develop the channel format to optimize the capacity and the efficiency of our system later.



4(a)



4(b)



4(c)

Fig. 4 The simulation results of the missed (a), recovered (b) and tx-out (c) data

References

[1] Cedric F. Lam, Wanyi Gu, Norbert Hanik, and Kimio Oguchi, Proceedings of SPIE, **5625**(2005), 491.

[2] Chen Hongda, Shen Rongxuan, and Mao Luhong, *Chinese journal of semiconductors*, **24**(2003), 245. (in Chinese)

[3] Chen Hongda, Shen Rongxuan, and Pei Weihua, *Chinese journal of semiconductors*, **26**(2005), 1500. (in Chinese)

[4] Pei Weihua, Chen Hongda, and Deng Hui, *Journal of Optelectronics • Laser*, **14**(2003), 893. (in Chinese)

[5] Jiao Yueguang, Yao Jin, and Zhou Bingkun, *Journal of Optelectronics • Laser*, **13**(2002), 759. (in Chinese)

[6] Jugnu J. Ojha, *OIF Very Short Reach (VSR) Interface Implementation Agreements*[S/OL]. [2005-10-08]. http://www.oiforum.com.

[7] OIF Physical and link layer working group, *Very Short Reach (VSR) OC-192/STM-64 Interface Based on Parallel Optics: Implementation Agreement OIF-VSR-*04. 0, California, USA, 2000, 7-13.