Design for SOP AMOLED display panel*

MA Hai-ying, XU Bu-heng, WU Chun-ya, MENG Zhi-guo, XIONG Shao-zhen, and ZHANG Li-zhu**

Tianjin Key Laboratory of Photo-electronic, Thin Film Devices and Technology Institute of Photo-electronics, NanKai University, Tianjin 300071 *China, Tianjin Vocational College Of Mechanics and Electricity, Tianjin* 300131, *China*

(Received 18 April 2005)

A novel full color SOP(system on panel) AMOLED display based on the MIUC polycrystalline silicon TFT technique, and a new control circuit for the panel, which can deal with both VGA and DVI input signals have been developed. To realize gray-scale a sub-frame technique has been designed and implemented by FPGA device, in which an I^2C module has been inserted. Through actual circuit, the whole design has been proven and the advantages of the SOP AMOLED display panel have been confirmed.

CLC number: TN312+.8 **Document code**: A **Article ID**: 1673-1905(2005)01-0027-03

Remarkable efforts to research and development of AMOLED displays have been made to open a new FPD (flat-panel display) application because of their advantages: high contrast ratio, very fast response, very wide viewing angle and simple device structure, etc[1,2].

With the development of FPD, in order to offer the high function display devices, a concept of "System-on-glass" displays has emerged. By integrating various functional circuits onto the display panels, it is possible to realize far more value-added display such as low power, higher information content, high reliable, and more compact terminal display devices.

According to the trend of FPD, a full color 80×60 SOP AMOLED display based on MIUC P-Si TFT technique was designed. MIUC is a recently developed low-cost technique to obtain high-performance poly-Si. Using the technology, high performance circuits can be achieved[3,4].

In order to drive the panel, a new control circuit to realize gray-scale by sub-frame technique has been developed and implemented by FPGA device. The scheme of FPGA device to realize the storage control circuit and display control circuit are designed by using Altera MAX+PLUS II, with Verilog HDL. An I^2C module also has been inserted in the FPGA, to initialize the outside multifunction chip. FPGA is an efficient and flexible device for designing various digital circuits that fit for versatile display interfaces. Moreover, by using of the FPGA, the area of the control circuit can be also saved[5,6].

Fig. 1 shows the SOP AMOLED panel. Each pixel is composed of three-color sub-pixels. The rows and the columns drivers are integrated on the same glass substrate by MIUC P-Si TFT process with the AMOLED display matrix. The drivers are composed of shift registers, which are the static D-type latch-based design based on the clocked CMOS (C2MOS) logic architecture. The panel only has seventeen pins including frame clock, horizontal clock, pixel clock, some enable signals and power pins etc.

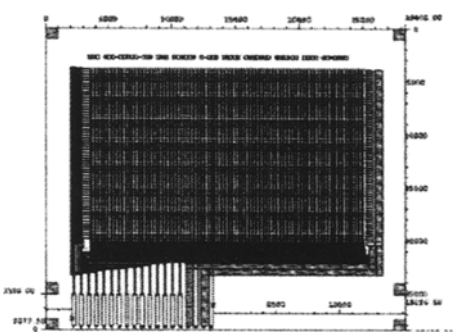

Fig. 1 SOP AM OLED Panel

The AMOLED matrix display is composed of 4800 pixel units. Fig. 2 shows the 2-TFT pixel circuit. The datum signal is written onto the datum storage capacitor C by T_1 when the row line is brought low. T_2 is a PFET device connected in a common source arrangement, and operates as a source follower to provide OLED current. The current is proportional to $(V_{dd}-V_{data}-V_t)^2$ for $V_{data} > V_{oled}-V_t$. Thus, the current can be independent upon the OLED voltage, which may vary from pixel to pixel and increase slowly with usage, $\sim 0.1-1$ mV/hour providing additional sources of no uniformity[7,8,9].

An issue with the circuit shown in the Fig. 2 is the current dependence upon the threshold voltage of T_2.

* Supported by National 863 Project(No. 2004AA33570) and Key Project of National Natural Science Foundation of China (No. 60437030).

** E-mail: irris-mhy@yahoo.com.cn

The threshold variations can significantly impact the pixel-to-pixel uniformity. One exception may be the circuit that is driven hard enough for T_2 to operate as a switch. For gray level operation, multiple sub frame addressing is required.

Thus, we bring up a four-bit digital system to achieve 16 gray levels, which are more than that a natural eye can perceive. By combining the three four-bit colors in all possible ways the familiar palette of 65536 colors can be created. Each pixel in this system has to be addressed four times (once for each bit) to define the brightness of each pixel on the screen. This means that each video frame becomes four sub-frames. The average brightness of the sub-frame is 1, 2, 4 and 8 times of the minimum one. The total time used to display of each frame is 8.7 ms, which is equal to the T_{frame} (16.7 ms) minus the T_{write} (8 ms).

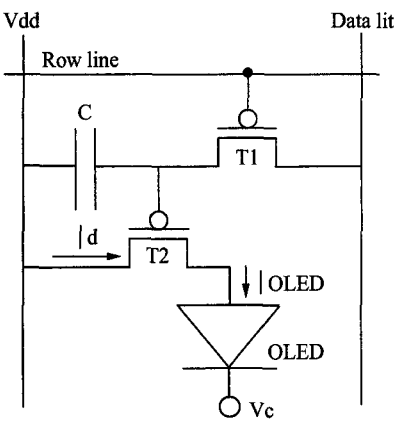

Fig. 2 2-TFT Pixel Circuit

Fig. 3 shows the block diagram of the interface control circuit. The circuit is composed of 12 parts. For example, EPROM is used to store a set of keys, which will unlock and allow the display of the digital content; ICS is used to generate a high quality, high frequency clock output from a lower frequency crystal or clock input; and FPGA configurates device EPC, etc.

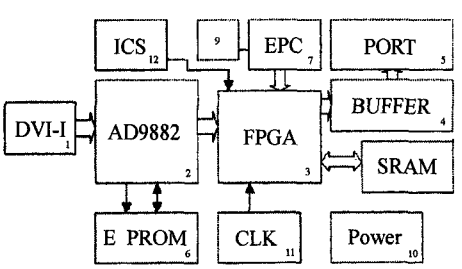

Fig. 3 Block diagram of Control Circuit

The rest main parts including DVI-I, AD9882, and FPGA will be introduced in the following paragraphs.

The Digital Visual Interface (DVI) was introduced by the Digital Display Working Group (DDWG) to create a universally accepted digital interface and to provide the industry with a path towards a single common display interface. DVI is based on Silicon Image's Transition Minimized Differential Signaling technology, which provides a high-bandwidth digital connection between the host computer and a display device. DVI-Integrated (DVI-I) supports both analog and digital connections to the display. This 29-pin connector can carry single or dual-link all-digital video/datum signals on 24 pins and uses 5 pins to carry analog video/datum signals and ground.

To decode the analog and digital signals, we choose AD 9882, which offers the flexibility of an analog interface and a DVI receiver integrated on a single chip. Also a support for High-Bandwidth Digital Content Protection (HDCP) is included. The analog interface contains a 140 MHz triple ADC that supports resolutions up to SXGA with fully integrated sync processing. The outputs mainly include Hsout signal, Vsout signal, Datack signal, groups of eight bits RGB, and a datum enable bit (DE).

Fig. 4 shows the FPGA inner Structure scheme. There are four function blocks. Each block is composed of certain parts coded by Verilog HDL:

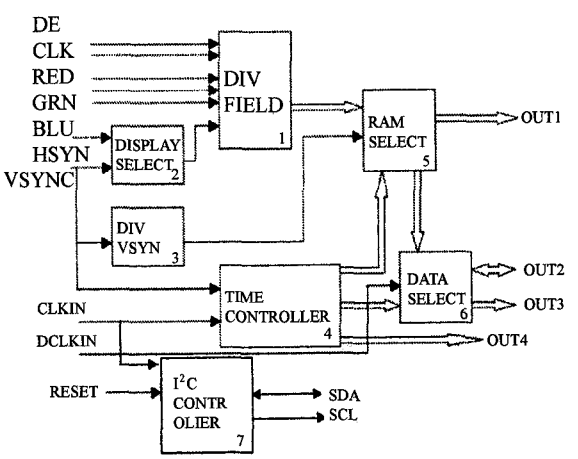

Fig. 4 Inner structure scheme of FPGA

1) DSP unit composed of part 1 and part 2. Part 1 is used to convert the RGB pixel signals decoded by AD 9882 to fit for each sub-frame and sent them to part 5; Part 2 is used to select the area displayed in the AMOLED panel.

2) Time Controller unit composed of part 4. The input signals of the unit include outside clock signal and Vsout signal. It offers control signals for part 5 and part 6; It also generates the delay signals, which determine

the display time of each sub-frame. The delay times are in proportion with 1:2:4:8 in order to realize the 16 gray scales. Meanwhile, it also generates the Vsync clock, Hsync clock, datum clock, and enable signals for the AMOLED display.

3) Output unit composed of part 3, part 5 and part 6. Part 3 acts as a 2-bit counter to generate a clock signal, of which the period is 2 times of the Vsync clock. Part 5 offers the address, write enable or read enable to control the outside storage circuit. Part 6 acts as a bi-direct bus, which sends the datum signals to the AMOLED display panel.

4) Part 7 is an I^2C module. Since the AD9882 is initialized and controlled by a set of registers that determines the operating modes, so we insert I^2C module in FPGA to write the control registers through the 2-wire serial interface port of AD9882. FPGA provides a serial interface that meets the Philips I^2C bus specification and operates in the master transmitter mode, which offers serial datum output through SDA while SCL outputs the serial clock.

MAX+PLUS II offers the Simulator, by which the results of simulation or functional testing can verify the logic function of our design. Fig. 5 shows the top-level simulation results. Through the figure, our design can be confirmed. The main signals are the same as the actual circuit results. The details will be introduce in the following.

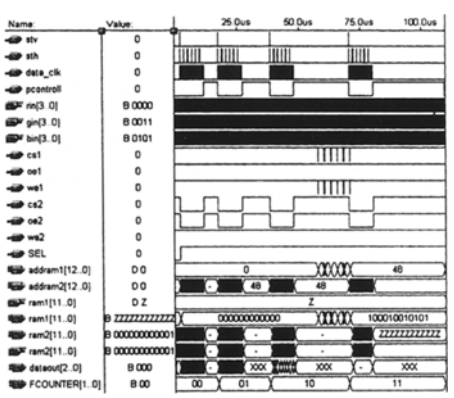

Fig. 5 Top-level simulation result

The results of the actual circuit are measured by multi-channel recording oscillograph of Agilent. As the Fig. 6 shown, the waveform on the top is the V sync signal and the left four pulses are the four sub-frames' V sync signals. In the middle is the Hsync signal. There are 60 Hsync signals in each sub-frame. At the bottom is the Pixel signals. Each row has 80 pixel pulses, while each sub-frame has 4800 pixel pulses. In the Fig. 6, the fifths column means that the first sub-frame's Vsync, Hsync and pixel signals of the next frame. The blank intervals between each pixel signal group are in accord with the brightness time of each sub-frame, which are in

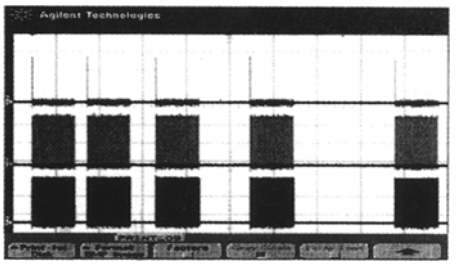

Fig. 6 The Vsync and Hsync, Pixel Signals of the next frame

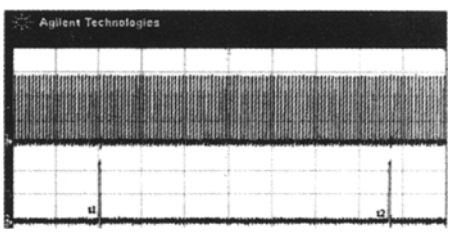

Fig. 7 The Wavefrom of Pixel Signals(up) and Hsyn Signals(down)

proportion with 1:2:4:8. As the Fig. 7 shown, on the top is the waveform of pixel signal and at the bottom is the waveform of Hsync signals, which have been amplified in order to be shown clearly.

Based on the MIUC Silicon technique, we developed a full color SOP AMOLED display panel, which has a 1-inch diagonal display area and 80 * 60 resolution. In order to drive the panel, we also developed a control circuit to realize 16 gray-scales by sub-frame technique, which is implemented by FPGA device.

It is demonstrated that the newly developed SOP AMOLED has opened a new FPD application. We are advancing continuously through development of the novel pixel unit, the higher performance system integrated display panel, and the more effective control method, etc, in order to meet the requirement of the information era.

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