Electrical Effects of Dislocations and Other Crystallographic Defects in $Hg_{0.78}Cd_{0.22}Te$ n-on-p Photodiodes

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An understanding of the effects of dislocations in HgCdTe diodes is complicated by several issues such as the diode architecture, diode formation process, and the thermal history and location of the dislocations. To help decouple the effects of these factors, high stress films were used to lithographically introduce dislocations[1] with different densities and locations during the fabrication process of ion implanted, n-on-p diodes. Both array and diode test structures were studied. After fabrication, the diodes were characterized with variable temperature I-V measurements and noise measurements. The diodes were then stripped and defect etched to quantify the density and distribution of the dislocations. The effects of these process-induced dislocations were analyzed and compared to the effects of as grown dislocations, subgrain boundaries and dislocations in other device architectures reported in the literature.[1,2] In general, high densities of either as grown or process-induced dislocations in n-on-p, ion implanted diodes severely degrade device performance by producing field dependent dark current. At 77K, dislocation densities greater than the mid 10^6 cm^{-2} can produce dark current densities in excess of the diode diffusion current. Dislocations located near the outer periphery of the diode produce approximately ten times the dark current of interior dislocations. Grain boundaries, sub-grain boundaries, and twins also produce sufficient field dependent dark current to limit diode performance at 77K. The dark current produced by dislocations is nearly temperature independent, suggesting rather severe limitations on dislocation densities for low temperature diode operation.

Key words: Dislocations, HgCdTe, ion-implanted n-on-p photodiodes, stress effects

INTRODUCTION

An understanding of the effects of defects in $Hg_{0.78}Cd_{0.22}Te$ is important not only because of their relatively high density compared to other more mature semiconductor materials, but also because the narrow band gap of $Hg_{0.78}Cd_{0.22}Te$ cannot mask even minor perturbations associated with defects. There is a large body of literature on the effects of dislocations in conventional wider band gap materials.[3–8] Only a few papers have previously been written on the effects of microstructure and dislocations on electrical device performance, most frequently directed toward metal insulator semiconductor (MIS) structures.[1,9–15] Last year's conference proceedings included an excellent study of the effects of dislocations on p-on-n double layer heterojunction diodes[2] which is referred to frequently throughout the text of this paper. It is the intent of this investigation to establish a more general perspective of the elecrical effects of dislocations in $Hg_{0.78}Cd_{0.22}Te$ diode devices. Specifically, issues concerning the distinction between dislocations with different thermal histories, different spatial locations within the diode, and different architectural environments are explored.

To address these diverse issues, several different experimental test vehicles were employed. All the experimental structures were grown on nominally 10 micron cut-off wavelength long wave infrared (LWIR) material employing a planar, boron ion implanted n-on-p diode formation process. Test structures on liquid phase epitaxy (LPE) material with variable densities of lithographically defined dislocations[1] were employed for detailed temperature dependent mea-

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surements. Array structures on LPE material with specially chosen high as-grown dislocation densities as well as precisely located lithographically defined dislocations provided a statistical base for quantifying the effects of dislocations. Finally, solid state recrystallized material with exceptionally high densities of grain and sub-grain boundaries was used to fabricate test structures to examine the effect of these defects. In total, temperature dependent current-voltage, capacitance-voltage, noise, quantum efficiency, and laser beam induced current measurements were performed.

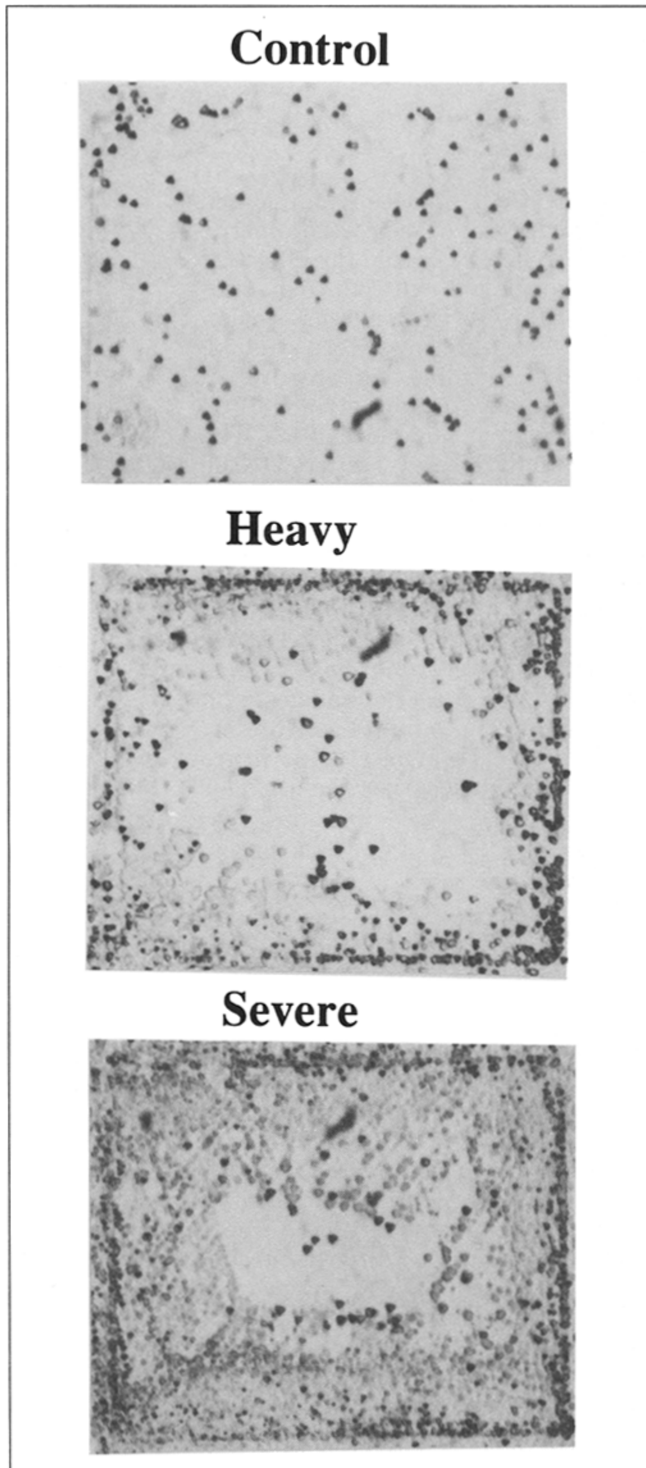


Fig. 1. Defect etches of $Hg_{0.78}Cd_{0.22}Te$ beneath the three types of test structures: control, heavy, and severe structures. Diode dimensions are 125×150 µm.

TEST STRUCTURES

The test structures employed in this study used high stress tantalum films to lithographically define regions of high dislocation density. Details of the technique used to fabricate such structures can be found in the literature.[1] The variably dislocated structures along with undislocated controls were located adjacent to each other on the same film of $Hg_{0.78}Cd_{0.22}Te$ to remove any systematic material or processing variations. The data presented in Figs. 1, 2, 3, and 4 are from a single slice of $Hg_{0.78}Cd_{0.22}Te$ with a cutoff wavelength of 9.8 µm. These test structure diodes were 125×150 µm. Six other slices exhibited similar data. Figure 1 exhibits typical results of the defect etches of the $Hg_{0.78}Cd_{0.22}Te$ beneath each of three distinct diode types with variable densities of lithographically induced dislocations. The most severely dislocated diodes, hereby referred to as severe, were formed by lithographically defining high stress tantalum films coincident with the ion implanted regions. The moderately heavily dislocated diodes, hereby referred to as heavy, used high stress tantalum films covering all regions not receiving the ion implant. The control diodes were not exposed to any high stress tantalum films during processing. There is a large gradient in the dislocation density in the diodes with lithographically defined dislocations. The highest stresses of the tantalum film occur at the outer edge of the diode for both the heavy and severe structures, and this not surprisingly corresponds to the highest dislocation density, at least 1×10^8 cm^{-2}. The severe structures have a wider band of high dislocation density, averaging approximately 2.5×10^7 cm^{-2} over the entire area of the diode, while the heavy structure averages only about 1×10^7 cm^{-2}. The control structures have a uniform dislocation density of approximately 5×10^5 cm^{-2}. Approximately 100 diodes of each of the three types were fabricated and measured before being defect etched.

The most obvious effect of dislocations is to increase the diode dark current. A plot of the dark current density vs inverse temperature can potentially yield insight into the dislocation dark current mechanism. Figure 2 exhibits the dark current density vs inverse temperature at two different biases for all three diode types. The low bias curves are more sensitive to diffusion currents while the high bias curves accentuate the tunneling currents. Several conclusions can be drawn from these plots. At high temperatures (above 100K) and low bias (10 mV), the three curves nearly converge to the same dark current densities. It is clear from the near $Hg_{0.78}Cd_{0.22}Te$ band gap slope of the control curve that its dominant dark current is diffusion current. This implies that dislocations do not significantly increase the diode diffusion current.

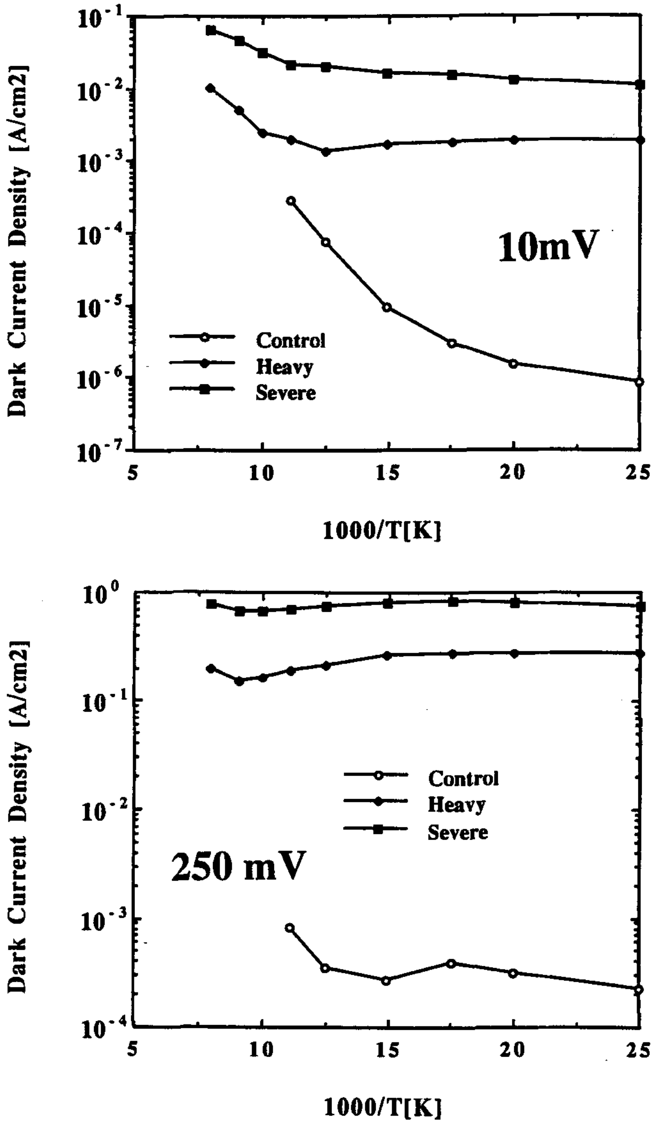


Fig. 2. Dark current density vs 1000/T for the three test structure types at biases of both 10 mV and 250 mV.

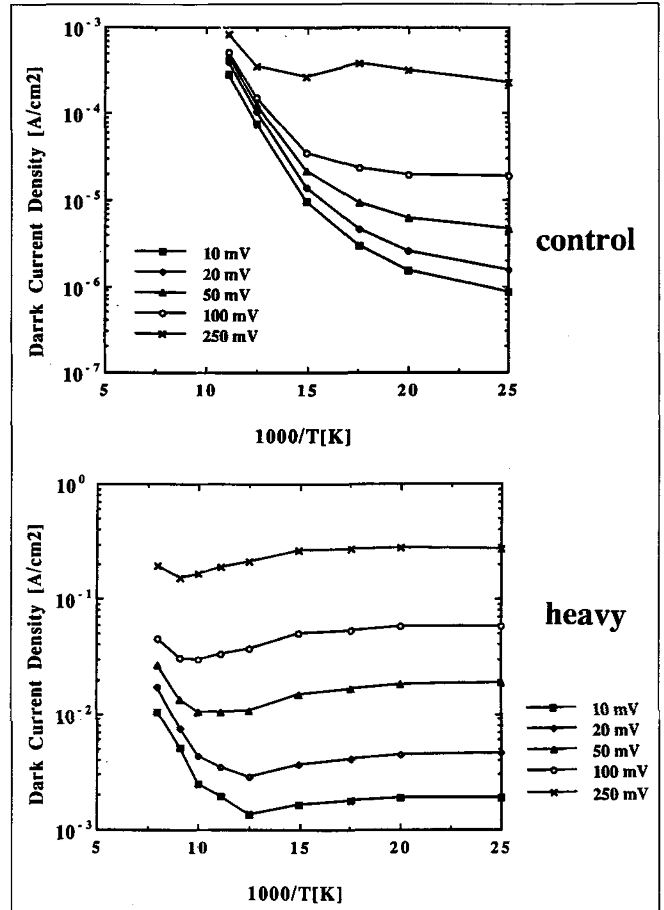


Fig. 3. Dark current densities vs 1000/T and bias for both control and heavy structures.

On the other hand, at low temperatures (below 50K) and low bias (10 mV), there is a three to four order of magnitude decrease in the dark current associated with the control diodes while that associated with the dislocated diodes is nearly constant. The consistency of the dislocation induced dark current throughout the entire temperature range suggests that the dark current has no appreciable activation energy. The lack of a significant activation energy would exclude both diffusion and G-R currents as possible dominant dislocation induced dark current sources. However, it should be noted that it is difficult to completely exclude G-R current as a major dislocation induced dark current in the 100 to 120K transition region between diffusion and tunneling current. Higher quality data and rigorous fitting would be required to definitively resolve this issue.

The dark currents for all three diode types at a 250 mV bias are nearly temperature independent, implying a tunneling dominated dark current interpretation. The three to four order of magnitude offset between the control and dislocated diodes for all temperatures at a 250 mV bias is equal to the offset at 10 mV bias and 40K. This supports the interpretation that all three diode types are tunnel limited at 40K with a 10 mV bias.

In addition to focusing on the temperature dependence of the dark current, it is useful to consider the bias dependence of the dark current in more detail. With the simplest possible assumptions, diffusion current should be independent of diode bias, G-R current should increase as the square root of the bias and tunneling current should increase exponentially with the applied bias. Figure 3 shows the temperature and bias dependence of the dark current of the control and heavy structures. The dark current of the control structure at 80K has very little bias dependence verifying that it is diffusion limited. At 40K, the control exhibits extremely strong nearly exponential bias dependence, verifying a tunneling mechanism. The bias dependence of the heavy structure is less easily interpreted. Between temperatures of 80 and 125K for a 10 mV bias and between temperatures of 100 and 125K for a 50 mV bias, the dark current has a weak, nearly square root bias dependence suggestive of G-R limited dark current. The G-R like dark current appears to become masked by a

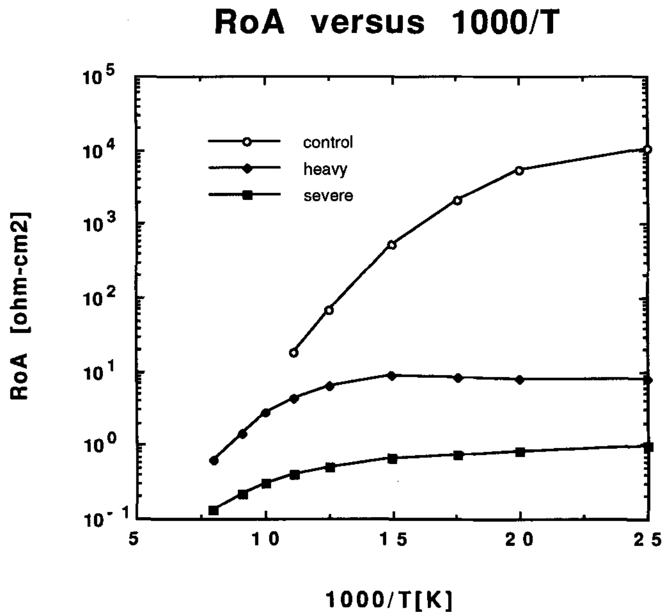


Fig. 4. Dynamic impedance at zero bias, R_0A, vs 1000/T for control, heavy, and severe structures.

more bias dependent, less temperature sensitive dark current as either the temperature is decreased or the bias is increased. This behavior is consistent with the dominance of tunneling current at high bias and low temperature; however, the observed bias dependence is only slightly superlinear and weaker than the low temperature bias dependence of the control. The dark current of the heavy structures at low temperatures have between a linear and quadratic bias dependence while the severe structures have very nearly a linear bias dependence. This nonexponential, nearly linear bias dependence of the tunneling current from dislocations suggests some type of saturation mechanism. The clear increase in dark current with decreasing temperature below the G-R like region is a manifestation of the decrease in the $Hg_{0.78}Cd_{0.22}Te$ band gap with decreasing temperature. This increase in dark current with decreasing temperature for all biases clearly removes any thermally assisted mechanisms from consideration.

To quantitatively compare the above effects of dislocations in planar, ion implanted n-on-p diodes with those in the literature[2] for p-on-n double layer heterojunction devices, it is useful to present the dynamic impedence at zero bias, R_0A. Figure 4 presents the R_0A of typical severe, heavy and control structures as a function of inverse temperature. These plots are very nearly the inverse of the dark currents at 10 mV bias and can be interpreted in an identical manner. Specifically, at temperatures above about 100K, all diode types have comparable R_0As which appear to be limited by diffusion current. At lower temperatures, the control diode R_0A increases by nearly four orders of magnitude due to a drop in diffusion limited dark current. An additional two order of magnitude increase in low dislocation density R_0A can be obtained with the use of more advanced passivation processes. On the other hand, the R_0As associated with the dislocated diodes is nearly independent of temperature due to the temperature independence of the tunneling dark current. This imposes severe constraints on the dislocation density for low temperature operation.

If a comparison is made between the above R_0As and those for p-on-n diodes in the literature,[2] one finds nearly identical temperature and dislocation density dependence. For both architectures, the diodes with low dislocation densities have R_0As which increase rapidly with decreasing temperature. In both cases, diodes with dislocation densities in the mid 10^5 cm^{-2} range have R_0As of approximately 3 to 10 and 3000 to 10000 ohm-cm^2 at 100K and 40K, respectively. Similarly, diodes of both architectures with dislocation densities in excess of 1×10^7 cm^{-2} have nearly temperature independent R_0As of less than 10 ohm-cm^2. The similarity in the effects of dislocations in such vastly different architectures suggests a common origin for the dark current mechanisms. This mechanism is probably trap assisted tunnel-tunnel processes which depend only upon dislocation induced trap states in the n-p junction region. Such a mechanism should be active only if a dislocation actually intersects the p-n junction. It should also be more sensitive to dislocations which intersect the junction and are nearly parallel to it compared to dislocations which intersect the junction perpendicularly. This is based simply on a consideration of maximizing the geometrical overlap between the dislocation and junction. To investigate these properties, it is necessary to consider diodes with much more precisely introduced dislocations.

ARRAY STRUCTURES

As a result of the local variations in the $Hg_{0.78}Cd_{0.22}Te$ yield strength and the stress levels of the high stress films employed for forming dislocations, it is difficult to exactly and reproducibly control the distribution of dislocations produced by high stress films, especially in the limit of low dislocation densities. To effect the ability to lithographically introduce dislocations with exacting positions and densities, one can use the material variations to his advantage by employing the combination of slightly sub-yielding stress levels and a large number of potentially yielding diodes. With this approach, most of the diodes will not exhibit process induced dislocations, but a few will manifest a range of dislocation densities including exceedingly low densities located precisely at the discontinuity of the high stress film.

The above approach was employed using a 64 × 64 array with discontinuous high stress film edges coincident with the implanted diode region. In addition, the starting material exhibited a very wide range of dislocation densities to facilitate comparisons between the effects of as grown and process-induced dislocations on diode performance. Of the 4096 diodes, only approximately 300 exhibited dislocations induced by the high stress films, and of those, only about 50 had sufficiently localized distributions of

dislocations to permit quantitative evaluations. This array had a 77K cutoff wavelength of 9.7 µm and a pixel diode area of 1800 μm^2.

Any attempt to quantify the effects of dislocations intrinsic to the high temperature material growth process by studying dislocations introduced during low temperature device fabrication must first establish their electrical equivalence. As-grown dislocations may have very different densities of defects, traps, and impurities compared to process induced dislocations due to their much higher annealing temperatures. To establish the effects of randomly distributed as-grown dislocations, etch pit counts were performed on 400 diodes which did not exhibit any process induced dislocations. These diodes were especially chosen from the area of the array with the highest as-grown dislocation density. Figure 5 presents plots of the dark current density of each diode vs their etch pit count for three different biases. Most of the diodes had fewer than 10 dislocations, corresponding to dislocation densities less than 6×10^5 cm^{-2}. However, many diodes had between 50 and 150 dislocations. There is a very large amount of scatter in the dark current in Fig. 5. Some of the reasons for the scatter will be discussed later. However, the minimum dark current associated with any given number of dislocations appears to increase linearly with the number of dislocations. The slope of this lower threshold line is similar to that obtained from a least squares fit to all the data. In addition, the amount of dark current per dislocation also appears to be linearly related to the diode bias as manifested by the linear increase in slope of the lower threshold line with increasing bias. From these plots, one would conclude that each as-grown dislocation produces a minimum dark current of 8 pA per mV of bias at 77K. If a diffusion limited dark current of approximately 200 $\mu A/cm^2$ is assumed, or inferred from the graph, this implies that the dislocation dark current will be equivalent to the diffusion current at a dislocation density of 3×10^6 cm^{-2} for a diode operated at a bias of 10 mV. For cutoff wavelengths below 9.7 µm, biases greater than 10 mV or lower temperature operation, the limiting dislocation density would be less than 3×10^6 cm^{-2}.

The high stress discontinuous films in the array produced a variety of dislocation distributions, several of which are presented in Fig. 6. It should be noted that several comparable examples of each of these distributions were apparent on the array. Figure 6a shows a control diode which had no process induced dislocations and seven as-grown dislocations. This was the most commonly occuring dislocation distribution. It had a dark current at 10 mV bias of 3.97 nA. The next most common dislocation distribution is shown in Fig. 6b. The edges of the high stress film created several clusters of extremely dense dislocations. The dark current from this diode exceeded the measurement capability of the test set, i.e. it was greater than 60 nA. Even much smaller clusters of process induced dislocations at the edge of the diode such as those shown in Fig. 6c could produce dark currents exceeding 60 nA. This diode had approximately 30 perimeter process-induced dislocations, 20 interior process-induced dislocations, and 25 interior as-grown dislocations. Figure 6d demonstrates that

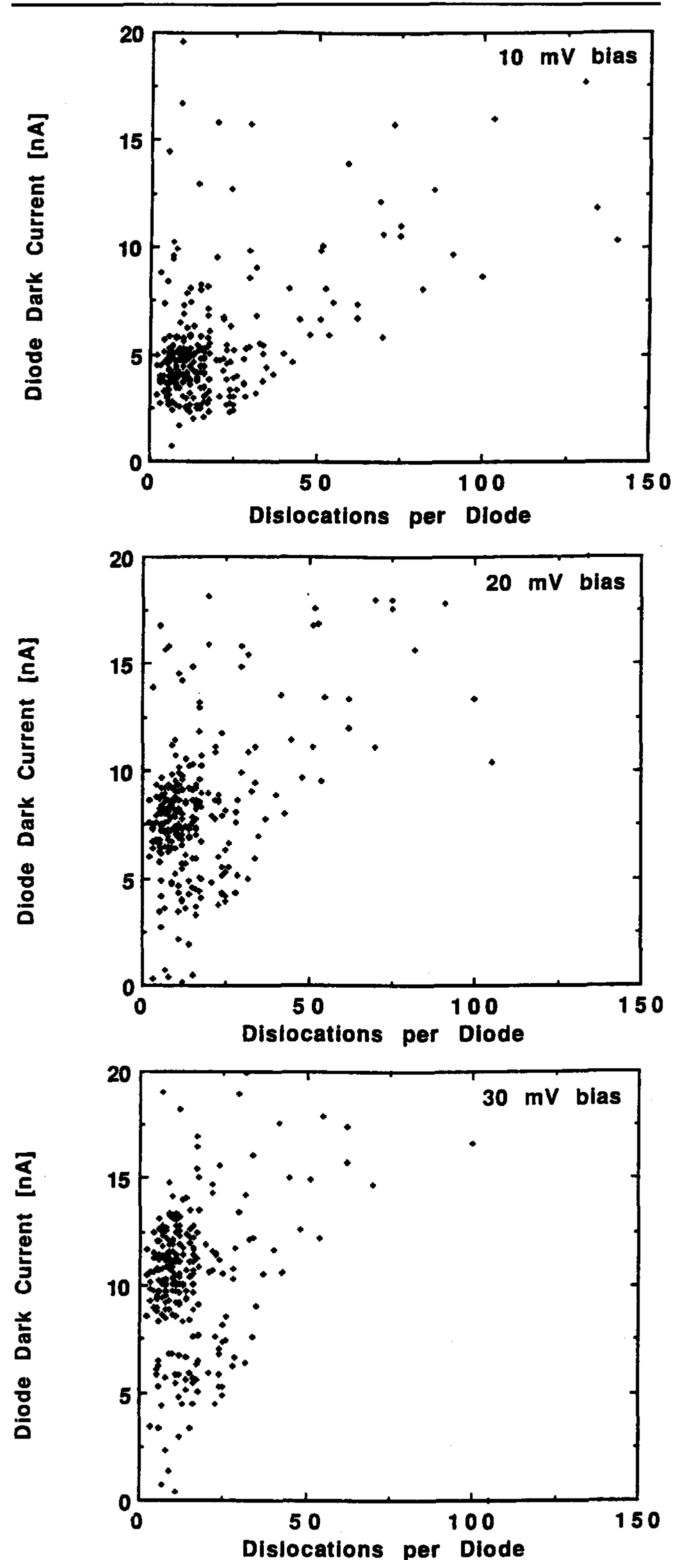


Fig. 5. Dark current vs number of dislocations for isolated as-grown dislocations in array structures at biases of 10, 20, and 30 mV at 77K.

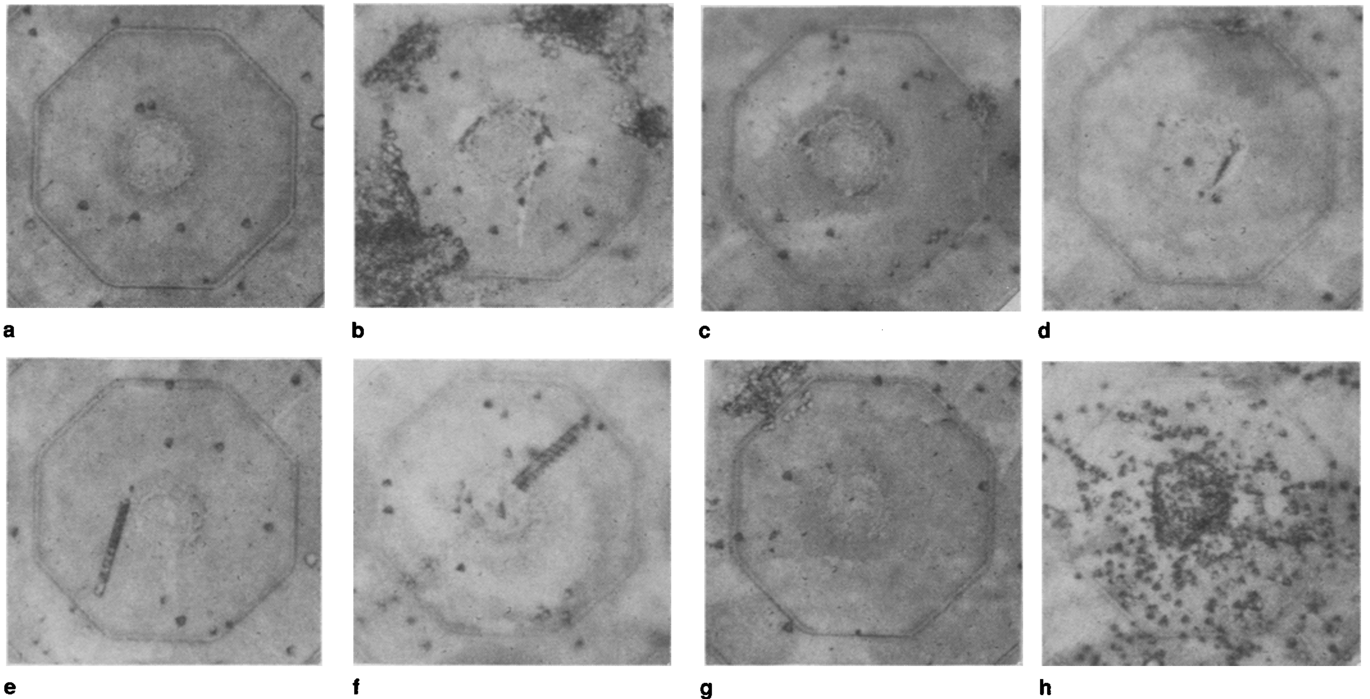


Fig. 6. Defect etches of the $Hg_{0.78}Cd_{0.22}Te$ beneath array diodes with a variety of dislocation distributions including: (a) control, (b) extremely dense process-induced dislocation clusters, (c) small cluster of process-induced dislocations located at the perimeter of the diode, (d) 15 perimeter process-induced dislocations, (e) process-induced single slip line, (f) two process-induced slip lines, (g) dense exterior cluster of process-induced dislocations, and (h) high density of isolated as-grown dislocations.

as few as 15 dislocations can produce excessive dark current if they happen to be concentrated near the diode perimeter. It had 15 perimeter process-induced dislocations, and five interior as-grown dislocations and a dark current of 26.5 nA.

From the above examples, one could attribute the high dark current of the process-induced dislocations either to their intrinsic unannealed nature or to their preferrential location near the outer perimeter of the diode. This perimeter location would enable the dislocation to intersect the p-n junction at an angle nearly parallel to it, thereby fulfilling the condition described at the end of the test structure section. To differentiate between these two possibilities, it is useful to examine other process-induced dislocation distributions. In particular, the high stress film can initiate the formation of slip lines which are not confined to the high stress perimeter of the diode but instead propogate along the natural slip directions of the $Hg_{0.78}Cd_{0.22}Te$ into the interior of the diode. Figures 6e and 6f show such distributions of dislocations. Figure 6e has a single slip line segment in its interior consisting of approximately 25 dislocations in addition to the seven interior as-grown dislocations. This diode has a dark current of only 4.54 nA, significantly less than the 6 nA which would be predicted. This prediction is based on a minimum dark current of 80 pA/dislocation at 10 mV bias in addition to the background diffusion current of 3.5 nA. Similarly, Fig. 6f exhibits a diode with two closely spaced parallel slip line segments which jointly contain 45 dislocations in addition to 18 interior as-grown dislocations. Again the measured diode dark current of 4.73 nA is much less than the 8.5 nA which would be predicted. These results imply that process-induced dislocations do not intrinsically produce more dark current than as-grown dislocations. In fact, these results suggest that the dark current per dislocation for process-induced, interior dislocations at extremely high local densities such as encountered in slip lines tends to decrease as the density is increased. This can possibly be explained by a reduction in the G-R depletion volume per dislocation as the dislocation density becomes very large. This result is also opposite to that reported in the literature.[2] The reason for this discrepancy is unclear but may be related to the difference between perimeter and interior dislocations.

Two additional dislocation distributions are presented in Figs. 6g and 6h. Figure 6g shows a diode with 13 interior as-grown dislocations, four process-induced perimeter dislocations, and approximately 100 process-induced dislocations just outside the diode region. It has a dark current at 10 mV bias of 7.30 nA, which is what would be expected from the interior dislocations alone, which suggests that external dislocations have almost no effect on the diode dark current. Similar independence of the diode dark current on exterior dislocations was found in test structures. Figure 6h portrays a diode with 203 as-grown interior dislocations. It has 21.67 nA of dark current, which is very close to the value of 20 nA predicted from the trend line for isolated as-grown dislocations.

The observations from the array structures have shed light on several fundamental characteristics of

dislocations. First, they show that the dark current attributable to a dislocation is an extremely strong function of the location of the dislocation within the diode. Dislocations within a few microns of, but not intersecting, the p-n junction have negligible effect on the diode dark current. Isolated interior dislocations which intersect the p-n junction along a line segment not too different in length from the depletion width produce approximately 8 pA/mV of bias. Interior dislocations with local densities exceeding mid 10^7 cm^{-2} produce less dark current per dislocation, possibly a result of the decreased effective depletion volume per dislocation for the G-R current at 77K. This saturation density also corresponds to that for which the piezoelectrically generated fields surrounding individual dislocations would start to overlap.[16] Perimeter dislocations appear to produce significantly more dark current than interior dislocations. This increased dark current could be attributable either to the increased geometric overlap with the p-n junction or the increased coupling with potential sources of surface charge. In an attempt to roughly quantify this effect, a perimeter dislocation was for convenience defined to be one with any portion of its etch pit intersecting the p-n junction. Since the etch pit diameters were roughly 2 μm while the junction depletion widths were only a few tenths of a micron, this counting procedure would overestimate the number of perimeter dislocations and thereby underestimate their dark current. Figure 7 shows a plot of the dark current vs number of perimeter dislocations. This plot has a slope of approximately ten times that for isolated as-grown dislocations presented in Fig. 5. The dark current of the perimeter dislocations also appears to be approximately linear with bias implying a lower bound of dark current per perimeter dislocation of 80 pA/mV at 77K.

The dark current of process-induced dislocations was found to either greatly exceed in the case of perimeter dislocations or fall short in the case of interior clusters that of isolated, interior as-grown dislocations. For comparable densities and locations, as-grown and process-induced dislocations appear to have comparable levels of dark current.

In addition to dark current measurements, noise and quantum efficiency measurements were performed. In general, the rms noise of a diode appeared to be proportional to its dark current, hence dislocations indirectly increase the noise level. This behavior is similar to that reported in the literature for p-on-n DLHJ diodes.[2] Perimeter dislocations appear to be particularly noisy since they increase the noise level with dark current at a slope approximately 2.5 times that of other sources of dark current, including interior dislocations. This is possibly due to the stronger coupling of the near surface perimeter dislocations with the noise sources in the surface passivation layer. The quantum efficiency of the diodes appear to be independent of their dislocation density up to the maximum dark current levels measurable on the test set, 60 nA. This would correspond to isolated interior dislocation densities up to the mid 10^7 cm^{-2} range. This was also observed for p-on-n DLHJ diodes.[2]

EFFECTS OF MICROSTRUCTURE

In addition to dislocations, other crystallographic defects such as sub-grain boundaries, grain boundaries and twin boundaries can have major detrimental effects on diode performance. Figure 8 shows three test diodes with variable amounts of sub-grain microstructure. The three diodes have dimensions of 50 × 50 μm, 75 × 75 μm and 125 × 150 μm, and a cutoff wavelength of 9.5 μm. The 50 × 50 μm diode has no microstructure and serves as a convenient control. At 77K, it has a R_0A of 114 ohm-cm^2 and dark current densities at 10 and 100 mV biases of 60 and 79 μA/cm^2, respectively, which is nearly diffusion limited. The 125 × 150 μm diode has two fairly low angle grain boundaries and R_0A, J (10mV) and J (100mV) values of 122 ohm-cm^2, 44 μA /cm^2 and 123 uA /cm^2, respectively. The R_0A and J(10mV) values are similar to the control, while the J(100mV) value is almost twice the control value, suggesting more bias dependent dark current. The 75 × 75 μm diode has a larger angle sub-

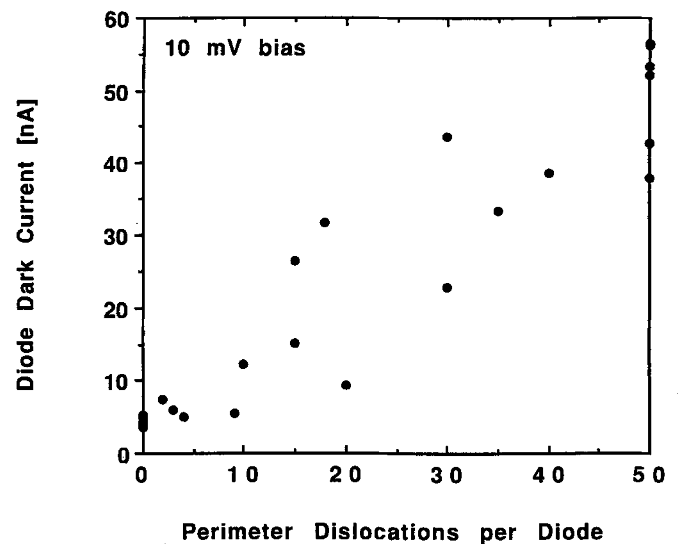


Fig. 7. Dark current vs number of dislocations for process-induced perimeter dislocations.

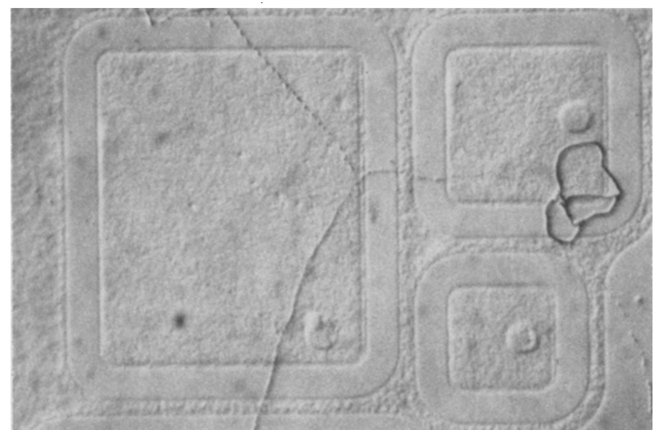


Fig. 8. Defect etch of SSR $Hg_{0.78}Cd_{0.22}Te$ showing sub-grain boundaries passing through diode regions.

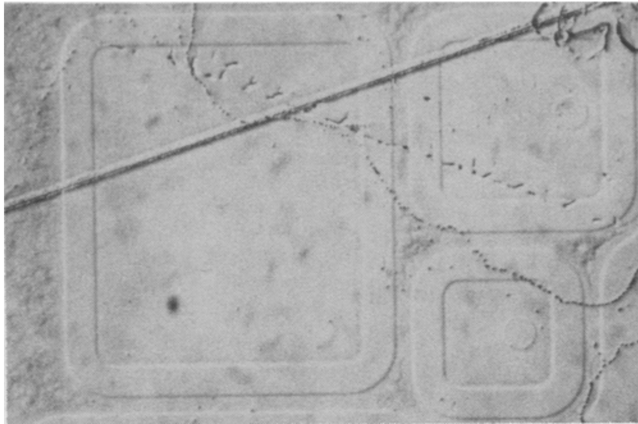
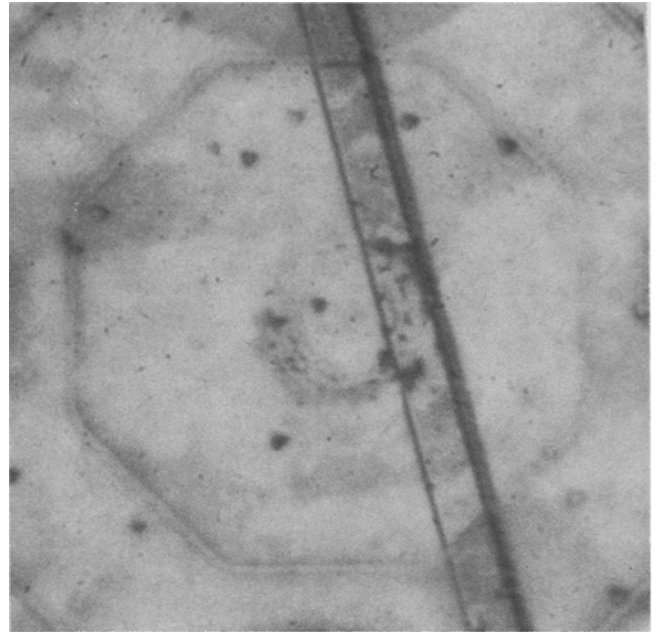


Fig. 9. Defect etch of SSR $Hg_{0.78}Cd_{0.22}Te$ showing a grain boundary passing through diode regions.

grain boundary, based on its relatively greater etch pit density, in its interior which results in R_0A, J (10mV) and J (100mV) values of 28 ohm-cm², 313 µA /cm², and 1093 uA /cm², respectively. This demonstrates that larger angle sub-grain boundaries can strongly affect the dark current both at high and low biases. Figure 9 shows a grain boundary intersecting both the 75 × 75 µm and 125 × 150 µm diodes and only a small angle sub-grain boundary intersecting the 50 × 50 µm diode. Both diodes with the grain boundary have R_0As of less than 1 ohm-cm² while the 50 × 50 µm diode has a R_0A of 45 ohm-cm². Hence, the amount of dark current associated with a grain or sub-grain boundary appears to be strongly dependent upon the angle of misorientation between the grains or sub-grains. The dependence of the sub-grain boundary dark current on both the angle of misorientation and bias are consistent with interpreting sub-grain and grain boundaries as simply an array of dislocations with a density proportional to the misorientation angle. It should be noted that the dark current per sub-grain boundary dislocation is severely depressed compared to that of isolated dislocations, just as it was for dislocations in process-induced slip lines.

Another interesting crystallographic defect is the twin boundary. Depending upon the perfection of the twinning, twin boundaries can have either few or many dislocations associated with them. Figure 10 displays examples of both these types of twin boundaries in diodes of the array geometry. Surprisingly, twin boundaries both with and without dislocations give rise to comparable amounts of dark current, approximately 20 nA per diode. This implies that the crystallographic defect of the twin itself is sufficient to greatly increase the diode dark current.



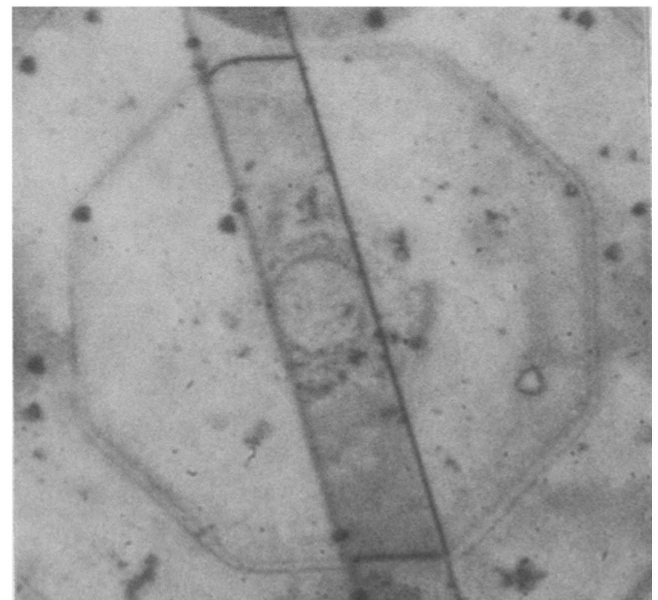


Fig. 10. Defect etch $Hg_{0.78}Cd_{0.22}Te$ beneath array diodes showing double twin boundaries both decorated and undecorated with dislocations.

DISCUSSION AND CONCLUSIONS

From the preceeding results, it is apparent that dislocations, sub-grain, grain, and twin boundaries all produce substantial amounts of dark current which can impact n-on-p diode device performance at 77K. Bias dependent studies show that isolated dislocations interior to the diode appear to produce approximately 8 pA / mV bias / dislocation at 77K. This would lead to dislocation limited dark current at 77K for dislocation densities greater than $3 \times 10^6 cm^{-2}$. Dislocations located along the perimeter of the diode produce at least ten times as much dark current per dislocation as those located in the diode interior, while dislocations which do not intersect the diode appear to have no effect on the diode dark current, even if they are located only a few microns from the p-n junction. Interior dislocations in clusters with densities exceeding the mid 10^7 cm^{-2} appear to produce substantially less dark current per dislocation than isolated dislocations. Temperature dependent dark

current measurements reveal that at temperatures above 77K, the dislocation induced dark current has a moderate temperature dependence suggestive of G-R current. At temperatures below 77K, the dark current associated with dislocations appears to be nearly temperature independent, with only a slight increase in dark current at reduced temperatures. Dislocations appear to have no measurable effect on the diode diffusion current. This implies that dislocation-induced dark current will start to limit diode performance at low temperatures for dislocation densities substantially less than 3×10^6 cm^{-2}. Dislocations appear to increase noise levels only indirectly through their increase in dark current, especially for perimeter dislocations. The quantum efficiency of photodiodes appears to be largely unaffected for dislocation densities less than the mid 10^7 cm^{-2} range. Nearly all the above results are consistent with measurements of the effects of dislocation in p-on-n diodes, with the exception of the dependence of dark current on the dislocation density.[2]

Nearly all of these results can be explained by a simple model. This model assumes that dislocations produce trap states which contribute the major tunnel-tunnel dark current at temperatures below 77K. Since no thermally activated processes are involved, the dark current is nearly temperature independent except for the slight decrease in $Hg_{0.78}Cd_{0.22}Te$ band gap with decreasing temperature. Furthermore, only dislocations which intersect the p-n junction would produce traps effective for tunneling, and those which intersect the p-n junction at an angle nearly parallel to it (perimeter dislocations) would produce a greater number of effective trap states per dislocation than dislocations intersecting the junction at a nearly perpendicular angle (interior dislocations). Perimeter dislocations also intersect the junction in close proximity to a surface which could act as a source of dark current and noise. The presence of dislocation induced trap states in the p-n junction as well as the additional dark current associated with surfaces are common to both n-on-p and p-on-n architectures and can explain their similarities. At temperatures between 77K and 120K, one has the option of invoking G-R current as the dominant dark current mechanism. This explains the moderate bias and temperature dependence of the dark current in this temperature range, as well as the apparent decrease in dark current per dislocation at extremely high dislocation densities. It is possible but more restrictive to propose that the apparent dislocation induced G-R current is simply a transistion between the dislocation induced tunneling current and dislocation independent diffusion current. At higher temperatures, the dark current is masked by diffusion current which appears to be independent of the dislocation density. The transition temperatures of the above model are based on dislocation densities of 1×10^7 cm^{-2} and diode biases of 10 mV. Higher dislocation densities or diode biases would increase the transition temperatures.

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