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Single phase power factor correction – A review

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Abstract. This paper provides a comprehensive review of the past and recent developments in the area of single-phase power factor correction (PFC) techniques. The motivation for the research in this area, and the manifold directions into which the research has gained impetus, are clearly brought out. The various PFC techniques are broadly classified into (1) passive, (2) active, and (3) active–passive PFC techniques. The active PFC techniques, based on the output dynamics, are further classified into (1) conventional techniques which have slow output dynamics and (2) techniques with fast output dynamics. The critical issues within each PFC technique are discussed in detail. An extensive list of references is also provided at the end.

Keywords. Power factor correction; single-phase; agency standards; IEC.

1. Introduction

Most applications requiring *ac-dc* power converters need the output *dc* voltage to be well regulated with good steady-state and transient performance. The circuitry typically favoured until recently (diode rectifier–capacitor filter) for the utility interface is cost effective, but it severely deteriorates the quality of the utility supply thereby affecting the performance of other loads connected to it besides causing other well-known problems. In order to maintain the quality of the utility supply, several national and international agencies have started imposing standards and recommendations for electronic equipment connected to the utility. Since the mid-1980's power electronics engineers have been developing new approaches for better utility interface, to meet these standards. These new circuits have been collectively called *Power factor correction (PFC)* circuits.

Reducing the input current harmonics to meet the agency standards implies improvement of power factor as well. For this reason the publications reported in this area have used "Power factor correction methods", and, "Harmonic elimination/reduction methods" almost interchangeably. Several techniques for PFC and harmonic reduction have been

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reported and a few of them have gained greater acceptance over the others. Commercial IC manufacturers have introduced control ICs in the market for the more popular techniques.

In this paper, we examine and review the developments in the field of single-phase PFC techniques. Section 2 covers briefly the background information in this area. Following this, § 3 outlines a few passive PFC techniques. This is then followed by § 4 which summarises and discusses various recent developments in the field of active PFC. Section 5 then presents a few active–passive PFC techniques and their merits.

2. Background

2.1 *Conventional single phase ac-dc utility interface*

Conventionally, the utility interface of a low power single phase off-line *ac-dc* converter typically consists of a simple uncontrolled rectifier feeding a bulky filter capacitor (see figure 1a). An input π filter, not shown in the figure, is usually present in the *ac* side in commercial products to reduce the electromagnetic interference (EMI) due to the converter. The bulk capacitor, C_{in}, is designed to maintain the ripple in the *dc* bus to an acceptable level and also to meet the "hold-up time" requirements. The circuit draws narrow input current pulses around the line voltage peaks (see figure 1b).

2.1a *Power factor:* Power factor (PF), is defined as the ratio of the average power to the apparent power,

$$\text{PF} = \frac{\text{average power}}{\text{apparent power}} = \frac{V_s I_{sl} \cos\theta_1}{V_s I_s} = \frac{I_{s1}}{I_s} \cos\theta_1. \tag{1}$$

Power factor reflects how effectively the given source power is utilised by the load. In (1), it has been assumed that the input voltage is sinusoidal with low distortion. Here, V_s is the *rms* input voltage, I_s is the *rms* input current, I_{s1} is the *rms* value of fundamental input current, and θ_1 is the phase angle of the fundamental current.

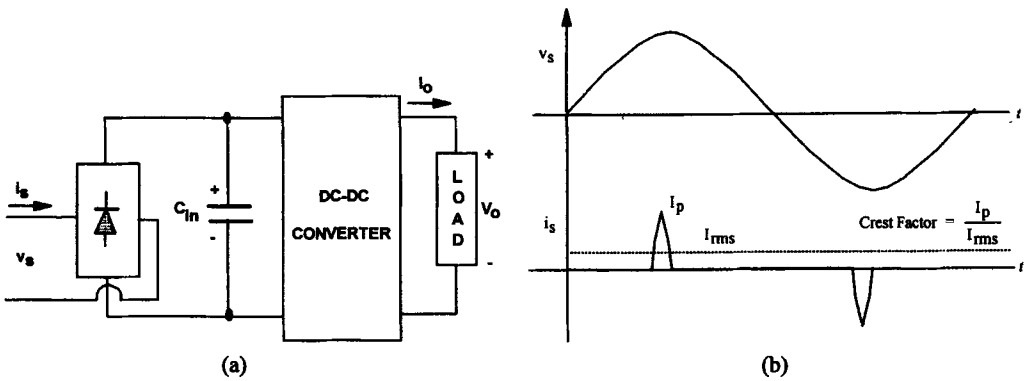

Figure 1. Off-line converter and its input waveforms. **(a)** Block schematic diagram. **(b)** Typical input waveforms.

Table 1. Typical input current harmonics of the single-phase rectifier–capacitor type interface.

n	3	5	7	9	11	13	15	17
$(I_{sn}/I_{sl})\%$	87	80	78	70	63	50	41	30

Note: Even harmonics are zero in magnitude

The ratio I_{s1}/I_s is the *distortion factor*; its value reflects the effect due to input current harmonics. The cosine of the angle θ_1 is the *displacement power factor*; its value reflects the conventional power factor when there is no distortion.

2.1b *PF and harmonic components of a conventional interface:* The narrow current pulses drawn by the conventional rectifier–capacitor type interface is rich in harmonics. The typical harmonic amplitudes of such an interface is listed in table 1 as a percentage of the fundamental [4]. The third, fifth, seventh, ninth and the eleventh harmonics, are considerable in magnitude.

The displacement factor being close to unity, the PF in a conventional interface is strongly linked to the distortion factor. The PF of operation is also quite poor (typically 0.60).

2.2 *Utility issues and agency standards*

2.2a *Problems of conventional interface:* The large harmonic content (see table 1) and the consequent poor PF of operation of the conventional rectifier–capacitor type interface causes several problems to the utility supply. Some of them are listed below. References [1–4] discuss these in greater detail.

(i) Due to harmonic components – Because of the non-zero source impedance in the utility supply, the harmonic currents flowing through it will cause the voltage waveform to be distorted at the point of common coupling to other loads. This may cause malfunction of other loads and also of power system protection and metering devices. Besides voltage waveform distortion, harmonic components can also cause the following problems.

(1) Overheating of the neutral line.

(2) Interference with communication and control signals.

(3) Overvoltages due to resonance conditions.

(4) Overheating of the distribution transformer and distribution lines.

(ii) Due to poor PF – Poor power factor of operation implies ineffective use of the volt–ampere ratings of the utility equipment such as transformers, distribution lines and generators. Also, it places a restriction on the total equipment load that can be connected to a typical home or office wall-plug with specified maximum *rms* current rating.

2.2b *Agency standards:* Due to the proliferation of power electronic equipment connected to the utility system, the concern over the pollution of the utility supply has been growing stronger over the years[7–10]. It has been reported that 5% of the utility generated power in USA is consumed by desk-top computers alone [5]. In order to facilitate the delivery of quality power to end-users and also to utilise the existing power generation and distribution equipment more effectively, several national and international agencies have started imposing strict standards that specify the extent of harmonic pollution that can be tolerated in the line current. One such standard (International Electrotechnical Commission IEC-555-2 or EN-1000-3-2) is expected to be implemented in Europe shortly [6]. Countries like USA and Japan are also showing strong inclination to impose similar standards.

2.3 *Desirable features of a PFC technique*

Input side features:

(1) Sinusoidal input current with close to unity PF operation.

(2) Reduced EMI.

(3) Insensitive to small signal perturbations in the load (i.e., good output-to-input susceptibility figure).

Output side features:

(1) Good line and load regulation.

(2) Low output voltage ripple.

(3) Fast output dynamics (i.e., high bandwidth).

(4) Multiple output voltage. levels if needed by the application.

Others: Electrical

(1) Galvanic isolation between input and output.

(2) High power conversion efficiency.

(3) Hold-up time if required.

(4) Universal input voltage operation (85 V–270 V *ac rms*).

Mechanical

(1) Low part count.

(2) Smaller size and weight.

Economical/environmental

(1) Low cost.

(2) Power save feature (green supply).

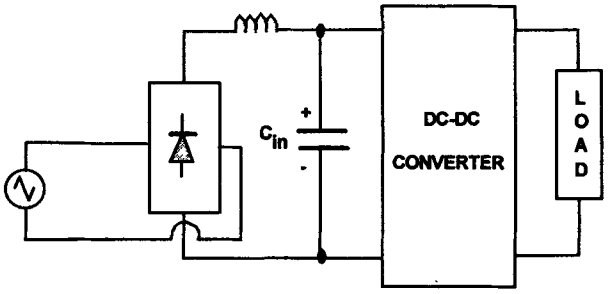

Figure 2. Conventional rectifier circuit with inductive filter.

3. Passive PFC techniques

The power line disturbances caused by the proliferation of phase controlled and diode rectifier circuits were of concern even in late 70s [3,11]. The definition of power factor for nonlinear circuits and passive techniques for improving it are presented in an early literature [11]. Currently, passive techniques remain attractive for low power PFC applications [16,19]. It has been reported [19] that power factor as high as 0.98 can be achieved using passive PFC techniques. The following sub-sections discuss a few of the passive PFC arrangements.

3.1 *Inductive filter*

Figure 2 shows a well-known scheme [4,11], with an inductor inserted between the output of the rectifier and the capacitor. The inclusion of the inductor results in larger conduction angle of the current pulse and reduced peak and *rms* values.

For low values of inductance the input current is discontinuous and pulsating. Typical PF achieved in discontinuous mode operation (DCM), with practical values for the inductor, is in the range of 0.65 to 0.75. Better power factor (PF) is achievable by using a larger value of the inductance and pushing the operation to continuous conduction mode (CCM). However, it is shown [11] that even for infinite value of the inductance, the PF cannot exceed 0.9 for this arrangement.

The inductor may also be introduced on the *ac* side [4]. The position of the inductance will not affect the PF in DCM operation. Under CCM operation, however, the circuit behaviour itself will be different depending upon the location of the inductance. For instance, the presence of an infinite inductance on the *ac* side (i.e. CCM operation) will result in zero input current and zero voltage across the bulk capacitor, theoretically. However, the same inductance on the *dc* side will result in rectangular blocks of current in the input with the bulk capacitor charging up to the average value of the rectified input voltage.

For lower power levels, the distribution line inductance will itself act as a good filter. For an office plug point (15 A), the line inductance is typically in the range of 1 to 4 mH. An estimate of this value can be obtained from the assumption that the *ac* side reactance X_s $(= \omega L_s)$ is 5% of the ratio of nominal rated voltage to the maximum current rating of the plug point [4]. A practical value for the line impedance seen at a particular wall-plug outlet, may also be obtained using the method suggested [72].

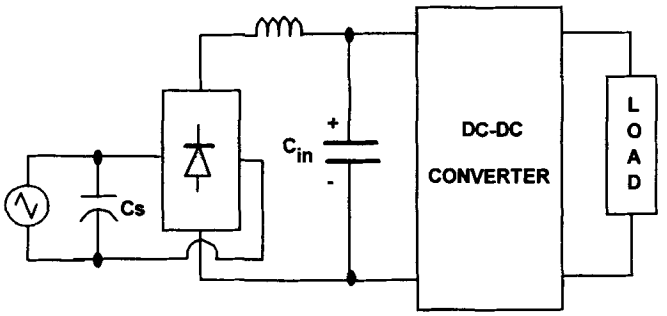

Figure 3. Rectifier circuit with input capacitor C_s.

In the scheme shown in figure 3, a small filter capacitor C_s is connected across the input terminals of the circuit. The line inductance (not shown in figure 3) and C_s forms the first stage LC filter. Therefore higher order harmonics of the line frequency will undergo greater attenuation (typically 80 dB) resulting in better harmonic performance. It is reported [12] that even for relatively small values of the inductance, a PF of 0.86 is attainable, which is a considerable improvement over the no-capacitance case.

3.2 *Resonant input filter*

Figure 4 shows the series filter arrangement for power factor correction [13–14], which results in good power factors as high as 0.94. Thus, harmonic performance is also good. However, the power factor depends upon the resonant quality factor which is load dependent. Here the bandpass filter is designed with a centre frequency equal to the supply frequency. The quality factor "Q" determines the bandwidth and hence the harmonic content of the supply current. High "Q" (narrow bandwidth) will result in reduced harmonic content and close to unity power factor. This circuit arrangement is popularly used in applications where the supply frequency is high. One such application is the space platform [13–14], with supply frequency up to 25 kHz.

Some authors [15,17], suggest the use of parallel resonant filter (see figure 5) for PF improvement. With this arrangement power factor close to 0.95 is achieved. The filter is tuned to offer a very high impedance to the third harmonic component (the most predominant). The high value parallel resistor is added to damp out circuit oscillations.

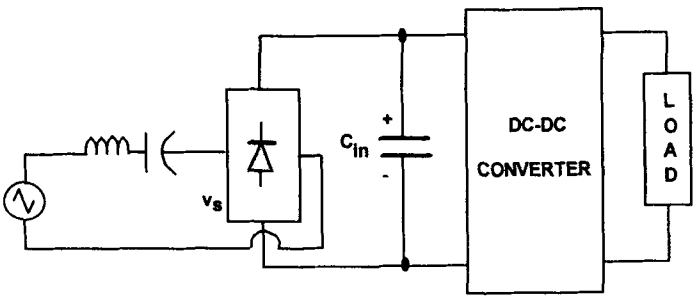

Figure 4. Rectifier circuit with series resonant filter.

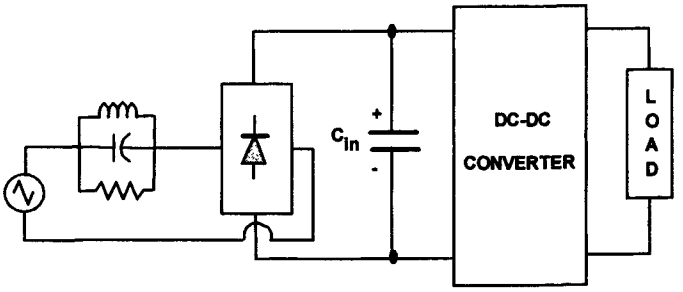

Figure 5. Conventional rectifier circuit with parallel resonant filter.

3.3 *Evaluation of passive techniques*

Passive filters may prove to be a good solution [16–18] for switch mode power supplies (SMPS) operating at lower power levels (<200 W). Typical applications are TVs, VCRs, other home entertainment electronics, and perhaps some of the lower powered office automation equipment such as computers, FAX machines etc.. It is to be noted that in these applications the real aim of the filter is to contain the harmonics within the agency specified limits [6] and not improvement of power factor *per se* [93]. At such power levels the passive solution is economical [16,19], and more efficient and may also result in size benefits. However, even for low power levels, there are a few factors that make the passive solution less attractive than the active solution in certain cases. The factors are as below.

Universal input voltage range (85 V to 280 V ac, 47 to 63 Hz): It is desirable for both the manufacturers and the users that the equipment works in all these supply conditions without any modifications. This requirement is difficult to meet using passive PFC technique whereas it is an inherent feature in many active PFC techniques.

Optimal use of the wall outlet power: Passive PFC technique results in lower PF than active PFC technique. Therefore, passive PFC technique is less attractive when priority is given to optimising the use of the wall plug's volt-ampere capacity rather than just meeting the agency standards. Optimising the wall plug's VA capacity allows a user to plug more equipment to the same wall outlet.

For higher power levels, however, the passive solution suffers from disadvantages such as:

(1) Large size of the reactive elements [17,24].

(2) May not be able to contain the harmonics within the agency specified limits (the agency requirements are different for different power levels [6]).

(3) Poor power factor compared with active schemes.

(4) Not cost effective.

However, the passive solutions are simple to understand and implement, besides being robust and reliable. Also, the use of passive solutions do not generate EMI which is a problem that needs to be addressed with active solutions.

4. Active power factor correction

The active PFC technique, which involves the shaping of the line current using switching devices such as MOSFETs (metal oxide semiconductor field effect transistors) and IGBTs (insulated gate bipolar junction transistors) is a result of advances in power semiconductor devices and microelectronics. For low and medium power ranges up to a few kilowatts (<5 kW), MOSFETs are by far the popular choice for PFC because of their switching speed, ease of driving and ruggedness. BJTs and more recently IGBTs are used for high voltage medium power applications which MOSFETs are unable to contend with owing to their large on-state resistances.

For achieving good input current waveshaping using active techniques, typically the switching frequency should be at least an order of magnitude greater than 3 kHz (= 50 × 60 Hz = 50th harmonic of line frequency). With modern advances in MOSFETs and IGBTs, this is feasible.

The use of active PFC techniques results in one or more of the following advantages.

- Lower harmonic content in the input current compared to the passive techniques.
- Reduced *rms* current rating of the output filter capacitor.
- Near unity power factor (0.99) is possible to achieve with the Total Harmonic Distortion (THD) as low as 3–5%.
- For higher power levels active PFC techniques will result in size, weight and cost benefits over passive PFC techniques.

The following sub-sections present the recent advances in single phase active PFC techniques. The active PFC techniques have been classified into two broad categories in this survey.

(1) Active PFC techniques with poor load dynamics. These have been referred to in this paper as "*Conventional active PFC techniques*" (§ 4.1). They are typically followed by a *dc-dc* downstream converter which caters to the demands of the load.

(2) Active PFC techniques with fast load dynamics (§ 4.2). Here, the PFC unit is capable of meeting the fast dynamic requirement of a typical load.

4.1 *Conventional active PFC techniques*

Here, there are basically two approaches. One approach is to use current-source-type circuit [47–51], in which the PFC acts as a current source feeding the load. Using the other approach results in the well known voltage-source-type circuits discussed [20–23,25–46,52–54, 57–68,70–72,75–95,102]. Though the voltage source type circuits are more popular, the current source type circuits are useful in certain niche applications. In the following subsections both types of circuits and schemes are discussed.

4.1a *Topologies:* The current-source-type PFC converter [47–51] is usually of buck type. However, for the voltage-source-type PFC converter, any one of the basic *dc* to *dc* converter switching cells, such as buck, boost, buck-boost and Cuk converter, can be used. Among

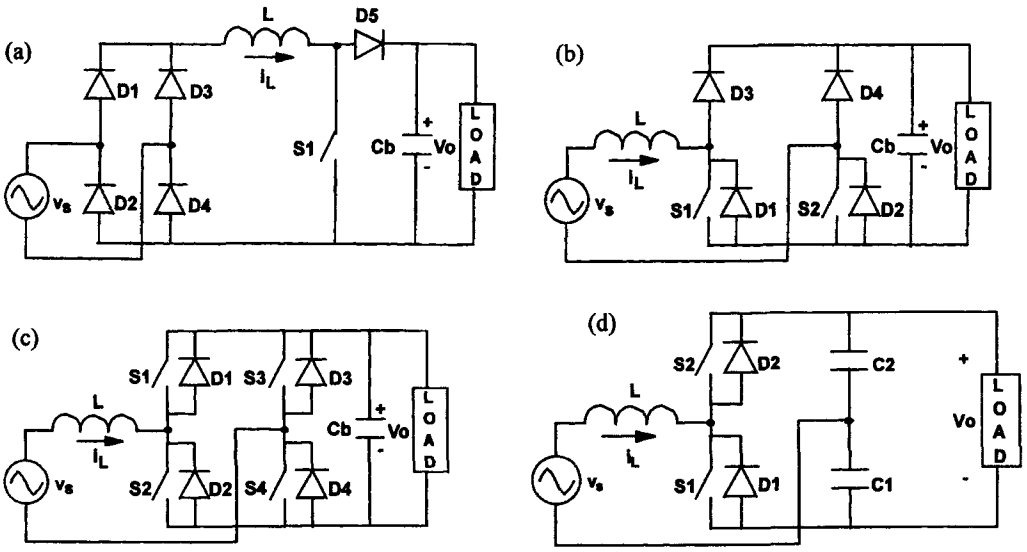

Figure 6. Circuit variations of the boost PFC topology. Single-switch (**a**), two-switch (**b**), four-switch (**c**), and half-bridge (**d**) boost PFC's.

these, the boost and the buck-boost topologies are more popular. In the following sub-sections the notable features of these topologies (both current and voltage source types) and certain critical issues related to these topologies are presented.

(i) Boost topology – In figure 6, some of the popular boost circuits are shown. Several features in the boost converter such as the position of the inductor on the input side (reduced input current ripple and EMI), and a *dc* voltage gain greater than unity, make it a natural choice for active PFC application [4]. The single-ended boost converter (figure 6a) is more popular due to its use of a single active switch and also due to the ease of driving the switch. Several modes of operation are possible for the single-ended boost converter topology.

(1) Continuous conduction mode (CCM) [25].

(2) Boundary of CCM and DCM[27].

(3) Discontinuous conduction mode (DCM) [102].

Boost CCM: This is a very popular choice for medium and high power applications. In this, the supply ripple current due to switching is low because of the presence of the large boost input inductor. Hence, the input filtering requirement is relatively low. Isolated version of boost PFC converter is also available [29]. The following issues are to be noted in relation to the boost converter operating in CCM.

Reverse recovery loss: The reverse recovery loss of the output diode is a serious problem in the single-ended boost converter operating in CCM [70–71]. The output diode should handle a reverse blocking voltage equal to the output voltage, which for the universal input voltage range (85–280 V) is typically set at 380–400 V. The reverse recovery time (t_{rr}) for such high voltage diodes is generally very high resulting in large reverse recovery losses.

This reverse recovery of the diode also increases the turn-on losses in the boost switch. This factor places a limitation on the switching frequency. Hence, the size of the unit cannot be reduced beyond a certain limit. The reverse recovery also causes increased EMI [71].

Charge dumping loss: Another factor that limits the switching frequency is the parasitic output capacitor (typically around 150 pF) of the boost switch, usually a power MOSFET. The capacitor's energy is lost in the channel of the switch during turn-on; the resulting power loss could be significant at high switching frequencies.

EMI performance: In a conventional off-line converter (figure 1), the line current is narrow and peaky. However, the waveform is still smooth with very little switching component owing to the presence of a bulky capacitor, C_{in}, at the output of the bridge rectifier feeding the *dc-dc* converter (see figure 1a). As a result, the input EMI filter size can be small. In the case of boost PFC converter, however, the switching frequency components are directly fed into the supply lines. Hence, a large EMI filter is required in spite of the presence of the boost inductor, L. The issues related to EMI filtering are presented [73,74].

Cusp distortion: The single-ended boost converter (figure 6a) operating in CCM suffers from line current distortion near the zero crossings [43,54]. This is because the reference current slope at zero crossings is higher than the slope of the charging current of the boost inductor which defines the maximum current rate at which the input current can be increased. The effect of this "cusp" distortion is to introduce line current harmonics. In DCM operation, cusp distortion may be lower, as only a small value of inductor will be used.

One or more of the foregoing problems may be addressed by using loss-less switching techniques. By turning the switch on during the instants when the voltage across it is zero (zero voltage switching – ZVS) the problem of loss due to charge dumping is solved. ZVS also helps to reduce the EMI. In converters using resonant techniques [58–59] to realise ZVS, even though switching losses are minimised, conduction losses and switch voltage stresses are higher compared to those using PWM control. This problem, however, is less severe in converters using PWM soft switching techniques [103–105]. Hua *et al* [105], a soft switching technique for a boost PFC circuit.

Boost in CCM – DCM boundary: The converter operating at the boundary of CCM and DCM is also a popular PFC technique used mainly for low power applications such a electronic ballasts for lighting [27]. The operation of the converter in CCM–DCM boundary eliminates the problems due to reverse recovery of the output diode. However, the charge dumping loss is not prevented. The high value of the switching currents places a severe stress on the switch, diodes and the output capacitor. The input filtering requirements are also high. It is this factor that limits its application to low power levels.

Boost DCM: As a front-end PFC converter in a cascaded scheme (§ 4.3a), the boost circuit operating in DCM mode is seldom used, as it offers no special advantage over that

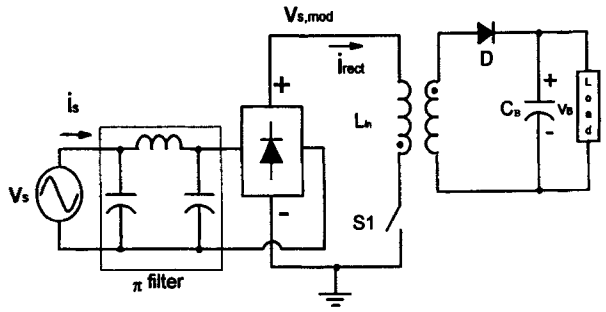

Figure 7. Flyback PFC converter.

operating in the boundary of CCM and DCM. However, operation in DCM is popular in single-stage PFC implementations (see § 4.3c) that use boost circuit as front part of the converter. Unlike the flyback converter discussed in the following paragraphs, a boost converter operating in DCM does not yield a sinusoidal input current (neglecting the switching components) if the duty ratio is held constant over a line cycle.

(ii) Buck-boost or flyback topology – The flyback topology (figure 7) is attractive for low power applications.

(1) The start-up inrush current problem faced by the boost topology is not present here.

(2) The implementation of the overload protection is simple compared with the boost topology.

(3) The output voltage may be greater or less than the peak input voltage.

(4) Implementation of galvanic isolation between the input and the output is simple with flyback topology.

Both CCM and DCM modes are possible for flyback PFC converter [26,36]. But in either mode the input current is chopped resulting in more noise and EMI than with a comparable boost topology. However, the DCM operation eliminates the diode reverse recovery problem.

The DCM operation of the flyback is popular because of the simplicity of control. Sinusoidal input current (after filtering the switching component) is drawn automatically if the switch duty cycle is maintained constant over one line half cycle [26].

Watson *et al* [103,104] used a flyback topology as shown in figure 8. Here, the switch S2 (with its anti-parallel diode) together with clamp capacitor C_c forms an active-snubber

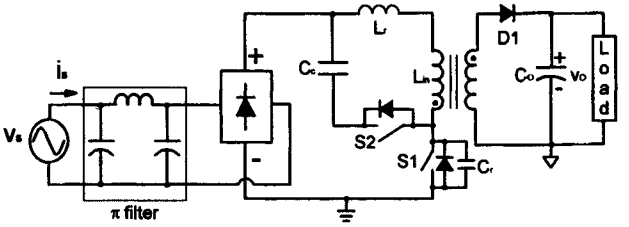

Figure 8. Flyback PFC converter with active-clamping circuit.

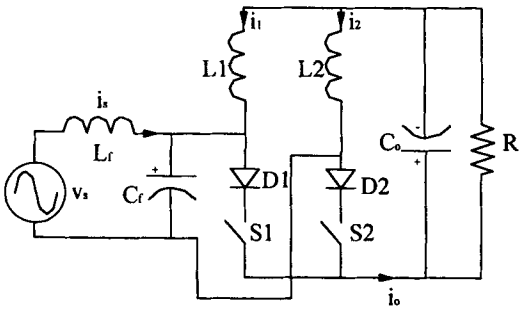

Figure 9. Power circuit of the half-bridge buck converter.

network. Due to this, the energy stored in the transformer leakage inductance L_{in} is not dissipated; instead it is recycled while minimising turn-off voltage stress across the power switch S1. Furthermore, the ZVS of switch S1 lowers output rectifier di/dt resulting in reduced rectifier switching loss and output switching noise.

(iii) Buck topology – In voltage source type buck circuits, the input voltage must be greater than the output voltage. Due to this, during certain intervals when the input voltage is less than the output voltage, no current will be drawn from the input; hence, the net input current will be nonsinusoidal. But the advantage of the buck converter is that it can provide current limit support due to the series buck switch [102].

In the application reported in references [38–40], the input voltage varies over a very wide range (130 to 600 V) but the output voltage desired is 400 V. Thus, the boost converter alone is not suitable. So, a topology with (Buck + Boost) operation is adopted to maintain the input current sinusoidal. When the input voltage is greater than 400 V, the buck operation is effective. Below 400 V, the boost operation is performed.

Unlike the voltage-source-type buck converter, the current-source-type buck PFC converter operates for all values of the input voltage drawing a sinusoidal current. To achieve this, however, the instantaneous output current has to be maintained at a higher value than the instantaneous input current.

A three-phase buck converter operating as a current-source-type PFC converter is also reported [47,48]. The application of the idea to a single-phase case is also mentioned [47,48]. References [49–51] deal with the single-phase implementation itself. Reference [51] discusses a two-switch current source type PFC circuit (figure 9) which has been derived from a half-bridge voltage source type PFC converter [45,46] based on the duality principle. Note that, in these converters, a diode must be added in series with the switch(es) to realise bipolar blocking capability; this results in additional conduction power loss. The current-source-type buck PFC converter is particularly useful in application where the output voltage must be reduced to low values, such as in a *dc* motor control or *ac-dc* rectifier with over current limit.

4.1b *Input current control techniques used in conventional PFC converters: (i) Peak current mode control* – In this constant frequency control method, the switch (peak) current is sensed and made to track the desired sinusoidal reference current [55,56,65]. The current reference is obtained by multiplying the error signal of the output voltage control loop with

the sinusoidal template obtained from the input voltage. The peak current mode control is easy to implement and has an inherent fast current limit protection. Several integrated circuits such as ML4812 [55], have been developed to implement this control.

The peak current mode control technique is not suitable for the buck and the flyback PFC topologies due to the large error between the switch peak current and the average input current which is to be controlled. The control method is however suitable for a boost converter, though there will be a "peak to average" error in this topology [56] also.

The peak current mode control technique suffers from duty cycle dependent instability ("subharmonic oscillation"). In a *dc-dc* converter, this problem can be eliminated by providing "external ramp compensation" [56]. In case of an *ac-dc* PFC converter, external ramp compensation is not very effective as the operating point, which is line and load dependent, varies over a wide range. Furthermore, providing excess ramp compensation leads to input current distortion, particularly around zero-crossings of the input voltage.

(ii) Average current mode control – By controlling the average input current instead of the peak [20,54,55,57], the subharmonic oscillation problem is avoided. Good input current wave shaping is achieved as the average line current is directly controlled. Due to the averaging filter used, the dynamic performance of the current control loop is not fast, which however is not seen as a major limitation in PFC applications. Several commercial integrated circuits such as UC3854 [54,57] are available for the implementation of this control for boost PFC converter operating in CCM.

(iii) Charge control – In charge control, the average input current is controlled on a cycle-by-cycle basis giving rise to fast current loop response. Though this technique is general, it is particularly useful for flyback PFC[35,36] where the use of average current control may not give the desired performance. As with peak current mode control, the charge control technique is also reported to exhibit subharmonic oscillation [35].

(iv) Hysteresis current control (HCC) – In this control method, the input current is made to switch within a reference current window called the hysteresis band [30,32,34,45,46,94]. There are many variations in this technique such as constant hysteresis band, and variable hysteresis band [32]. The variable frequency operation of this method is seen as one of its disadvantages as the energy storage elements including input filter may have to be sized for the lowest frequency of operation. HCC technique, however, offers several advantages such as ease of implementation, and fast and robust current control.

(v) Sinusoidal pulse width modulation control – Here, just as in inverter applications, a triangular carrier-wave is modulated with a sinusoidal modulating signal to generate the drive pulses for the switch(es) [28]. Closed loop regulation is achieved by varying the depth of modulation.

(vi) Delta modulation control (DMC) – This technique [69], which is the dual of the HCC method, is usually used with current-source-type *ac-dc* PFC converter [47,48] (see figure 9). Here, the capacitor (C_f) voltage is made to switch within a predetermined band about the reference sinusoidal voltage. For a given sinusoidal input voltage, the input current then

automatically becomes a sinusoid. The power factor of the input current can be adjusted to any value by appropriately adjusting the phase of the reference voltage. However, DMC is parameter sensitive and relatively complex leading to the proposal of the next control technique [50,51].

(vii) Inductor voltage control (IVC) – In this technique [50,51], the input inductor (L_f) voltage (figure 9) and hence the input current is controlled to follow a sinusoidal reference voltage, resulting in a significant performance improvement over the DMT, such as robustness, simplicity and direct input current control.

4.1c *Modelling of PFC converters: (i) Small signal modelling of conventional PFC circuits* – In most PFC applications, the output voltage of the PFC is dynamically regulated against load and line variations, using closed loop control. In order to design a good compensator circuit based on analysis, linear small-signal models are necessary for the power and control circuits. These models are dependent on the topology and the control technique used.

Mohan *et al* [20] present the small signal model for the boost converter operating in CCM with the load assumed to be resistive. However, in most cases, the load of a conventional PFC would be of constant power type with negative impedance characteristics. The small signal model for the boost converter with this type of load is also discussed [25,57,67,68].

(ii) Large signal modelling of PFC converters – The large signal "averaged" model can be used to obtain several steady-state results of the system easily. Besides steady-state analysis, the averaged model is very useful in efficient simulation (using SPICE, SABER etc.) of complex systems such as the PFC circuit. Both simulation time and the memory storage requirement for the output are significantly less than in the simulation using actual switches. Due to these, unlike with a switched model, the averaged model simulation can be easily run several times to optimise converter and controller performance. There are a variety of approaches to obtain an averaged model. These are dealt with in detail in other references [96–101]. The averaged model concept for PFC application is used extensively [46,51,93,94].

The "switched" model with ideal switches, despite its drawbacks such as long simulation time and large secondary storage space, is still useful and necessary in the study of switching transients and in the determination of quantities such as peak voltage and current stress of the device, duty ratio and switching frequency variations. Thus, the averaged and the switched models complement each other in their usefulness.

4.2 *Problems in conventional active PFC techniques*

All conventional PFC techniques discussed in § 4.1 suffer from some drawbacks which are discussed in this section. These form the motivation for the "Active PFC techniques with fast load dynamics" discussed in § 4.3.

4.2a *Large filter components:* Assuming the PFC converter in figure 10 to be lossless and neglecting the small energy stored within the block, it may be seen that the instanta-

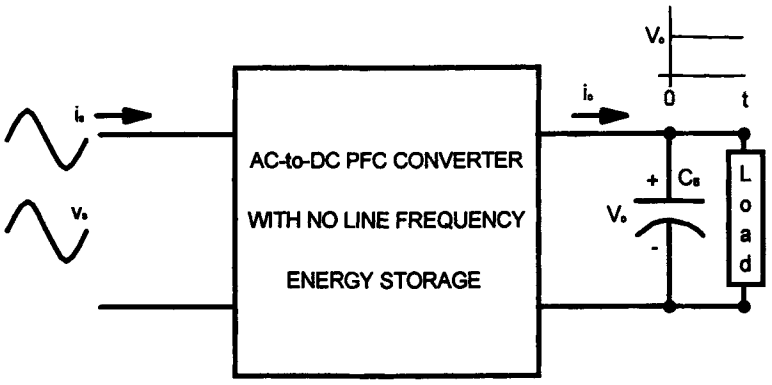

Figure 10. Input–output properties of a PFC converter.

neous input and output power must be equal. With sinusoidal input current and voltage, the instantaneous input power is a sine-squared function (figure 11) consisting of a *dc* power component plus an *ac* component with frequency at twice the line frequency. At the output port, the output voltage is regulated to a constant value and hence the load draws constant (*dc*) power only. Due to this, there must be a bulk energy storage element (such as C_B in figure 10) to absorb the second harmonic input power. The amplitude of the second harmonic power is the same as the *dc* value delivered to the load, hence requiring a large capacitor.

The second harmonic energy can also be stored in an inductor such as in current-source-type PFC converters. However, with the present technology, the size and cost of a capacitor is generally much lower than a corresponding inductor. This is the main reason for the present popularity of voltage-source PFC converters over current-source PFC converters.

4.2b *Slow output dynamics:* A typical closed loop control system for a PFC is shown in figure 12. In order to have fast dynamic response for sudden changes in line voltage and load, the bandwidth of the loop must be high. But, as the magnitude of the second harmonic voltage component at the output is quite high (even with large C_B), the control signal V_c (figure 12) will then have a large second harmonic component. However, in order to achieve a sinusoidal input current it is essential that V_c be slow varying and be

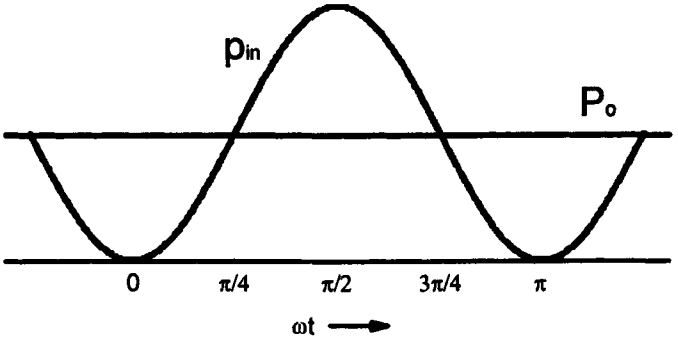

Figure 11. Input and output power waveforms.

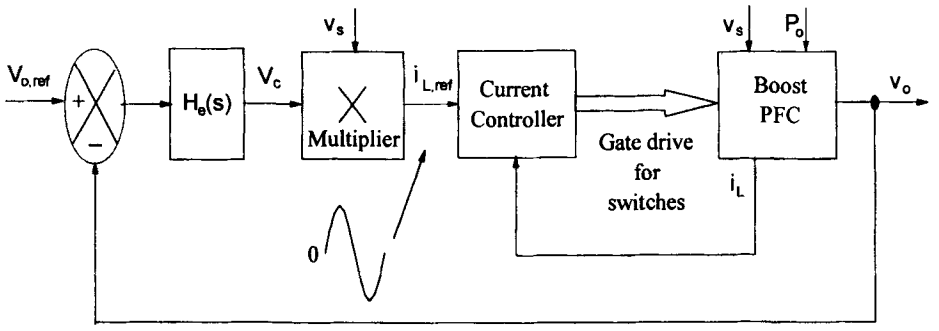

Figure 12. Block schematic of a typical closed loop system for PFC converter.

maintained constant at least over one half of the line cycle. Due to this design conflict, the requirement of fast dynamics is usually sacrificed in order to achieve good input current waveform. The typical bandwidth of the outer voltage loop will be of the order of 5–20 Hz, resulting in slow output dynamics.

Note: The response for line voltage variations, however, is usually good due to a input voltage feed-forward that is typically adopted [102].

4.3 *Active PFC techniques with fast load dynamics*

As pointed out in § 4.2, due to the existence of the second harmonic problem in conventional active PFC techniques, the output voltage-control-loop will have a poor response. Approaches to overcome this limitation are discussed in the following sections.

4.3a *Cascaded scheme:* This scheme [102] is currently very popular. Here, the conventional PFC is cascaded with a down stream *dc-dc* converter (see figure 13). The downstream converter addresses the load requirements such as providing fast dynamics, tight regulation etc., and the PFC converter meets the line requirements, thus ensuring independent control over the input and output requirements. Also, the resulting PFC arrangement is modular in construction. Several ICs are available, ML 4819 [55] for example, with the PFC and DC/DC converter control functions integrated. With all its advantages, the cascaded scheme still suffers from the following drawbacks.

(1) The rated output power is handled twice resulting in poor efficiency.

(2) Having separate full power rated modules for the PFC and the downstream *dc-dc* converter entails higher cost, weight and size.

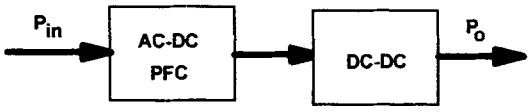

Figure 13. Power flow in a cascaded scheme.

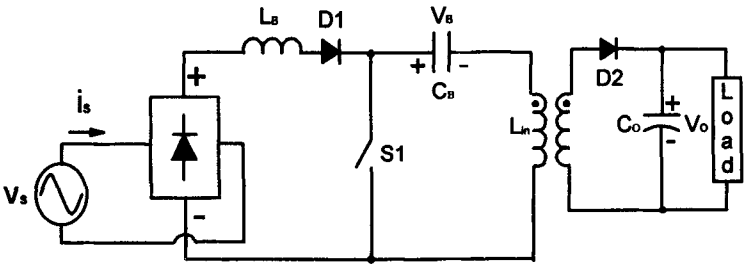

Figure 14. A single-stage PFC scheme – Boost integrated with flyback rectifier/energy storage *dc-dc* converter (BIFRED).

4.3b *Second-harmonic filtering scheme:* The dynamics of conventional PFC converters can be improved by filtering-out the second harmonic component of line frequency from entering the error amplifier stage of the control loop by using a notch filter [75,76]. The error amplifier can now be designed to have a wide bandwidth and high-gain for the low frequency range resulting in fast response. However, with the use of this technique, no corrective action will be taken by the loop for perturbations at around twice the line frequency. It must be noted that, this technique does not prevent the second harmonic of the line frequency from reaching the load; it only avoids it from reaching the control loop.

4.3c *Single-stage PFC schemes (S^2PFC):* A variety of single-stage schemes featuring tight output regulation and near-sinusoidal input current with power factor close to unity have been proposed [78,89]. Most single stage schemes, such as the BIFRED[83,86], BIBRED [83], DITHER [79] are realised by combining the two power stages of a cascaded scheme into a single power stage allowing the active switch(es) to be shared (figure 14). Because of the sharing of the switches, the control freedom is greatly reduced. Also, the voltage and current stresses of the active switches are typically much higher than those of the switches in the cascaded scheme, thereby resulting in less efficiency. Often variable frequency PWM techniques [79,82,83] or resonant techniques [80] are employed in S^2PFC scheme.

In many variable frequency PWM techniques, two control variables (say switch on-time and frequency) are still used for meeting the line and the load requirements independently. Divan *et al* [78], however, report a single-stage scheme operating with fixed frequency PWM

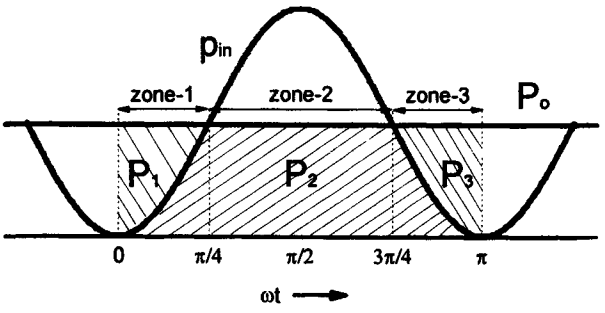

Figure 15. Input and output power waveforms to illustrate P^2PFC concept.

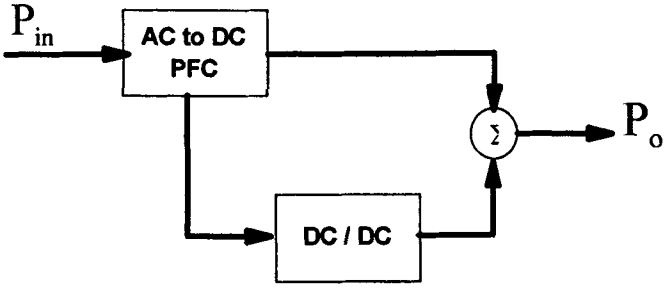

Figure 16. Power flow in a P^2PFC scheme-1.

technique. Here, a two-switch forward converter is integrated with the boost PFC. One of the switches is shared by both the converters.

Generally, single-stage schemes suffer from one or more of the following drawbacks.

(1) Suffers from all the drawbacks of DCM operation of conventional PFCs.

(2) In many cases, the voltage across the bulk energy storage capacitor is uncontrolled and can reach high values. A higher rated capacitor will result in increased cost and greater power loss due to larger ESR (Equivalent Series Resistance) values.

(3) The frequency varies in many cases over a wide range (typically 1 : 8) making the EMI filter design difficult.

(4) Increased stress on devices.

(5) Efficiency of power conversion is generally low.

(6) Complex control.

4.3d *Partially parallel PFC schemes (P^2PFC):* In figure 15, the input and output power waveforms are divided into three (time) zones. In zone-2, the input power processed by the PFC is greater than the output power demand. In a conventional PFC scheme, this excess energy flows into the output bulk capacitor or inductor. In the P^2PFC scheme, however, this excess power is diverted to a bulk capacitor (or a bulk inductor) within the system.

During zone-1 and zone-3, the input power processed by the PFC is less than the output power demand. Therefore, in order to meet the load power requirement, the excess energy stored previously in zone-2 is now released to load (through another power conversion). The sum of energy deficits during zones 1 & 3 is equal in value to the excess energy stored within the system during zone-2.

It can be shown that the average value of the excess power during zone-2 is equal to 32% of the output power P_o. Thus, in this scheme, 68% of the output power is directly fed to the load after one-time processing by the PFC stage. The remaining 32% is however

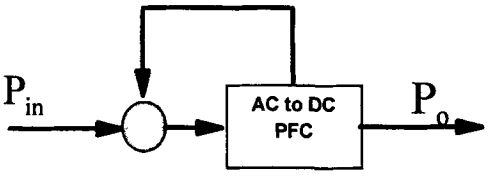

Figure 17. Power flow in a feed back type of P^2PFC scheme-2.

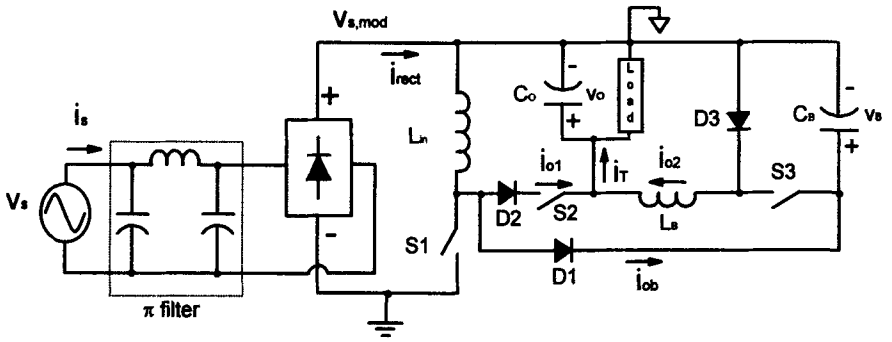

Figure 18. A PFC circuit based on P^{2}PFC scheme-1.

processed twice before it is fed to the load. As a result, the overall efficiency of such a scheme can be expected to be higher than that of the cascaded scheme. The challenge, here, lies in designing an appropriate control scheme that ensures fast output dynamics while enabling the input current to be a sinusoid with PF close to unity.

Figures 16 & 17 show two possible power flow structures that can be used to implement the P^{2}PFC concept. Several circuit implementations are possible to realise each of the power flow structures. In the circuit (figure 18) proposed [106], the *ac-dc* PFC stage is implemented using a flyback converter operating in DCM. The *dc-dc* converter stage is implemented using a buck converter. The flyback converter delivers 68% of the output power directly to the load. The remaining 32% is handled once by the flyback PFC stage and for the second time by the *dc-dc* converter stage before it is fed to the load. A few other circuit implementations conforming to the P^{2}PFC power flow structure are also reported [77,90]. Fast output dynamics is achieved by appropriately controlling the PFC stage and the *dc-dc* converter stage.

In figure 19, a circuit based on flyback topology that implements P^{2}PFC scheme-2 is shown [77,91]. Here, the PFC stage feeds the rated power to the load, but part of the output power (32%) is fed back to itself via C_B to be processed again during zones 1 and 3.

4.3e *Output shunt PFC scheme (OSPFC):* This scheme is referred to [92] as Reactive Shunt Regulator Scheme and is shown in figures 20 and 21. Here, the second harmonic power processed by the PFC stage is diverted to the *dc-dc* converter stage and the *dc* power

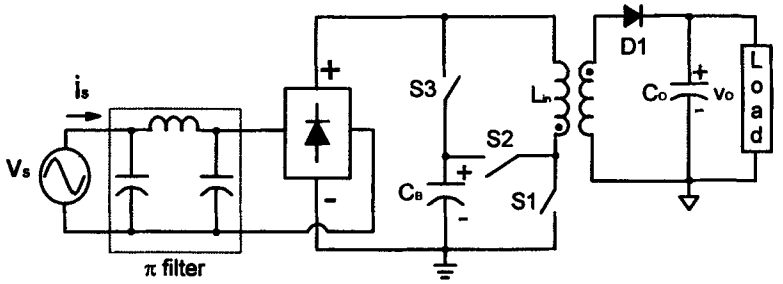

Figure 19. A PFC circuit based on P^{2}PFC scheme-2.

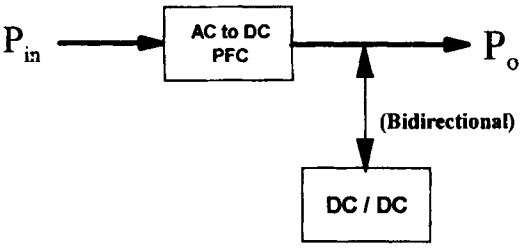

Figure 20. Power flow in OSPFC scheme.

is fed to the load. It is easy to see that in this arrangement, the *dc-dc* stage processes 64% (i.e. $2 \times 32\%$) of P_o while the PFC stage processes full power P_o. Hence, the improvement in efficiency over the cascaded scheme may not be significant.

4.3f *Input-shunt PFC schemes (ISPFC):* Unlike the OSPFC scheme, the shunt converter here is an *ac-dc* bi-directional converter and it is located at the *ac* input side. The literature reports two approaches for the ISPFC scheme which are discussed in the following paragraphs.

(i) Scheme-1 – This scheme (figure 22) has been in use for several years in large power systems for harmonic elimination [60–64]. However, this can be successfully used for correcting the power factor of small systems also[64]. The off-line converter in the main power flow path draws the well-known nonsinusoidal current (see figure 1b). In order for the net input current to be sinusoidal, the *ac-dc* shunt PFC stage is made to draw a current which is the difference of the desired sinusoidal input current and the off-line converter's input current. It must be noted that the PFC stage does not process any active power; it only handles the harmonic power. Because of the high value of the peak input current drawn by the off-line converters, the *ac-dc* PFC stage should be designed to handle high current stress.

(ii) Scheme-2 – This scheme [94,106], consists of a cascaded scheme paralleled at the input with an off-line converter (figure 23). With this arrangement, the net input current is

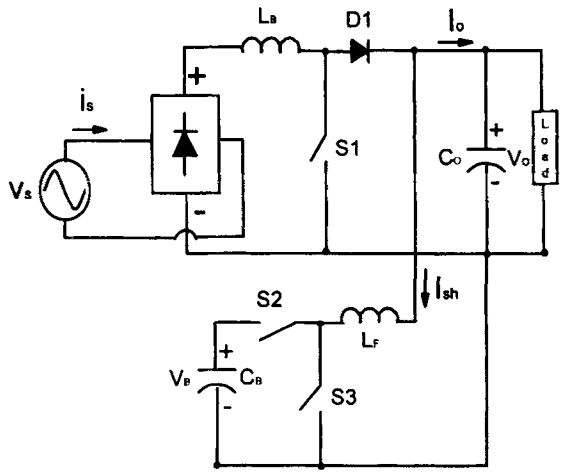

Figure 21. A circuit implementation of OSPFC scheme.

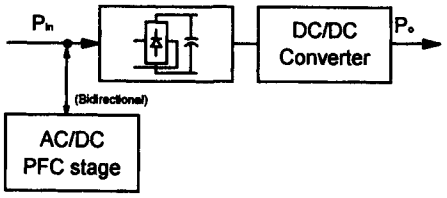

Figure 22. Input-shunt PFC scheme-1

controlled in such a way that it is sinusoidal and in phase with the input voltage. Therefore, (as in scheme-1) the current drawn by the PFC stage will be the difference of the sinusoidal input current and the narrow and peaky current drawn by the rectifier–capacitor front-end. Again, as in scheme-1, the *ac-dc* PFC converter here handles bi-directional power flow. However, as it also processes active power, the peak current stress here is relatively low [94,106]. For a certain range of power sharing between the two parallel paths, this scheme may result in a better efficiency than the cascaded scheme [94,106].

At the output, the *dc-dc* converters #1 and #2 may each be supplying independent loads (figure 23a), and may each have multiple output voltage levels. However, for the case when there is only one load, the outputs of the two *dc-dc* converters may be paralleled to feed the load (figure 23b). For ensuring stable parallel operation, current-mode control technique may be used in the *dc-dc* converters. The sharing of the load power may also be programmed using this control technique.

4.3g *Fully parallel PFC scheme (FPPFC):* A fully parallel PFC scheme is proposed [93] in which a PFC stage is paralleled, both at the input and the output, with a conventional off-line *ac-dc* converter with rectifier–capacitor front-end (figure 24). The power flow is shared between *dc-dc* converter and *ac-dc* PFC stage. Thus, the overall power is processed once only. Due to this arrangement, the net input current is nonsinusoidal; though the PFC stage draws a sinusoidal current, the off-line converter draws the well-known narrow and spiky currents. The main aim in this scheme is to only contain the line current harmonics within the agency specified limits rather than achieving a high power factor. At the output, fast dynamics is achieved by using the off-line converter to cancel the second harmonic component injected by the PFC stage. Here again, it is shown that a 68% power sharing by the PFC stage and 32% power sharing by the off-line converter results in good performance. This technique may prove to be economical for lower power levels.

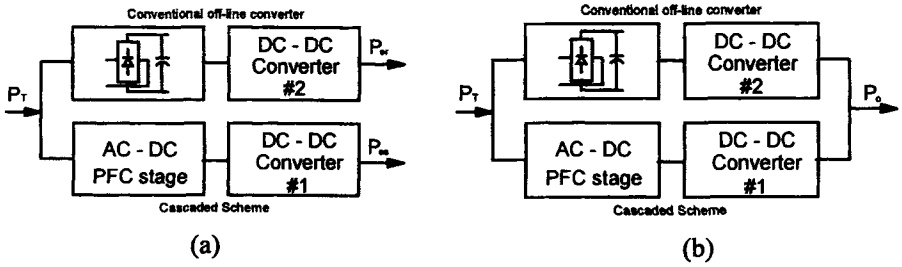

Figure 23. Input-shunt PFC scheme-2 (ISPFC-2). **(a)** Independent loads. **(b)** Outputs paralleled.

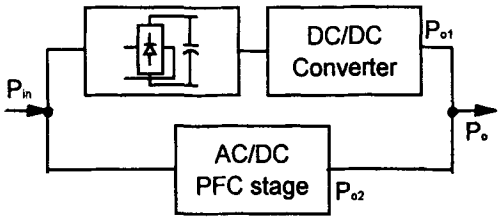

Figure 24. Block diagram of a fully parallel scheme (FPPFC).

5. Active–passive PFC techniques

As the name indicates, active–passive PFC involves the combination of active and passive techniques for PFC/harmonic reduction. The main motivation for this technique is improvement of efficiency (over the cascaded scheme) and possible size and cost reduction.

The input currents of the active–passive schemes reported so far[70–71], are not pure sinusoids. The attained PF though low (0.75 to 0.9) is, however, significantly higher than the conventional off-line converter with rectifier–capacitor type interface. Active–passive scheme can be used for applications where the main aim is to contain the line current harmonics within the agency specified limits rather than achieving a high power factor. This technique may prove to be economical for lower power levels.

In the scheme by Elmore *et al* [70], a conventional boost PFC is provided with a bypass passive path consisting of the boost inductor, boost output diode and the output capacitor. The boost switch is not operated around the line voltage peaks; during this interval, the passive path conducts. A simple open loop control is adopted [70], which results in large output voltage variations and uncontrolled power sharing between the two parallel paths.

Oruganti & Thean [71] suggest a loop control scheme, in which both the output voltage and the power sharing are directly controlled. The control scheme, however, is somewhat complex. The merits and demerits [71] of the active passive scheme is given below.

(1) The diode reverse recovery loss problem, occurring in a boost converter, which is maximum around the line voltage peaks is now reduced. Hence, efficiency is improved. Or else, for a given efficiency, the switching frequency can be pushed higher to achieve cost and size reduction.

(2) Reduced EMI as the line current wave form does not have any switching current component around the peaks.

(3) Input current is non-sinusoidal and hence higher harmonic content. Power factor is also poor when compared with the conventional PFC.

(4) Does not alleviate the problem of slow output dynamics. Thus the active–passive PFC stage must be further cascaded with a *dc-dc* converter.

(5) Not suitable for universal input voltage range as the output voltage varies with *ac* input voltage magnitude.

6. Conclusions

As seen in the paper, the research activities in the area of single-phase PFC can be identified as falling under three categories: (1) Passive PFC technique, (2) active PFC technique, and

(3) active–passive PFC technique. Passive PFC techniques result in significant improvement in PF and harmonic performance compared to the rectifier–capacitor type interface. However, in general, these are not superior compared to what is achievable using active PFC techniques. It is stated in many publications that passive PFC technique does not offer cost, size, and weight benefits. However, such a statement is very general. This is because, if the main aim is to contain the line current harmonics within the agency specified limits and not improvement of PF *per se*, then the passive PFC technique may prove to be a better choice for lower power levels (<200 W). A designer must investigate this aspect further for his/her specific application.

The work in active PFC technique was classified in two ways, in this paper: (1) Conventional active PFC (poor output dynamics); (2) Active PFC with fast output dynamics.

The conventional PFC circuits interface well with the utility supply in terms of high PF (near unity) and reduced harmonics. However, they cannot be used to feed loads that require fast output dynamics. Several alternative PFC schemes to overcome this problem, such as cascaded, S^2PFC, P^2PFC, OSPFC, ISPFC, and FPPFC have been reported. In all these the primary aim of the researchers has been to achieve one or more of advantages such as (1) improved performance, (2) higher efficiency and (3) cost, size and weight benefits.

The work reported in active–passive PFC schemes is not extensive. Schemes have been reported in which an active PFC path is paralleled with a passive rectifier to realise several advantages such as increased efficiency, reduced EMI, and increased switching frequency.

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