Application of Au-Sn Eutectic Bonding in Hermetic Radio-Frequency Microelectromechanical System Wafer Level Packaging

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Development of packaging is one of the critical issues toward realizing commercialization of radio-frequency–microelectromechanical system (RF-MEMS) devices. The RF-MEMS package should be designed to have small size, hermetic protection, good RF performance, and high reliability. In addition, packaging should be conducted at sufficiently low temperature. In this paper, a low-temperature hermetic wafer level packaging scheme for the RF-MEMS devices is presented. For hermetic sealing, Au-Sn eutectic bonding technology at temperatures below 300°C is used. Au-Sn multilayer metallization with a square loop of 70 μm in width is performed. The electrical feed-through is achieved by the vertical through-hole via filling with electroplated Cu. The size of the MEMS package is 1 mm × 1 mm × 700 μm. The shear strength and hermeticity of the package satisfies the requirements of MIL-STD-883F. Any organic gases or contamination are not observed inside the package. The total insertion loss for the packaging is 0.075 dB at 2 GHz. Furthermore, the robustness of the package is demonstrated by observing no performance degradation and physical damage of the package after several reliability tests.

Key words: Radio-frequency–microelectromechanical system (RF-MEMS), wafer level packaging, Au-Sn bonding, hermeticity

INTRODUCTION

Compared with more mature MEMS technology fields, radio-frequency–microelectromechanical system (RF-MEMS) technology is relatively new, but has already shown great promise for improving the performance and integration of the RF front-end module in wireless systems. By incorporating MEMS-based fabrication technologies into RF systems, numerous novel RF-MEMS devices have been developed and reported. Some of these devices include switches, filters, tunable capacitors, inductors, transmission lines, and resonators. These RF-MEMS devices not only reduce the size and power consumption substantially, but also have superior RF performances in comparison with current MEMS technologies.[1]

(Received October 24, 2005; accepted November 21, 2005)

Recently emphasis of RF-MEMS research has been shifted to the system integration, reliability, and packaging. Among them, development of RF-MEMS packaging technology is one of the most critical issues, because packaging determines the cost, size, and reliability[2,3] of the device. Design of the package should meet the requirements of different RF-MEMS specific functions, and these requirements are very stringent. The RF-MEMS package should provide environmental protection, and also meet the requirements of good RF response such as low insertion loss, low return loss, and high isolation. The RF-MEMS package may also need to be hermetically sealed to prevent the penetration of moisture and contamination, which frequently cause the stiction and corrosion problems of the devices.[4] Also, the packaging should be conducted at sufficiently low temperature (typically below 350°C) so that metallization and other materials of

the RF-MEMS device are not adversely affected. The package must be designed to minimize the mechanical deformation of the MEMS structure that is mainly induced by thermal expansion mismatch between the packaging materials and devices.[5] Wafer level packaging (WLP) is a very promising candidate for RF-MEMS packaging due to the lower cost and higher volume throughput relative to the component level packaging.[6] Wafer level packaging also offers key advantages in terms of miniaturization and system integration. However, long-term reliability of WLP is still one of the critical concerns. Therefore, a low-temperature, hermetic, and reliable WLP technology is required for the RF-MEMS devices.

There are generally three types of bonding technology used in WLP: direct bonding, which is also called fusion bonding; anodic bonding; and intermediate layer bonding.[7] Each bonding technology has its own characteristics and should be selected according to the applications. Fusion bonding requires a high process temperature that cannot be applied to the RF-MEMS. Anodic bonding is restricted to bond the glass with silicon, and a high electric force is not compatible for active devices. There are three types of intermediate layer bonding: eutectic bonding, adhesive bonding,[8] and glass frit bonding.[9] Adhesive bonding and glass frit bonding are available for low temperature, but have the problems of outgassing and contaminations. Although many advanced packaging technologies have been developed to perform a reliable bonding at low temperature, such as surface activated bonding,[10] localized bonding,[11] and gold-gold thermocompression bonding,[12] at present, eutectic bonding is still the most common packaging technology. The choice of materials for eutectic bonding is based on the optimization of a series of properties such as wettability, melting temperature, mechanical properties, coefficient of thermal expansion, and fatigue life. The Au-Sn metallization system has been used for flip-chip bonding in many applications such as optoelectronic packaging and RF device because of its high yield strength, good thermal conductivity, and wetting behavior, especially in fluxless application.[13,14] In particular, Au-20wt.%Sn that has a melting point of 280°C is considered to be suitable for MEMS packaging.

In this paper, a hermetic WLP scheme for RF-MEMS devices is presented. A fluxless Au-Sn multilayer eutectic bonding technology in a relatively low temperature is applied to achieve hermetic sealing, and the packaging structure with through-wafer interconnection is also used. The fabrication process is described, and the performance tests are conducted to evaluate the packaging. The robustness of the package is also confirmed by several tests such as the hermeticity test, shear strength test, and reliability tests.

PRINCIPLES OF Au-Sn BONDING

The Au-Sn solder system is selected as the sealing material for the hermetic RF packaging structure.

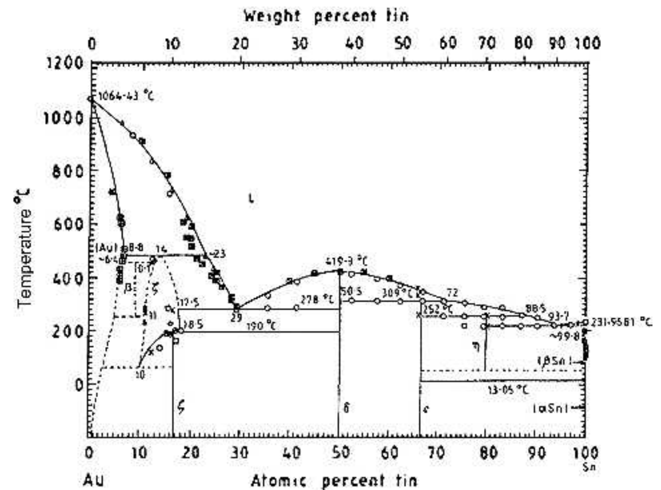

Fig. 1. Au-Sn equilibrium plhase diagram.[15]

Figure 1 shows the binary equilibrium phase diagram of the Au-Sn system.[15] It contains four different stable intermetallic compounds (IMCs) between Au and Sn at room temperature: Au_5Sn, AuSn, $AuSn_2$, and $AuSn_4$. Among them, Au_5Sn or eutectic 80wt.%Au and 20wt.%Sn composition with a melting point of 280°C is known to be the most appropriate composition for the high bonding quality because of its high melting temperature, good creep behavior, and good corrosion resistance.[16]

Figure 2 shows the design of the multilayer Au-Sn composite structure used in this study. Different multiple layers of metallization are sputtered on the silicon cap wafer and the silicon bottom wafer. For the cap wafer, Ti and Ni are first deposited on the silicon wafer followed by the deposition of Au, Sn, and outer Au, as shown in Fig. 2a. The Ti layer enhances adhesion with the silicon substrate, and Ni acts as a diffusion barrier and wettable layer between the substrate and solder metallization. Since Sn is quite easy to oxidize even under ambient conditions, an extra Au layer on the top surface is

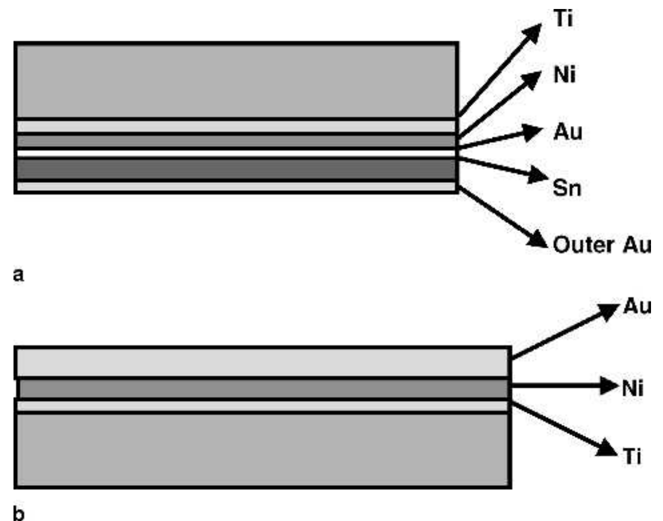

Fig. 2. (a) and (b) Schematic view of multilayer Au-Sn composite structure design.

necessary as the barrier layer to prevent oxidation of Sn. Also, deposition of Au-Sn-Au combination is performed sequentially in one high vacuum cycle in order to prevent oxidation of the Sn layer during the bonding process. For the bottom wafer, the Ti-Ni-Au composite structure is sequentially deposited on the silicon wafer, as shown in Fig. 2b. The relative thickness of Au and Sn is designed such that if all of the joining materials at the interface form a uniform joint, this composite will form a uniform alloy of 80wt.%Au-20wt.%Sn.

During the bonding process, two wafers are brought into contact with a static pressure force, and heated at a peak temperature of 280°C, which is higher than the melting point of pure Sn (232°C). Consequently, the pure Sn layer at the interface melts first, the molten Sn has an intimate contact with the Au layer and dissolves Au layer on both sides, and a series of IMCs could form according to the phase diagram. As the entire joint is heated at the peak temperature, Au and Sn at the joint will continue to diffuse into each other due to the concentration gradient. The entire process is considered to be a combination of chemical reaction and physical interdiffusion. To achieve a uniform concentration distribution at overall joint, a relatively long dwelling time at peak temperature is necessary to ensure sufficient interdiffusion and chemical reaction between Au and Sn. The bonding is performed under vacuum or in an inert gas environment to prevent oxidation of Sn and thus the entire process is flux free.

PACKAGE DESIGN AND FABRICATION

Figure 3 shows the schematic view of the packaging structure developed in this study. The size of the package is 1 mm × 1 mm and it is around 700 μm in height. The cap wafer and bottom wafer will be hermetically sealed with each other through a closed square loop of Au-Sn eutectic solder. A 4-in. high-resistivity silicon (HR-Si) wafer with a resistivity over $2.0 \times 10^4\ \Omega \cdot \mathrm{cm}$ is used for both wafers in order to reduce the attenuation of the RF signal and improve the isolation characteristics between the vias. The thickness of both wafers is 350 μm. The

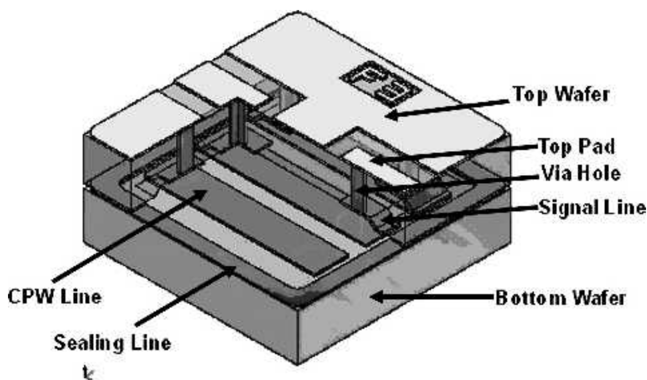

Fig. 3. Schematic three-dimensional view of RF package developed in this study.

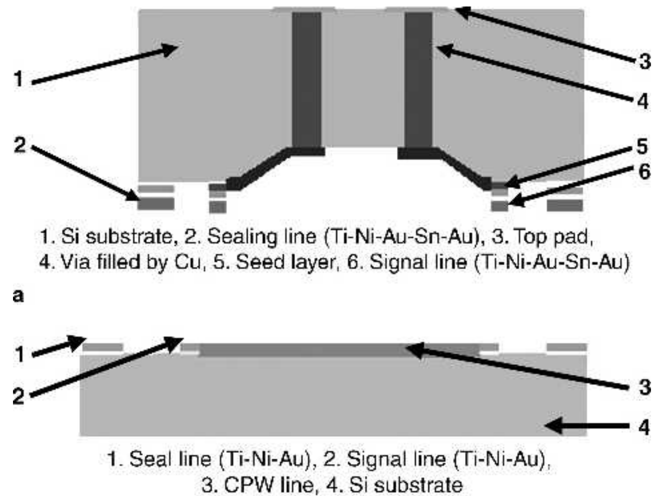

Fig. 4. Schematic cross-sectional view of the RF-MEMS package structure developed in this study: (a) cap wafer and (b) bottom wafer.

cap wafer, shown in Fig. 4a, contains the cavity, the vertical feed-through holes, and the top pads for electrical connection. The bottom wafer in Fig. 4b has the coplanar waveguide (CPW) lines and the signal lines.

Figure 5 shows a brief description of the fabrication process flow for the cap wafer. At first, 5,000 Å thick SiO_2 is formed on the silicon wafer using the thermal oxidation process as a photolithography mask for via definition. Then, the shallow cavity with a depth of 20 μm is made by the TMAH wet

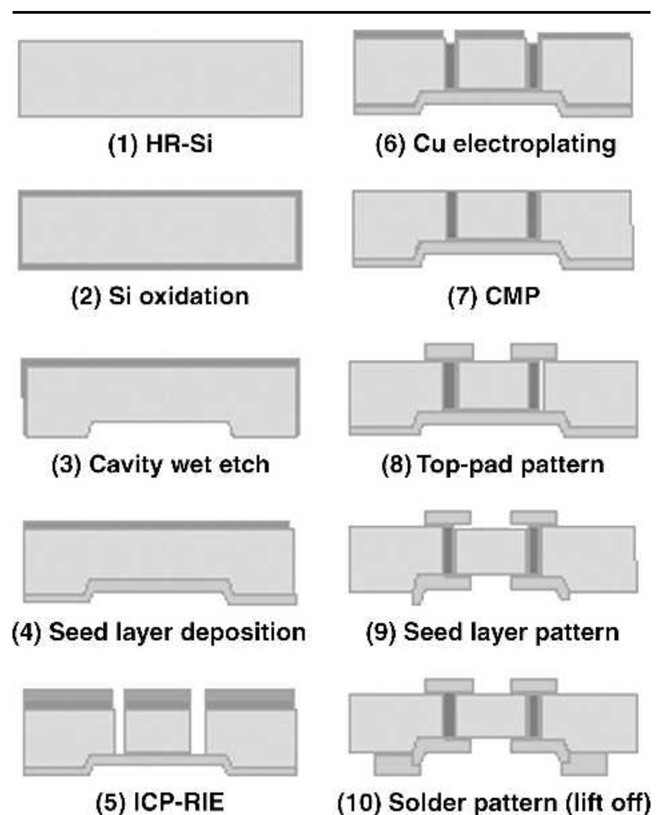

Fig. 5. Cap wafer fabrication process flow.

etching process to ensure the internal space for the RF-MEMS device. The Cr/Au layer is sputtered on the cavity side of the wafer as the adhesion layer and the seed layer for later via filling process by Cu electroplating. The thicknesses of Cr and Au are 500 Å and 2 μm, respectively. In order to achieve the small size package with low loss and low parasitic capacity, electrical feed-through of the cap wafer is achieved using a through-wafer interconnection. Through-hole via is fabricated with the inductively coupled plasma–reactive ion etching (ICP-RIE) dry etching process. The SF_6 and C_4F_8 are used as the etching and passivation gas, respectively. An approximate etch rate of 4.0 μm/min. could be achieved for the via with a diameter of 40 μm and a depth of 300 μm. After the ICP-RIE process, the oxygen plasma ashing process is performed in order to remove residual contamination inside the via hole. Metallization of the via hole is extremely challenging due to its high aspect ratio. The electroplating process has been accepted as one of the preferred methods for the deep via filling.[17] Since Cu has been widely used as an interconnection material because of its lower electromigration and resistance, capacitance time delay compared with Al, Cu electroplating is selected in this study.

To obtain the flat surface and co-planarity between the filled via hole and the wafer, a chemical mechanical polishing process is applied after Cu electroplating. Afterward, the Ti-Ni-Au metal layer was sputtered onto the top surface and patterned to make the top pads for electric connection. Therefore, the signal exchange between the internal and external circuits is through the top pads and the metallized via hole. Then, solder materials for the bonding are deposited onto the patterned seed layer of Cr/Au. A combination of Ti-Ni-Au-Sn-Au metallization is co-evaporated in sequence. The thickness of Ti-Ni-Au-Sn-Au metallization is designed as 0.1 μm, 0.2 μm, 0.07 μm, 2.9 μm, and 0.08 μm, respectively. The lift-off process is applied to pattern the seed layer as well as each bonding layer. The width of the sealing line is 70 μm. Similar to the sealing line, the interconnection between the via hole of the cap substrate and the bottom substrate is also achieved by Au-Sn solder, which is the signal line shown in Figs. 3 and 4.

For the bottom wafer, a Ti-Ni-Au combination structure is deposited and patterned in accordance with the sealing and interconnection areas of the cap wafer. In addition, the CPW line is fabricated on the bottom wafer instead of the RF-MEMS device in order to test the RF performances of the package itself. To form the CPW line, 500 Å thick Cr layer and 2-μm-thick Au layer are sequentially evaporated on the bottom wafer. The CPW line has the characteristic impedance of 50 Ω. The width of the CPW line is 150 μm and the spacing between the CPW lines is 90 μm. Design and simulation of the CPW line are performed using an Ansoft high-frequency structure simulator (ansoft Corporation, Pittsburgh, PA).

After the fabrication of the cap and bottom wafer, bonding of both wafers is conducted in a wafer level with a commercially available eutectic bonder (TPS-2000A, BNP Science, Sioul, Korea). Both wafers are aligned and brought into contact. The bonding is conducted with a static pressure of 4.5 MPa related to the solder patterning area in a nitrogen atmosphere. Based on the experiments conducted in this study, the optimal temperature profile for the Au-Sn bonding process is shown in Fig. 6. The bonded wafer is heated to a peak temperature of 280°C with a dwelling time of 20 min. Afterward, the wafer is cooled to room temperature using N_2 gas blowing for solidification of the solder joint. Finally, the bonded wafer is diced into individual square chips of 1 mm × 1 mm size.

RESULTS AND DISCUSSION

To evaluate the quality of the bonding fabricated, a scanning electron microscope (SEM) equipped with energy-dispersive x-ray microanalysis (EDAX) was used. In addition, several tests and measurements were performed, which include the shear strength test for mechanical properties measurement, insertion loss measurement for RF characteristics, helium leak rate measurement, and residual gas analysis (RGA) for hermeticity test. As a final step, several reliability tests were also performed to investigate the performance and robustness of the package.

Microstructure Observation

The quality and reliability of eutectic bonding strongly depends on the microstructure formed in the bonding joint. Since the entire process is flux free, surface cleaning before the bonding process is necessary as the bonding quality strongly depends on surface condition. For example, the oxide layer on the top surface and contaminants that are introduced during the bonding process will generate the defects at the interface and result in degradation of the bonding quality.

If there is no additional process except conventional wet cleaning before the bonding process, large voids of around 1–2 μm in diameter were detected at the joint interface, as shown in Fig. 7. The voids are generally located near the Au layer of the bottom wafer, which indicated the source of the voids to be Au surface

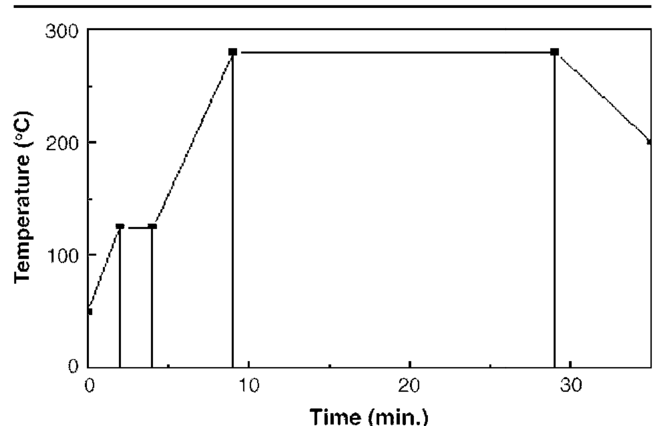

Fig. 6. Bonding temperature profile.

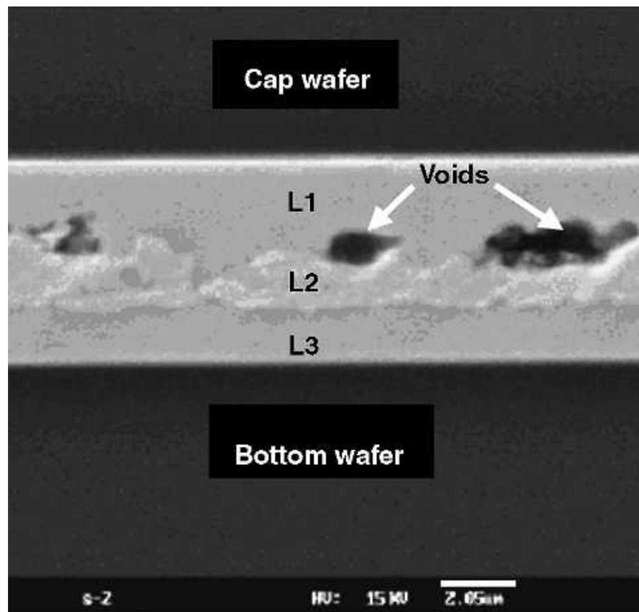

Fig. 7. SEM image of a cross section of the bonding layer for the sample without surface treatment before bonding.

contamination of the bottom wafer. Also, existing contamination will block the interdiffusion process between Au and Sn; therefore, three sublayers, which represent three different phases, could be detected along the joint area; they are marked as L1, L2, and L3, respectively, in the picture. The composition in different sublayers had been detected by EDAX, as listed in Table I. L1 and L3 are mainly Au-Sn intermetallic compound with ternary Au-Sn-Ni. L2 is an Au-rich layer. According to the EDAX result and phase diagram, it is concluded that the major compositions of the three sublayers are as follows:

L1: Au_5Sn (ζ phase), AuSn (δ phase) with ternary Au-Sn-Ni
L2: Au_5Sn (ζ phase)
L3: $AuSn_2$ (ε phase) with ternary Au-Sn-Ni

This result indicates that the interdiffusion between Au and Sn is not sufficient enough during the bonding process, resulting in a nonuniform alloy along the solder interface.

Table I. Detailed Composition of Each Layer in the Bonding Interface

Layer	Element	wt.%	at.%
L1	Ti	0.0579	0.1935
	Ni	3.0875	8.4252
	Sn	23.4921	31.7098
	Au	73.3625	59.6715
L2	Ti	—	—
	Ni	0.3193	0.9994
	Sn	9.7611	15.1122
	Au	89.9196	83.8884
L3	Ti	—	—
	Ni	10.0595	22.1622
	Sn	43.3539	47.2454
	Au	45.5866	30.5924

The O_2 plasma ashing or cleaning is considered to be an effective way to remove the oxide layer and organic contaminants to get a clean surface. In addition, it was reported that sufficient surface activation such as O_2 plasma ashing would have no direct effect on the bonding strength.[18] Therefore, O_2 plasma ashing was conducted before the bonding process. Figure 8 presents the magnified picture of the microstructure of the joint for the sample with O_2 plasma ashing before the bonding. Void-free structure is obtained within the solder layer. Also, the microstructure of the solder layer is considered to be uniform because no extra phase or layer could be detected within the entire solder layer. The EDAX result indicated that the composition of the bonding layer is only AuSn. The cross-sectional view of the well-bonded package is shown in Fig. 9. Void-free structures in the bonding interfaces and within the via holes are observed; therefore, a hermetic sealing of the packaging is expected.

Shear Strength

One of the most important mechanical properties for evaluation of the bonding quality is the bonding strength or toughness. High bond strength is always required for the packaging structure since mechanical support is one of the basic functions of the package. Shear strength measurements for the diced package samples were carried out by a commercially available shear tester (Royce 552–100 K, Royce Instrument, Napa, CA). The shear strength value measured for 20 different samples ranged from 44.7 MPa to 65.8 MPa, and an average value of 51.7 MPa was obtained. During the shear test, failure always occurs at the UBM layer, which in Ti-Ni indicates that bonding strength is stronger than UBM layer adhesion. According to MIL-STD-883F, for die shear strength failure criteria, the die of area smaller than 5×10^{-4} in.^{2} (or 0.32 mm^2) shall withstand a minimum force of 0.04 kg/10^{-4} in.^{2} (or 6.1 MPa).

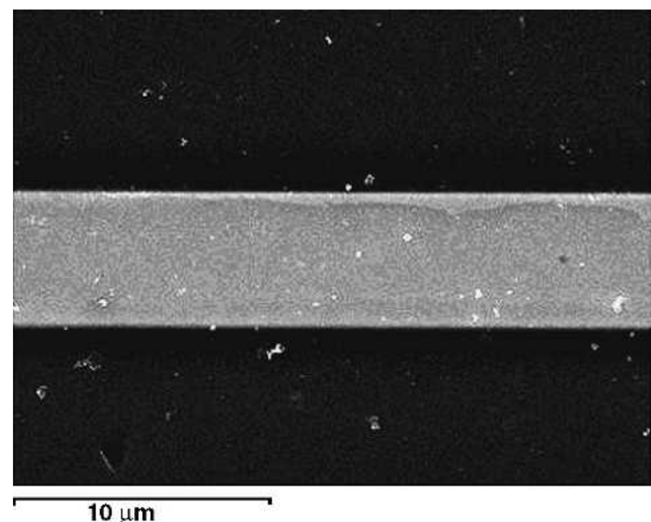

Fig. 8. SEM image of a cross section of the bonding layer for the sample with O_2 plasma ashing before bonding.

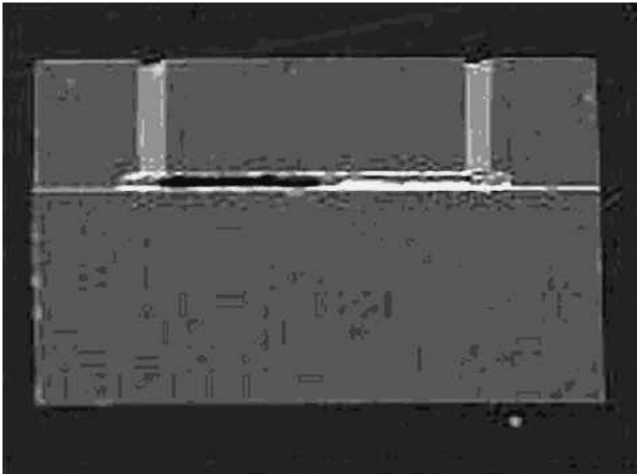

Fig. 9. Cross-sectional view of the RF-MEMS package after bonding and via hole filling.

In this study, the total sealing area of one chip is 0.289 mm^2, so a strong bond is confirmed by the shear strength test.

Insertion Loss

For evaluation of RF-signal transmission characteristics of the RF-MEMS device, the insertion loss could be representative for RF performance. Packaging should also be designed to minimize the insertion loss as low as possible. In this study, RF characteristics of the RF packaging were measured with the CPW line instead of the RF-MEMS device. The RF measurement of the MEMS package in this study is performed using an HP 8510C Vector Network Analyzer, GGB Picoprobe 250-μm pitch coplanar, and GGB CS-5 SOLT (short-open-load-through) calibration standard. The insertion loss was measured by HP 8510C Network Analyzer Probe Station (Hewlett-Packard, Palo Alto, CA) in which the frequency was swept from 0.5 GHz to 10 GHz. Figure 10 shows the insertion loss before the bonding, which corresponds to the insertion loss of the CPW line,

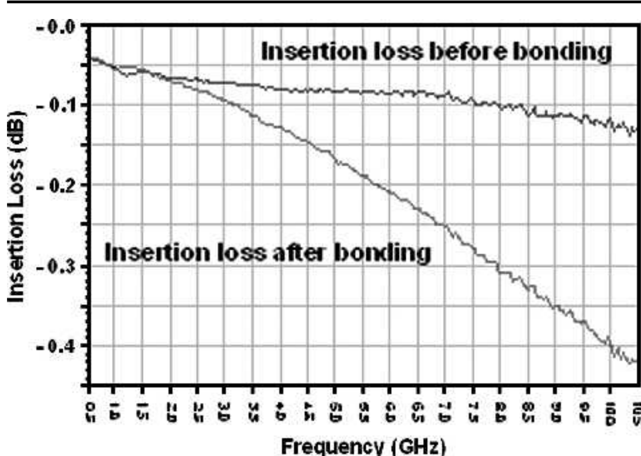

Fig. 10. Result of insertion loss measurement. Insertion loss after bonding indicates the total insertion of the package.

and the total insertion loss after the bonding, which is the sum of the package loss and CPW line loss. The measurement results indicate that a total insertion loss is around 0.075 dB at 2 GHz, and the insertion loss for the packaging itself is very small. This result showed that the RF signal could be well transmitted under acceptable loss.

Hermeticity Test

Hermeticity of the packaging is characterized by measuring the leakage rate. The leakage rate was measured with a helium leak detector of Alcatel DGC-1001 that has the detection limitation of 2×10^{-11} atm·cc/sec. Since the packaging structure in this study has a cavity volume of only $600 \times 600 \times 30$ μm^3 (or 1.08×10^{-5} cc), which is too small to be used with a helium leak detector, a specific test vehicle, which has the similar structure as the packaging used but in a large cavity size of $0.5 \times 0.5 \times 0.05$ cm^3 (1.25×10^{-2} cc), was fabricated only for the hermeticity test. In a specific test vehicle, the width of the sealing line of the Au-Sn solder is the same as that of the original package, which is 70 μm. The leak rate test showed a maximum equivalent leak rate of 1.58×10^{-8} atm·cc/sec, which is below the failure criteria of 5.0×10^{-8} mbar·L/sec (or 4.94×10^{-8} atm·cc/sec) described in the MIL-STD-883F specification.

In addition, RGA is performed for the analysis of gas and vapor species inside the sealed cavity. Outgassing or gas generation caused during the bonding process or the desorption of gas molecules absorbed on the surface inside cavity will degrade the performance of the RF-MEMS device such as the resonator and the RF switch.[4,19] Therefore, outgassing inside the cavity should be minimized. The RGA was done using temperature-programmed desorption–mass spectrometry (TPD-MS). After the chip was placed in a vacuum chamber, the cavity was opened by breaking the cap wafer covering the cavity, and the released gases from the cavity were sequentially analyzed by a mass spectrometry. Due to the measurable detection limitation of the mass spectrometry, three chips were placed in a vacuum chamber and broken at the same time. The gas generated from the three chips was measured and finally averaged for calculation. As shown in Fig. 11, gases released from the cavity are N_2 (95.9%), H_2O (1.6%), O_2 (1.0%), and Ar (1.5%). Among them, N_2 is the main gas released. It is thought that N_2 originated from the N_2 environment in the bonding chamber during the bonding process. Since N_2 is considered to be an inert gas, the effect of N_2 gas on packaging reliability can be negligible. H_2O is considered to be environmental moisture, and O_2 and Ar should come from the wafer surface, which was absorbed during fabrication (for example, plasma ashing) before bonding. Any other contamination or organic gases were not detected. However, it is not clear at this stage how much residual gas such as H_2O and O_2 detected will influence

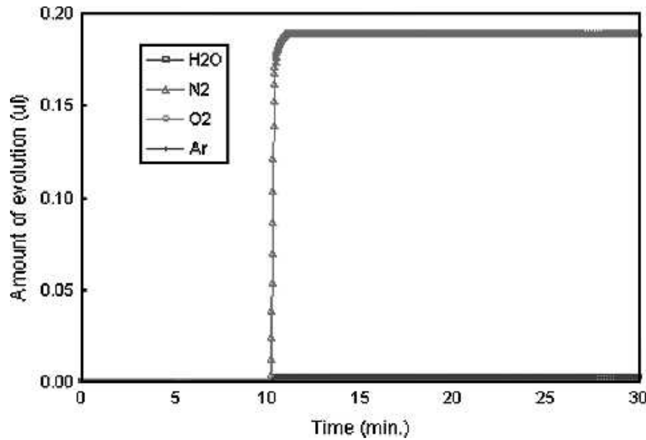

Fig. 11. Amounts of gas evolution inside the cavity measured with TPD-MS for the RF-MEMS package.

the performance of the RF-MEMS device. However, the amount of gas is much smaller compared to the total volume of internal gas, and these gases are supposed to be easily eliminated by the prebaking process of the wafer in a vacuum oven, which was stated by several studies.[20,21] In conclusion, we could expect a good quality of the hermetic packaging for RF-MEMS devices.

Reliability Test

Reliability requirements differ significantly from application to application. For application to mobile phones, the critical issues involve mechanical stress factors (e.g., vibration and shock) and environmental factors (e.g., temperature + humidity and temperature cycling). Extensive reliability studies were performed to demonstrate the robustness of the packaging.

For each reliability test, a total of ten package samples were tested. For the thermal shock test, the samples were subjected to temperature cycling, which is −40°C (20 min.) ↔ 85°C (20 min.) for 50 cycles. The high humidity storage test, which is 85°C, 85% RH for 120 h, the high-temperature storage test, which is 125°C for 168 h, and the pressure cooker test (PCT), which is 121°C, 100% RH, 2 atm for 96 h, were also performed. Any significant changes in the shear strength and insertion loss were not observed after the reliability tests, indicating no degradation of joint properties. Shock resistance was also measured with a free drop test. The free drop test setup consists of a falling metal block of 150 g weight with mount for the sample and a vertical guiding rod. A total of ten individual samples were dropped from 152-cm height to a hard surface floor. The block with the sample was dropped to the floor 3 times in a row with 6 (x, y, z, −x, −y, and −z) orientations, with one extra drop in the final; the sample was dropped a total of 19 times. This is a common qualification test for the components of the mobile phone. Any performance degradation and physical damage in the solder joint were not observed after the drop test.

CONCLUSIONS

In this paper, we presented a low-temperature hermetic wafer level packaging scheme for RF-MEMS devices, which uses the standard micromachining technology. For hermetic sealing, a Au-Sn multilayer metallization with a close square loop of 70 μm in width was sputtered onto the cap wafer and bottom wafer as a soldering system. In order to achieve the smaller package with low loss, electrical feed-through of the cap wafer was achieved by the vertical through-hole via. Void-free structures in the bonding interfaces and within the via holes could be obtained. A total insertion loss of the package including the CPW line is around 0.075 dB at 2 GHz, and insertion loss for the packaging itself is very small. The average value of the shear strength is 51.7 MPa. Helium leak testing indicated that the leak rate of the package meets the requirements of MIL-STD-883F, and the RGA test showed that any contamination or organic gases were not detected, except small amounts of H_2O and O_2, which could be easily eliminated by the prebaking process. In order to validate the above results, several reliability tests such as thermal shock, high-temperature storage, pressure cooker test, and drop test were performed. Any physical damage to the package was not observed after several reliability tests, which demonstrates the robustness of the package.

ACKNOWLEDGMENTS

We thank the RF device project team of SAIT for supporting this research, and we also appreciate MEMS Lab, Nano Fabrication Center, AE Lab in SAIT, and EPRC (Electronic Packaging Technology R&D Center) in Tsinghua University for assistance with measurement and processing.

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