Journal of Electronic Materials, Vol. 12, No. 4, 1983

WORK FUNCTION MEASUREMENT OF TUNGSTEN POLYCIDE GATE STRUCTURES

T. J. Hwang*, S. H. Rogers*, and B. Z. Li**

*NCR Microelectronics, 1635 Aeroplaza Drive,
Colorado Springs, Co. 80916

**Department of Physics
University of Colorado at Colorado Springs, Co. 80907

(Received November 5, 1982; revised February 28, 1983)

Three MOS gate structures; polysilicon, tungsten silicide and tungsten polycide, were fabricated and their work-functions measured with the high frequency C-V technique. The work functions were 4.14 ev and 4.82 ev for phosphorus doped polysilicon and silicon-rich tungsten silicide, respectively. The tungsten polycide structure, however, showed a variance between 4.14 ev and 4.38 ev for different experiments. The polycide MOS device threshold was about 0.15 volt higher than that of polysilicon. Phosphorus out-diffusion and tungsten diffusion along polysilicon grain boundaries were postulated to explain this phenomenon.

Key Words: Work function, tungsten silicide, polycide, threshold voltage

Introduction

The next generation VLSI circuits with higher speed and density require some alternative interconnect materials to polycrystalline silicon in order to decrease the RC time delay. Refractory metal silicides, including WSi_2, $MoSi_2$, $TaSi_2$ and $TiSi_2$[1,2,3], are being considered as prospective materials for VLSI interconnects due to their low resistivity and good process compatibility [4,5]. Recently,

0361-5235/83/1204-0667$3.00 © 1983 AIME

the polycide gate structure, silicide on doped polysilicon, instead of the simpler silicide gate, has been proposed by Crowder et al.[6] because it can achieve relatively high conductivity while retaining polysilicon gate electrical characteristics.

Early proponents of the polycide structure made the assumption that the device threshold of polycide gate would not deviate from those of polysilicon gates. This requires that the work function of the lower polysilicon layer not be perturbed by the presence of the upper silicide layer. However, some recent reports observed a slight difference in threshold voltage between polycide and polysilicon gate devices [7,8]. It is therefore of interest to study the work function of the polycide gate structure.

Three basic structures (polycide, polysilicon and silicide) have been fabricated and the work functions measured utilizing the high frequency C-V method described in the next section. The experimental results and discussion are given in a later section.

Experimental Procedure

P-type <100> silicon wafers with ~17 Ω-cm resistivity were used as substrates to fabricate MOS capacitors. Three different gate structures were fabricated and tested in this experiment: (1) 5000Å phosphorus-doped polysilicon gate; (2) 3000Å to 4000Å tungsten silicide gate; (3) tungsten polycide gate with 1400Å to 4600Å phosphorus-doped polysilicon and 2500Å to 4000Å tungsten silicide.

All wafers were etched to bare silicon and then oxidized to a thickness of 2500Å at 1000°C. The wafers in each gate structure group were etched to produce a series of different gate oxide thicknesses in a buffered hydrofluoric acid solution. LPCVD polysilicon was deposited and then doped by phosphorus diffusion. The tungsten silicide film was deposited by co-sputtering from tungsten disilicide and silicon targets using a dual target S-gun sputtering system. The deposition rate was about 2Å/sec at 3.5 mTorr argon pressure. This co-sputtering process yields a silicon rich silicide film, WSi_x where x is about 3. A silicon rich silicide film is used to establish good adhesion to the substrate[9]. A barrel etcher was used to

delineate the gate areas using an SF_6/O_2 plasma. Barrel etching was used because of its greater selectivity over oxide than planar etching[10]. The polysilicon gate wafers were annealed in O_2 followed by N_2 for a total of 30 min. at 1000°C. Wafers with tungsten silicide films were annealed with the same thermal cycle, but with N_2 only. All wafers received a 30 min., 450°C anneal in forming gas. In two of the experiments a 1μm field isolation oxide was grown before the gate oxide to eliminate the lateral effect during C-V measurement. One set of wafers had a layer of undoped oxide deposited, contact holes opened and followed by aluminum metallization.

High frequency (1MHz) C-V measurements were used to determine the work functions of different structures. Under thermal equilibrium, the flatband voltage V_{FB} of a MOS structure is given by

$$V_{FB} = V_{MS} - \int_0^{t_i} \frac{\rho(x)x}{\varepsilon_i \varepsilon_o} \, dx \qquad (1)$$

where V_{MS} is the metal-semiconductor work function difference in volts, $\rho(x)$ is the charge density distribution in the oxide, t_i is the gate oxide thickness, ε_i is the dielectric constant of SiO_2, and ε_o is the permittivity of free space. In general, four types of charges exist in thermally-grown silicon dioxide[11]: (1) Fixed oxide charge Q_f, located near the Si/SiO_2 interface in the oxide; (2) Interface trapped charge Q_{it}; (3) Mobile ionic charge Q_m, and (4) Oxide trapped charge Q_{ot}. A bias-temperature stress test (20V, 200°C, 3 min.) produced less than 0.05 volt shift in the C-V curve. This implies that the mobile ionic charge is negligible. Also, for a well-grown gate oxide, the oxide trapped charge density is usually low enough to be negligible. The expression (1) can be simplified to

$$V_{FB} = V_{MS} - \frac{Q_i t_i}{\varepsilon_i \varepsilon_o} \qquad (2)$$

where Q_i is the total oxide charge density consisting of Q_f and Q_{it}. Once the V_{FB} versus oxide thickness curve is established, one can easily obtain the V_{MS} from the y-axis intercept and the Q_i from the slope based on the simple linear equation. The work function of the gate material

ϕ_M can be determined from

$$\phi_M = \phi_{MS} + (\chi_{Si} + \tfrac{1}{2}E_g + KT\ln\frac{N_A}{n_i}) \qquad (3)$$

where χ_{Si} is the silicon electron affinity (4.05ev), E_g is the silicon band-gap energy (1.12 ev), N_A is the acceptor concentration of the substrate, n_i is the intrinsic carrier concentration of the silicon. The MOS device threshold voltage may be calculated from the following expression

$$V_T = V_{MS} - \frac{Q_i}{C_i} - \frac{Q_B}{C_i} + 2V_F \qquad (4)$$

where C_i is the gate oxide capacitance, $V_F = \frac{KT}{q}\ln\frac{N_A}{n_i}$, and $Q_B = -(4\varepsilon_s\varepsilon_o N_A q V_F)^{\frac{1}{2}}$.

Results and Discussion

The final resistivity of the tungsten silicide after all processing steps is about 8×10^{-5} Ω-cm while the polysilicon resistivity is about 1×10^{-3} Ω-cm. High frequency C-V measurements were performed on all wafers with different gate structures and oxide thicknesses. Fig. 1 shows the C-V plots for a tungsten polycide gate of 2500Å polysilicon and 2500Å tungsten silicide and with various gate oxide thicknesses. The oxide thicknesses were calculated from C_i (or C_{max}). These thicknesses are in agreement with measurements taken before depositing polysilicon or tungsten silicide. The acceptor doping concentration was found to be (8-10) X 10^{14} cm^{-3} from C_{min} data. The flatband capacitance of each oxide thickness was first calculated from N_A and t_i in order to obtain the flatband voltage shifts V_{FB} from the C-V curve[11].

Fig. 2 shows the flatband voltage dependence on oxide thickness for polysilicon gates. The work function difference ϕ_{MS} is found to be -0.75ev (±0.05ev) and the work function of the polysilicon ϕ_M is 4.14ev(±0.05ev).

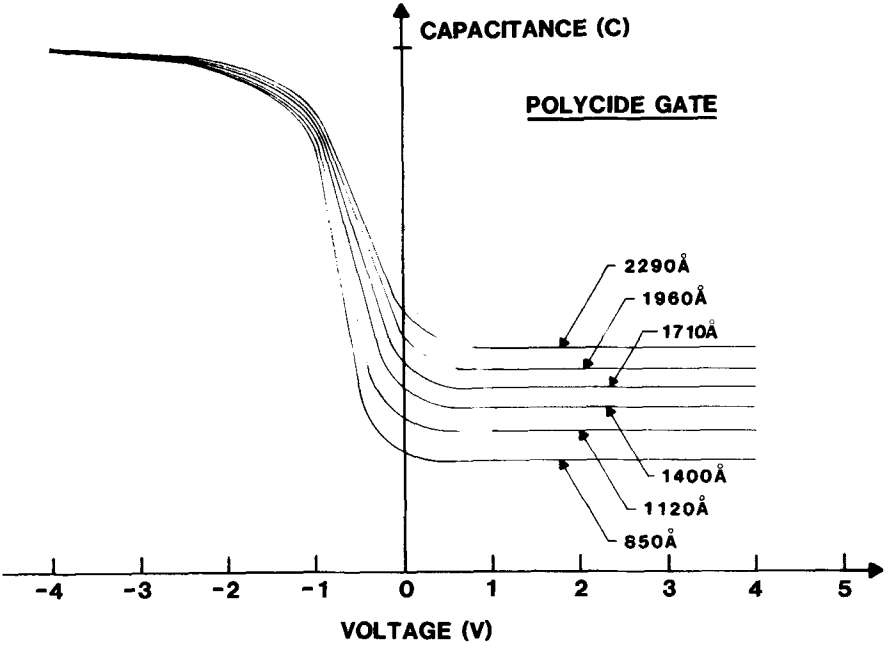

Fig. 1. Tungsten polycide (2500Å Poly/2500Å tungsten silicide) C-V plots for various gate oxide thicknesses.

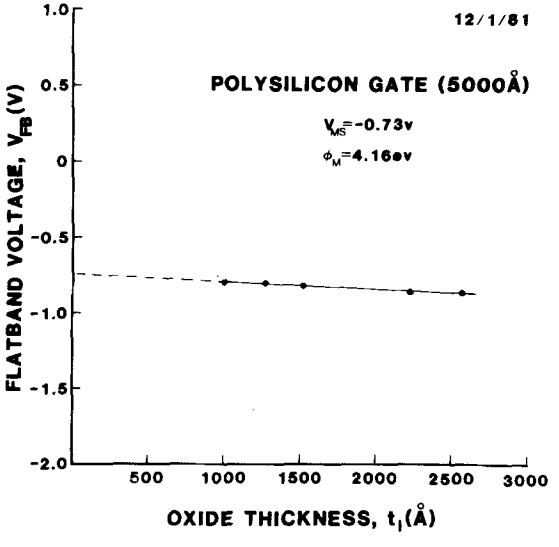

Fig. 2. The flatband voltage dependence on oxide thickness for a polysilicon gate MOS structure.

Fig. 3 is the plot of V_{FB} vs t_i for the tungsten silicide structure. The work function difference is -0.08ev $\pm$ 0.05ev. The work function of tungsten silicide has a corresponding value of 4.82ev $\pm$ 0.05ev. This result is in good agreement with the 4.8ev obtained by Saraswat et al.[12] whose experiments were on N-type substrates.

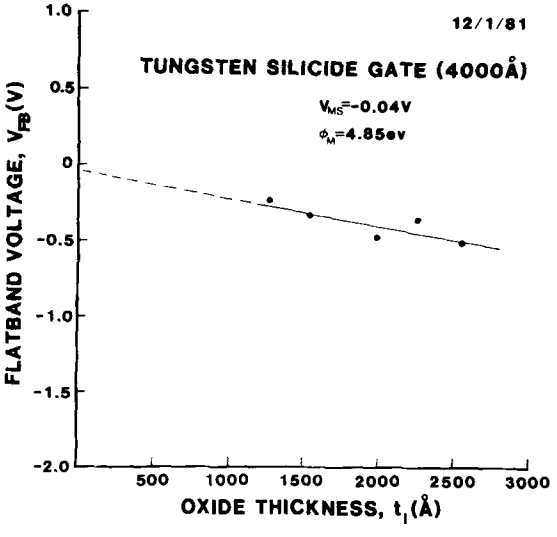

Fig. 3. The flatband voltage dependence on oxide thickness for a tungsten silicide gate MOS structure.

Fig. 4 and 5 show the typical plots $V_{FB}(t_i)$ from two sets of polycide experiments. Table I summarizes the data for the tungsten polycide experiments.

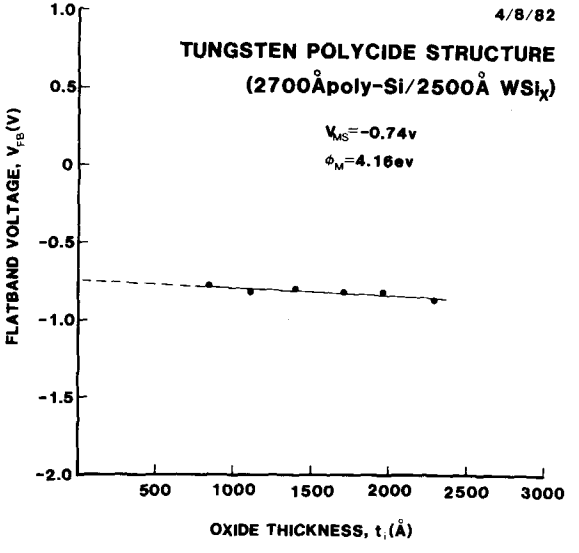

Fig. 4. A typical flatband voltage dependence on oxide thickness for the tungsten polycide MOS structure.

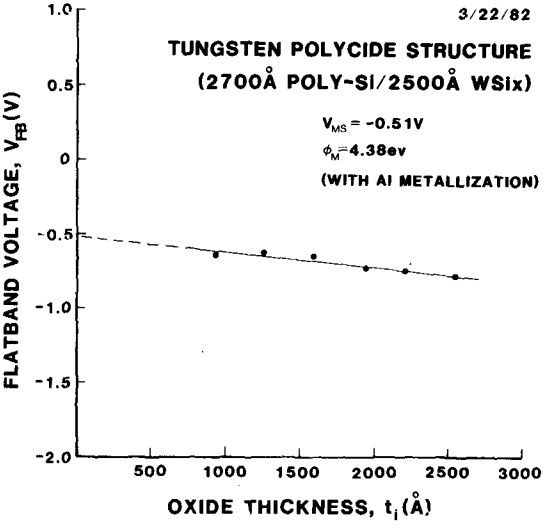

Fig. 5. Another typical flatband voltage dependence on oxide thickness for the tungsten polycide gate MOS structure.

TABLE I

Summary of Work Functions of Various Polycide Structures

EXPERIMENT	GATE STRUCTURE	V_{MS}(V)	ϕ_M(ev)
1	Poly-Si(2800Å)/WSi_x(2500Å)	-0.54	4.35
	Poly-Si(1000Å)/WSi_x(4000Å)	-0.51	4.38
2	Poly-Si(2700Å)/WSi_x(2500Å)	-0.51	4.38
3	Poly-Si(4600Å)/WSi_x(2500Å)	-0.76	4.14
	Poly-Si(2700Å)/WSi_x(2500Å)	-0.74	4.16
	Poly-Si(1400Å)/WSi_x(3000Å)	-0.74	4.16

The work function of tungsten polycide falls between polysilicon and tungsten silicide: ϕ_M(Polysilicon) $\leq \phi_M$ (tungsten polycide) $< \phi_M$(Tungsten silicide).

Fig. 6 depicts the $V_{FB}(t_i)$ data for the different gate structures from the same experiment. Fig. 7 shows the energy band diagrams for the three gate structures studied.

The threshold voltages of MOS devices with different gate structures were also compared. Using the work function and oxide charge density obtained from Fig. 6, the threshold voltages of MOS devices with t_i = 1000Å were calculated to be 0.14V for polysilicon gate and 0.33V for tungsten polycide gate. This threshold difference agrees with the measured threshold voltages of MOS devices from several regularly processed experiments, in which wafers were split between the polysilicon gate and polycide gate (2500Å Poly-Si/2500Å WSi_x) processes. For example, the 50um by 50um enhancement devices measured with zero back bias voltage produced the results of V_T = 0.35V for polysilicon gate and V_T = 0.52V for tungsten polycide gate and ΔV_T = 0.17V. Other tests (see Table II) on tungsten polycide gate devices of various sizes also showed a threshold difference of about 0.15 volt.

TABLE II

Linear Threshold Voltages of
Polysilicon and Polycide Gate Structures

Transistor Size (W/L) (μM)	Substrate Bias V_{BB}	Linear Threshold Polycide Gate	Linear Threshold Polysilicon Gate	Difference
3/3	-2.5V	$V_T = 1.10 \pm 0.04$	$V_T = 0.98 \pm 0.04$	$\Delta V_T = 0.12$
4.5/4.5	-2.5V	$V_T = 1.10 \pm 0.03$	$V_T = 0.97 \pm 0.04$	$\Delta V_T = 0.13$
18.75/3	-2.5V	$V_T = 0.99 \pm 0.04$	$V_T = 0.86 \pm 0.04$	$\Delta V_T = 0.13$
18.75/4	-2.5V	$V_T = 1.03 \pm 0.04$	$V_T = 0.90 \pm 0.04$	$\Delta V_T = 0.13$
3/9	-2.5V	$V_T = 1.17 \pm 0.02$	$V_T = 1.08 \pm 0.04$	$\Delta V_T = 0.09$
37.5/37.5	-2.5V	$V_T = 1.08 \pm 0.04$	$V_T = 0.93 \pm 0.03$	$\Delta V_T = 0.15$
37.5/37.5	0V	$V_T = 0.66 \pm 0.07$	$V_T = 0.50 \pm 0.02$	$\Delta V_T = 0.16$

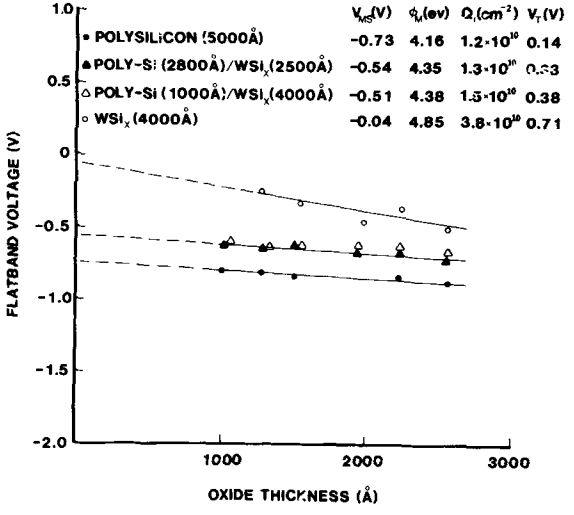

Fig. 6. The flatband voltage dependence on oxide thickness for different gate structures from one experiment.

The reason for the observed work function variance for the polycide structure is not clear. However, several possibilities may be postulated. First of all, it is possible that refractory metal atoms diffuse along the polysilicon grain boundaries which could significantly modify the Poly-Si/SiO_2 interface and result in a corresponding C-V shift. Another plausible explanation is based upon the outdiffusion of phosphorus from the doped polysilicon through the silicide layer. An oxide diffusion barrier was grown on the polysilicon gate devices in this study, whereas, the polycide gate devices lacked this barrier. In addition to this, recent work by Pan et al.[13] indicates that the diffusion coefficient of phosphorus in tungsten silicide is considerably greater than it is in polysilicon. Differences in polysilicon doping level could account for part of the observed threshold difference.

Other, as yet unidentified, process parameters could affect the work function. For instance, Razouk and Deal[14] have recently reported a strong hydrogen annealing effect on the metal-semiconductor work function difference. There remains considerable room for additional work to fully

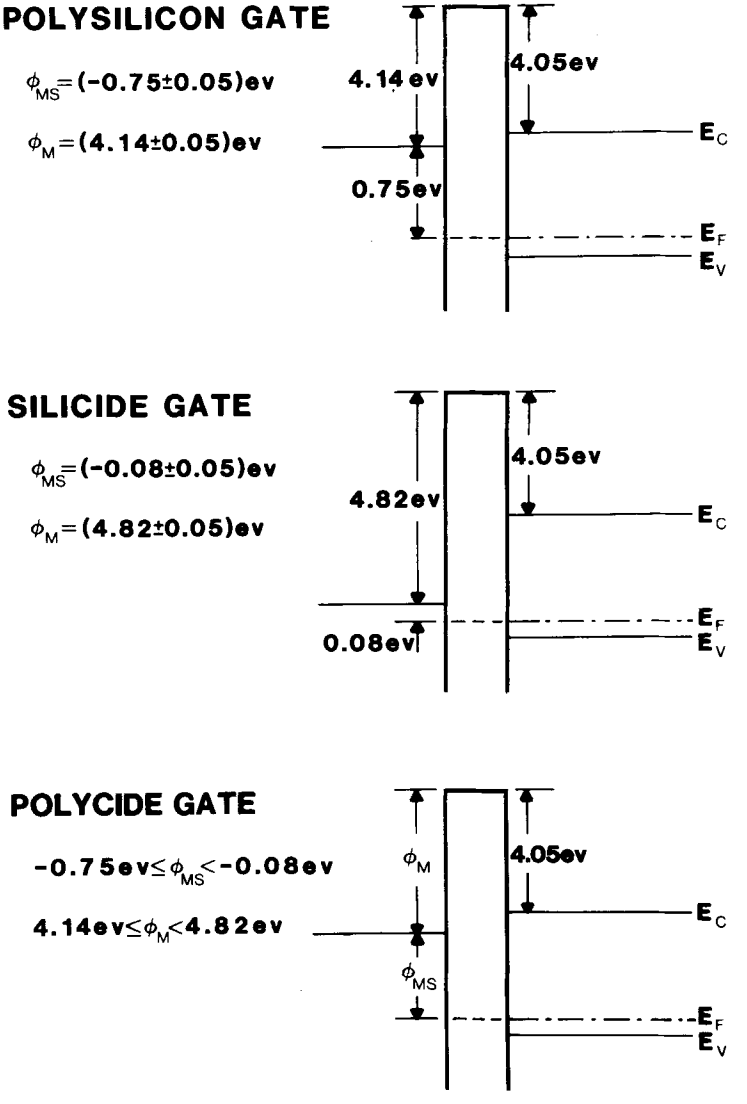

Fig. 7. The energy band diagrams for the MOS structures with polysilicon, tungsten silicide and tungsten polycide gates.

characterize and explain the observed variance of the work function difference of the tungsten polycide gate from that of the familiar polysilicon gate.

Summary

The work functions of polysilicon, tungsten silicide and tungsten polycide have been measured with the high frequency MOS C-V technique. The work function of phosphorus doped polysilicon, 4.14ev (±0.05ev), is in good agreement with previous work. Also, the work function of tungsten silicide 4.82ev (±0.05ev) obtained on P-Si substrates, supports the results of Saraswat et al., whose work used N type Si substrates. Variations of the work function difference between the values for polysilicon and tungsten silicide have been observed for the tungsten polycide structure. The higher threshold voltages of tungsten polycide devices compared with polysilicon devices have been shown essentially related to the higher work function of polycide structure. Some plausible reasons are suggested, however, the exact cause still requires further research.

Acknowledgement

The authors wish to thank M. E. Coe, D. Madden and R & D pilot line personnel for their help in the fabrication of the devices. They also thank the management support of NCR Microelectronics and the University of Colorado at Colorado Springs.

References

(1) J. L. Vossen, J. Vac, Sci.. Technol. 19, 761 (1981).

(2) S. P. Murarka, D. B. Farser, A. K. Shinha, and H. J. Levinstein, IEEE Trans. Electron Devices ED-27, 1409 (1980).

(3) T. P. Chow, A. J. Stecl, and R. T. Jerdonek, IEEE Electron Device Letters EDL-3, 37 (1982).

(4) F. Mohammad, Solid State Technol. Jan., 65 (1981).

(5) A. K. Sinha, J. Vac, Sci. Technol. 19, 778 (1981).

(6) B. L. Crowder and S. Zirinsky, IEEE Trans. Electron Devices ED-26, 369 (1979).

(7) D. B. Fraser, S. P. Murarka, A. R. Tretola, and A. K. Sinha, J. Vac., Si. Technol. 18, 345 (1981).

(8) M. Y. Tsai, H. H. Chao, L. M. Ephrath, B. L. Crowder, A. Cramer, R. S. Bennett, C. J. Lucchese, and M. Wordeman, J. Electrochem. Soc. 128, 2207 (1981).

(9) T. J. Hwang, S. H. Rogers, M. E. Coe, and B. Z. Li, Electrochem. Soc. Spring Meeting, Abs. #224, May (1982).

(10) M. E. Coe and S. H. Rogers, 1982 International Conference and Seminar Proceeding: Advanced Plasma Technology, Hawaii, Jan. 26, 1982.

(11) S. M. Sze, Physics of Semiconductor Devices, Chapter 7, Wiley, New York (1981).

(12) K. C. Saraswat, F. Mohammadi, and J. D. Meindl, IEDM Proceedings, 462 (1979).

(13) P. Pan, N. Hsieh, H. J. Geipel, and G. J. Slusser, J. Appl. Phys. 53, 3059 (1982).

(14) R. R. Razouk and B. E. Deal, J. Electrochem. Soc. 129, 805 (1982).