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# Morphology of Electromigration-Induced Damage and Failure in Al Alloy Thin Film Conductors

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Distinct morphologies of electromigration-induced voids and failures are shown for Al, Al-2%Cu, and Al-2%Cu-1% Si narrow (1–6 $\mu$m) unpassivated thin film conductors. SEM and TEM images typically show large non-fatal voids and narrow slit-like open circuit failures for all film conditions and accelerated test conditions. Evidence for transgranular slit failures is shown for 1.33 $\mu$m wide conductors. A simple model for void growth is presented which accounts for the void morphologies seen. The observed morphologies and the results of void growth modelling suggest that slit voids nucleate after other voids and rapidly produce failure. These conclusions are discussed in terms of 'classical' models for electromigration failure processes and resistance and noise power monitoring techniques.

**Key words:** Electromigration, Al-Cu, reliability, metallization

## INTRODUCTION

The reliability of thin film aluminum alloy interconnects is of increasing importance in integrated circuit device technologies. VLSI devices utilize large ($10^6$) numbers and long lengths (several meters) of metallization interconnects of decreasing width, thickness and spacing. These applications require extremely reliable metallization materials. However concern for electromigration and stressmigration failures limit device design and integration. These factors are expected to become more limiting as interconnect dimensions decrease further. Detailed microstructural analysis of tested and failed interconnects will be essential in order to characterize microstructural effects on failure mechanisms.

There have been many observations of electromigration-induced voids, hillocks and failure sites.[1–9] However many of these early studies were conducted on wide lines, $\cong$10–20 $\mu$m. Wide lines typically have many grains across their width with a linewidth-to-grain size ratio (W/d) of approximately 5–20. These previous observations can be summarized as follows. Electromigration mass flux divergences induce many voids in line interiors by nucleation and growth, usually at grain boundaries and grain triple points. (By definition sites of void growth are regions of negative mass flux divergence.) These voids, which were also shown to be mobile, grew large enough to coalesce[1] and significantly reduce the linewidth. The increased current density in the remaining cross section leads to local joule heating. This in turn could accelerate void growth either by increasing mass flux at the divergent site or by temperature gradient-induced vacancy accumulation.[8] Accelerated void growth would rapidly lead to open circuit failure. (It was noted however[4] that large voids did not necessarily produce failures. Failures could occur at the cathode ends of stripes[4] when this was the region of large temperature gradient.) In general the resultant failure site would be wide with extensive voiding surrounding the open circuit. Often local melting would make microstructural failure analysis difficult. In addition, usual constant current testing often destroys the open circuit site, complicating failure analysis[10] as the power supply output potential climbs rapidly at failure. The consistency of these observations has led to the acceptance of this process as the general open circuit failure mechanism. Microstructural details such as solute segregation or depletion,[8,11] local grain boundary structure,[8] and large size differences between adjacent grains[5,6] could give rise to the flux divergent sites which initiate the failure process. Implicit in this process is that sites of the largest flux divergence would produce the earliest failures.

Currently VLSI interconnects are typically 1–2 $\mu$m wide, and 0.5 $\mu$m wide lines are currently in development for 16 MB DRAM applications. Unless barrier material underlayers limit grain size their structure is nearly 'bamboo' along the line, with W/d $\cong$ 1.0 or less. It is not obvious that the failure model described above is operative for these narrow interconnects. Research has shown that stress migration[12,13,14,15] failure rates increase as linewidths decrease below $\cong$3.0 $\mu$m, and that the electromigration median time to failure (MTF) exhibits a minimum[16,17] around W/d $\cong$ 1.0. Stress migration produces both large voids and distinctive narrow slit open circuit failures[13,18] at these linewidths. However there have been relatively few recent detailed analyses of electromigration-induced damage and failures in narrow interconnects.[10,19] The results presented here include SEM and TEM observations

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of damage and open circuit failures in electromigration tested Al, Al-2%Cu and Al-2%Cu-1% Si unpassivated interconnects with linewidths from ≅1.0 μm to 6.0 μm.

## EXPERIMENTAL

Al, Al-2%Cu and Al-2%Cu-1% Si films, nominally 0.5 μm thick, were deposited in single wafer or in batch sputtering systems. Substrates for all films were (100) 100 mm silicon wafers thermally oxidized to 450Å thickness. Sputtering dc bias was 0V, −100V, and −450V, and substrate temperatures were nominally ambient (unheated) or 450° C in the sputtering chamber. Electromigration test pattern lithography and anisotropic plasma etching produced conductor linewidths from ≅1.0 to 6.0 μm. Test circuits consisted of parallel line arrays (PLA) of 25 and 50 conductors which are suitable for constant voltage testing. Circuits were annealed in forming gas by rapid thermal annealing (RTA) or in a hot wall furnace. RTA cycle was 500° C for 1 min, while the furnace cycle was 425° C for 30 min. Annealing occurred either prior to or after PLA circuit patterning. Unpassivated circuits were tested in both the as-deposited and annealed conditions. Accelerated electromigration testing was performed between 200 to 250° C at current densities in the range 0.7 to 2.5 $10^6$ amps/sq cm. A constant voltage power supply[20] was used to power the PLA test structures. This testing mode preserves the open circuit failure site and allows for failure site microscopy.[10] The constant voltage condition is essentially identical to the usual constant current case when resistance drift during testing is on the order of 1% prior to open circuit. This is usually the case for long (1.0 mm) single layer aluminum alloy conductors.

PLA circuits were examined by SEM and TEM after open circuit failure of all of the lines in the array. However one test was interrupted for sequential SEM observation of 4 or 5 sites each on 12 lines in a 50 line array. Void growth and damage was monitored after 18.3, 36.1 and 111.1 hr during interruption intervals of approximately 1.5 hr each.

## RESULTS

### *Post Mortem Void Morphologies*

Extensive voiding and hillock formation was seen in pure aluminum conductors, Fig. 1. Large equiaxed voids were usually nearby and "upstream" to large hillocks with respect to the direction of electron and mass flux. By definition hillocks are regions of positive mass flux divergence, and voids are sites of negative flux divergence. Growth of surface perturbations such as hillocks, extrusions and whiskers may lead to failure by short circuiting with adjacent interconnects. Hillock and whisker formation are also observed after annealing. Their formation is presumably due to compressive stress relaxation by diffusional creep at film grain boundaries.[21,22]

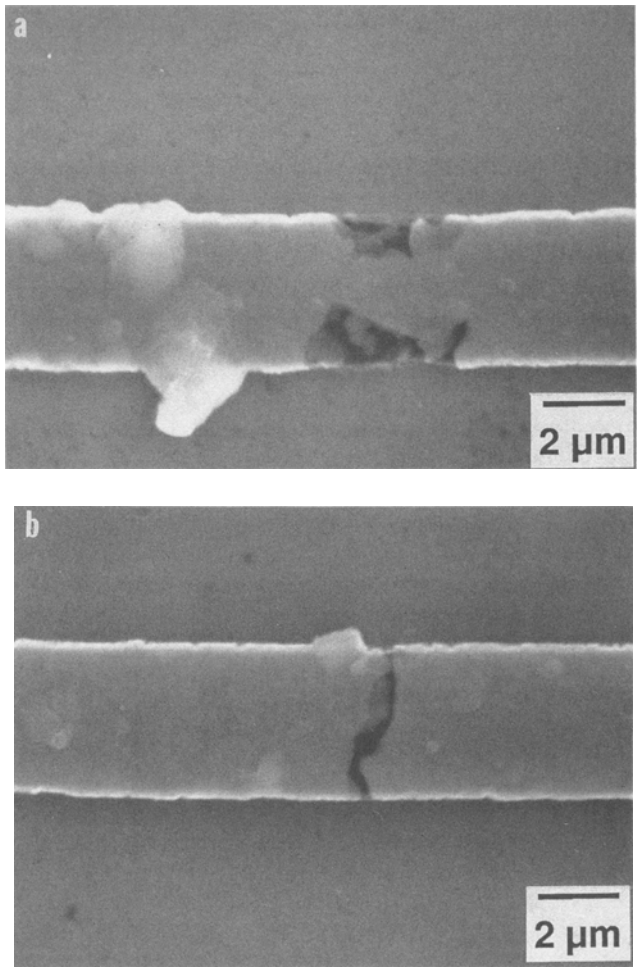


Fig. 1 — Electromigration-induced voids, hillocks and narrow failures in 3.8 μm wide Al conductor tested at 250° C and 1.0 10E6 A/sq cm. Direction of electron and mass flux was from right to left. a) Erosion void and downstream hillock. b) Narrow void failure in same line as a).

Thermal expansion mismatch between Al and Si is the source of thermal stress.

Open circuit failure sites in pure Al were usually narrow and widely separated from hillocks of significant volume. The surfaces of both the large-wide voids and the narrow slit failures showed significant faceting and layering, Fig. 1. Plan view TEM of a large 'erosion' void shows the disappearance of grains, Fig. 2.

Both Al-2%Cu and Al-2%Cu-1%Si conductors similarly had numerous large voids with large nearby "downstream" hillocks and narrow slit failures, Fig. 3. Again the failures were widely separated from significant hillocking. Void and failure surfaces were very smooth. Both wide erosion voids and slit failures occurred near Cu rich $\Theta$ precipitates, Fig. 4. Thus copper depletion was not observed to be a general precursor to failure. In addition, long and shallow edge voids were up to 5 μm long, Fig. 5. It has been shown that slit failures may occur across grains, not along grain boundaries.[10] TEM evidence of a similar transgranular open cir-

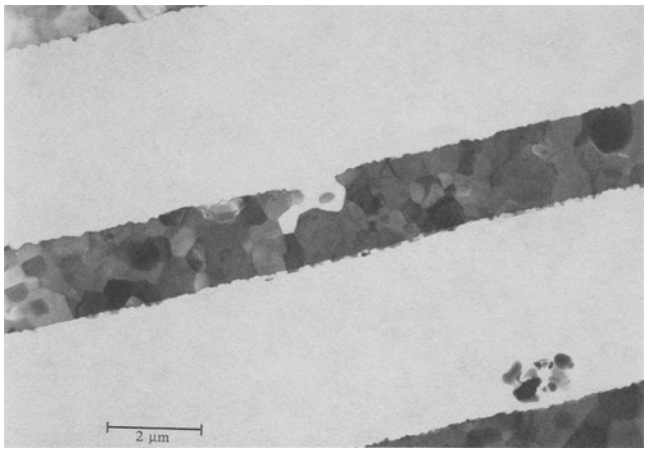


Fig. 2 — Plan view TEM of erosion void in 2 μm wide Al conductor.

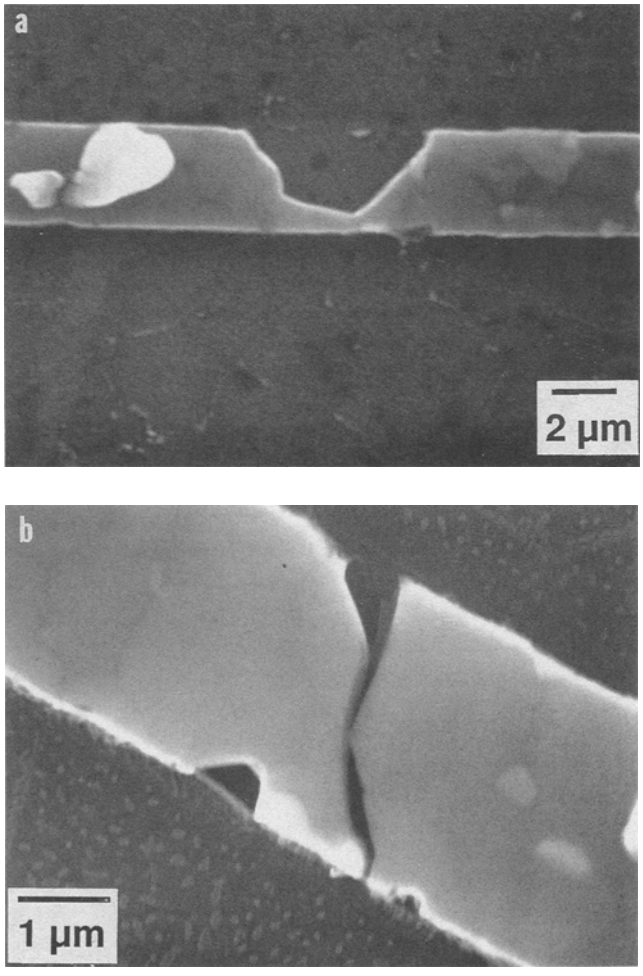


Fig. 3 — Electromigration-induced void, hillock and slit failure in 3.8 μm wide Al-2% Cu conductor tested at 250° C and 1.2 10E6 A/sq cm. Direction of electron and mass flux was from right to left. a) Erosion void and downstream hillock. b) Narrow void failure.

cuit is shown in Fig. 6, with arrows pointing out grain boundary contrast. The conductor in Fig. 6 was annealed prior to patterning, and the film structure prior to testing was equiaxed columnar grains with 2.4 μm average diameter.

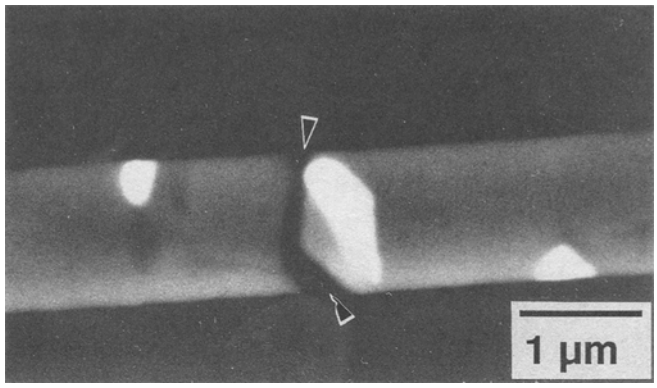


Fig. 4 — Backscattered electron image of narrow slit failure (arrows) in Al-2% Cu conductor. Failure (arrows) is adjacent to $\Theta$ ($CuAl_2$) precipitate which shows bright contrast. Conductor linewidth is 1.33 μm and was tested at 230° C and 1.75 10E6 A/sq cm.

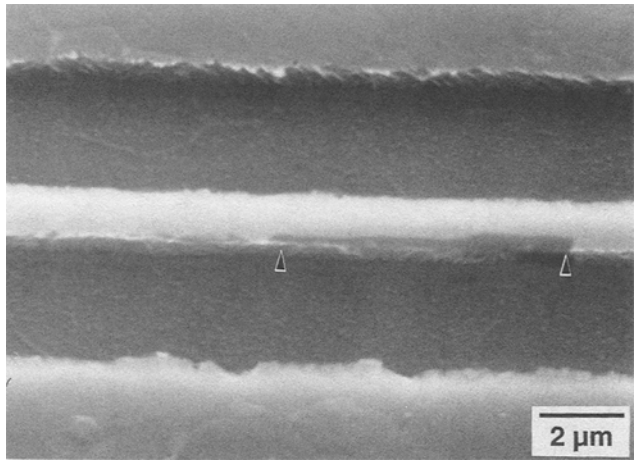


Fig. 5 — Long edge notch void in Al-2% Cu 1.5 μm conductor tested at 264° C and 1.75 10E6 A/sq cm. Sample is tilted at 45°.

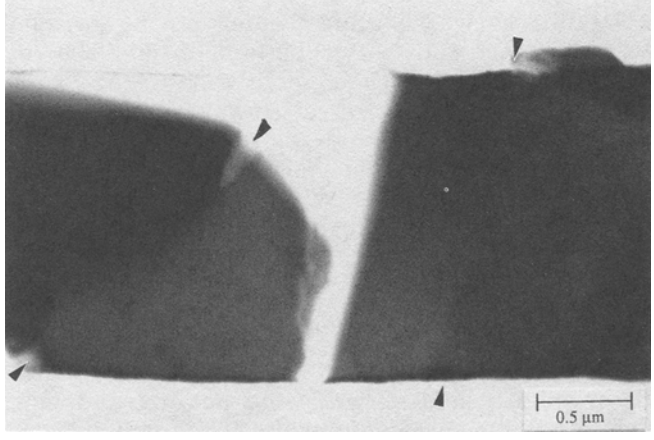


Fig. 6 — TEM micrograph of slit failure in Al-2% Cu-1% Si 1.33 μm wide conductor. Arrows indicate grain boundary contrast, suggesting slit is transgranular. Film was sputter deposited at 450° C and −100 volts bias, and was annealed by RTA at 500° C for 1 min prior to patterning. Average grain size is 2.4 μm, and linewidth/grain size ratio ($W/d$) is ≅0.5.

Conductors for each film type showed many sites of void and hillock growth. The damage included small and large equiaxed erosion voids with nearby hillocks, long shallow edge voids, and a single narrow slit open circuit. The degree of notch and erosion voiding trended roughly inversely with electromigration lifetime (MTF). Pure Al conductors tested at the highest temperature and current density had the most extensive voiding and shortest MTF. Al-Cu and Al-Cu-Si conductors tested at the lowest temperatures and current densities showed the least amount of non-fatal voiding and damage, as expected. However in all cases failure was typically due to a relatively small volume narrow slit void. The width of slit failures decreased with decreasing linewidths and decreasing W/d. Small slit voids not completely traversing the line, which could be incipient slit failures, were rarely seen.

Unannealed 1.33 and 2.20 $\mu$m wide Al-2%Cu conductors with initial grain size of about 0.13 $\mu$m had (W/d) from 10 to 17, respectively. Failure sites in both were relatively small voids, although not as narrow as for annealed conductors of the same linewidth. Annealed conductors had a larger grain size and therefore a smaller (W/d) by a factor of about 10 for these linewidths. Extensive agglomeration and uniform thinning occurred in many of the unannealed 1.33 $\mu$m lines. Some of the thinned areas produced failures by local melting, Fig. 7. No agglomeration or thinning was observed in the unannealed 2.2 $\mu$m conductors after testing or in adjacent untested 1.33 $\mu$m lines. The agglomeration and thinning is probably due to film morphological instability[23] for the narrowest small grained conductor. Grain growth,[23] extensive grain boundary diffusion, narrow linewidth and the accelerated test conditions (230° C at 1.75 $10^6$ A/sq cm) allow the morphological instability to produce agglomerated/thinned structure. This effect is not expected to be relevant for interconnects in actual service. Film annealing and passivation layers will reduce the driving forces and mechanism for conductor breakup by agglomeration.

All films showed 'healing events'[20] during testing. No systematic study was done to determine the effects of film composition, microstructure and test conditions on healing rates. However the narrow open circuit suggests that the opposite faces may easily 'reconnect' during testing by surface diffusion, driven for example by capillarity or the large electric field ($\cong 10^5$ V/cm) across the narrow interface.

*Interrupted Test Observations*

SEM inspections during test interruptions show discontinuous void growth, void healing and motion, similar to previous results.[3,24,25] Void growth rate and direction changed as testing proceeded, Fig. 8. Void location varied with time, Fig. 9. This evidence does not determine if void motion is principally due to shrinkage and regrowth in another location or due to uniform void migration. Evidence of void growth by the coalescence of small voids into larger ones was seen only for the widest lines. Void growth and coarsening by coalescence have been reported both for passivated[25] and unpassivated[3,24] conductors undergoing electromigration.

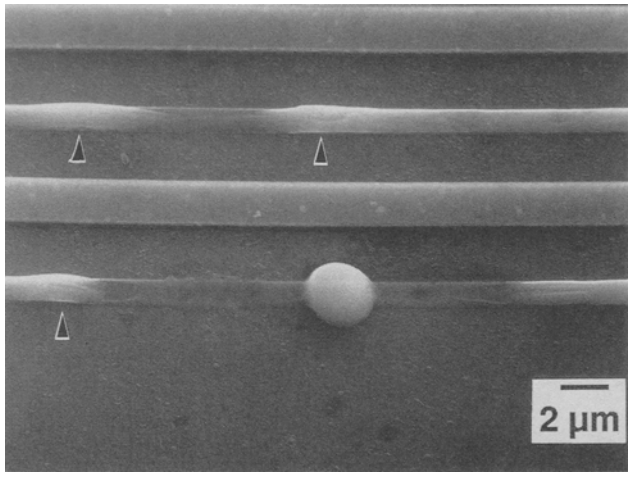


Fig. 7 — Agglomeration (at arrows), melting and thinning during electromigration testing of 1.33 $\mu$m wide Al-2% Cu conductor in as-deposited condition. Initial grain size $\cong$0.13 $\mu$m, and $W/d \cong 10$. Identical untested lines did not decompose during the thermal cycle of the accelerated (230° C, 1.75 10E6 A/sq cm) electromigration test.

As in the post mortem observations, failures were due to narrow slit voids, Fig. 10. Slits appeared narrower than for the uninterrupted cases. Small slit voids were not observed during test interruptions. This suggests that the slit void growth rate is significantly more rapid than for the other morphologies seen, and that the slit void, once initiated, rapidly produces an open circuit failure.

## DISCUSSION

Extensive voiding and varied void morphologies were seen for all film compositions, linewidths and test conditions. (Since only open circuit failures are studied here, hillocks are relevant only because of their proximity to large equiaxed voids.) More extensive voiding was indicative of reduced MTF. This can be assumed to be due to increased electromigration-induced mass flux acting with local microstructure to produce more sites of flux divergence. A commonly used expression for electromigration flux[26] is

$$J = (N\,Do/kT)\,Z\,e\,j\,\rho \exp(-Ea/kT) \qquad (1)$$

where

$J$ = mass flux,
$N$ = number of atoms/volume,
$Do$ = diffusion pre-exponent,
$Z$ = 'effective charge' of diffusing ion,
$e$ = electronic charge,

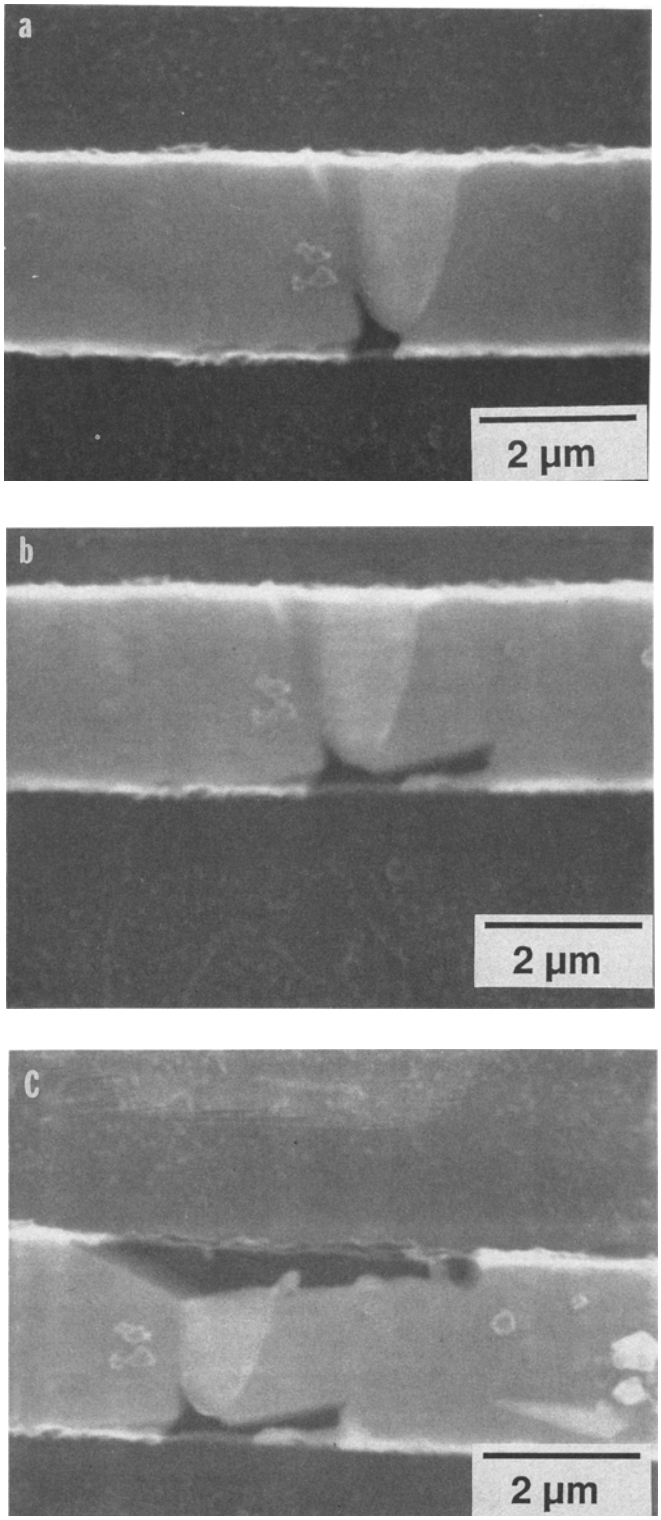


Fig. 8 — Discontinuous void growth observed during electromigration test interruptions in Al-2% Cu 2.6 $\mu$m wide conductor. Accelerated test conditions were 248° C and 0.8 10E6 A/sq cm. a) Void after 18.3 hr b) after 36.1 hr c) after 111.1 hr.

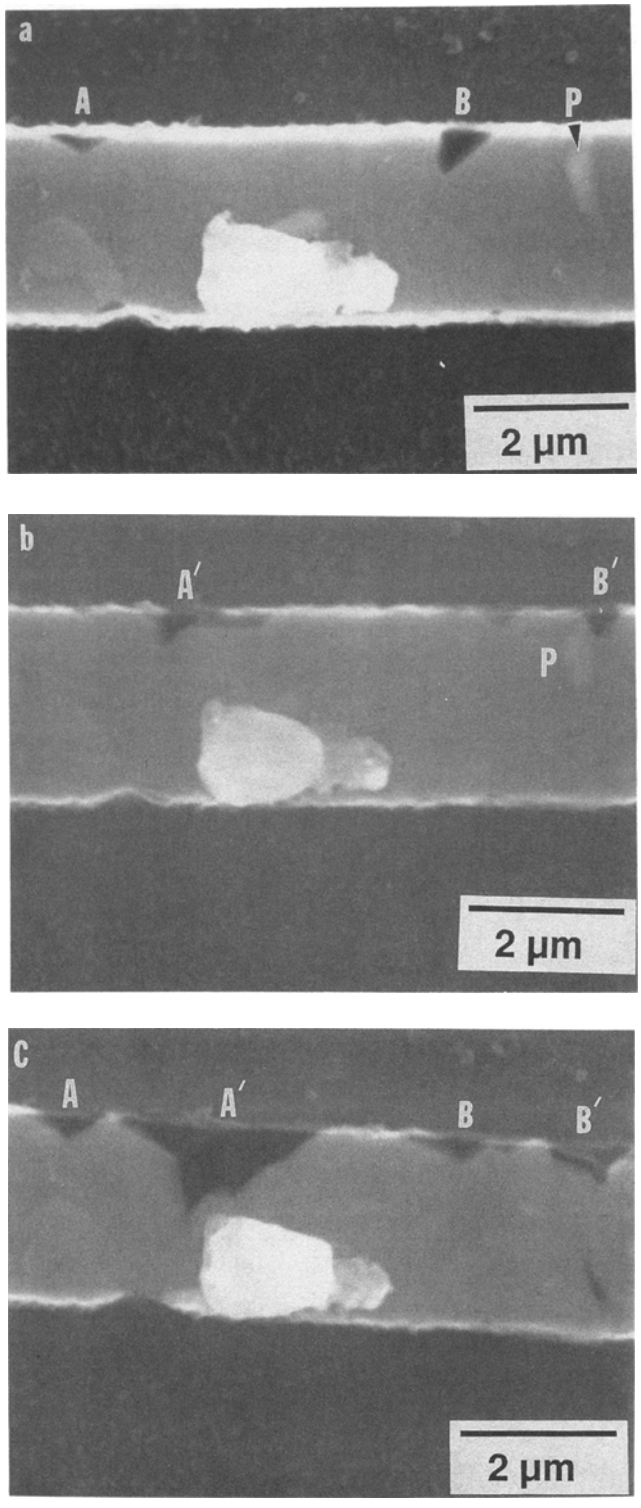


Fig. 9 — Void motion during interrupted testing of Al-2% Cu conductor, same series as in Fig. 8. a) Note voids after 18.3 hr at locations A, B and $\Theta$ precipitate at $P$. b) New positions of voids, A′, B′, after 36.1 hr. c) Void regrowth at original locations A, B and continued growth at A′, B′, after 111.1 hr. Note virtual disappearance of $\Theta$ at position P.

$j$ = electrical current density,
$\rho$ = conductor resistivity,
$E$ = activation energy for diffusion,
$k$ = Boltzman's constant,
$T$ = temperature.

This expression is insensitive to film microstructural factors which are known to largely determine conductor lifetime. Since it is assumed that grain boundaries are the diffusion pathways (1) can be

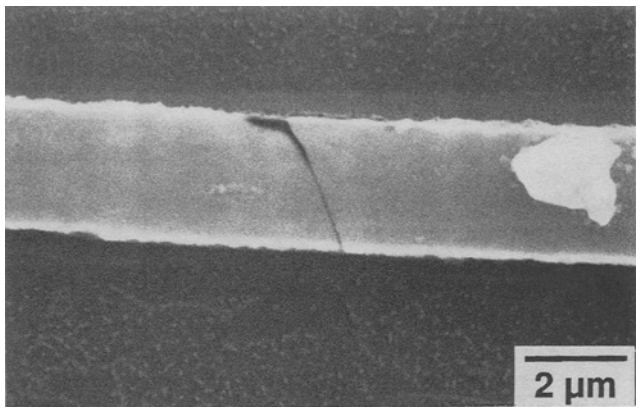


Fig. 10 — Narrow slit failure in 2.6 μm wide Al-2% Cu conductor during interrupted test.

modified to include the ratio of grain boundary width to grain size ($\delta/d$) and the grain boundary diffusion activation energy ($Egb$)

$$J = [\delta/d](N\,Do/kT)\,Z\,e\,j\,\rho \exp(-Egb/kT) \quad (2)$$

Traditionally this expression is used to describe the driving force and process for mass depletion electromigration failure along grain boundaries. However it does not provide a basis for the description of mass flux divergence leading to void initiation, growth and conductor failure. The 'classical' model for failure, as described above, suggests that the largest flux divergences produce the largest and fastest growing voids, which produce the earliest failures. We have documented that the degree and extent of non-fatal voiding is somewhat correlated with average conductor lifetime. However, failures were in general due to small flux divergences which produced failures of relatively small void volumes. This is especially significant since it has been shown that slit failures may be transgranular[10] in the narrowest conductors, Fig. 6. Therefore a simple failure mechanism of mass depletion along a grain boundary (crossing the line width) which produces a narrow open circuit is not generally applicable.

Electromigration-induced voids in narrow interconnects may be characterized by three distinct morphologies, shallow edge "notch," equiaxed "erosion" and narrow "slit" failures. A simple model of void growth for these morphologies may be constructed. The model may be helpful in understanding the implications of the various void morphologies seen. Assume an initial void nucleus of length $l$, width $Y$, and of thickness $T$ equal to film thickness positioned on the conductor of linewidth $W$ as in Fig. 11. Final void morphology can be considered to be the result of growth under three limiting conditions. A notch is produced when void length $l$ increases and width $Y$ is constant during testing, $Y$ = constant and $l = l(t)$. Similarly an equiaxed erosion void is produced under the growth conditions $Y = Y(t) \cong l(t)$. A slit is produced when $l$ = constant, and $Y = Y(t)$. Assume that the rate of void growth is determined by the magnitude of (local)

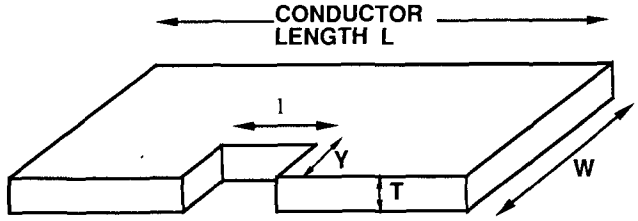


Fig. 11 — Schematic of an initial electromigration void on a conductor. Edge void develops as length 1 increases with $Y$ = constant. Equiaxed erosion void develops as $l$ and $Y$ increase. Narrow slit void occurs with $l$ = constant and $Y$ increasing.

volumetric mass flux divergence ($\nabla J$). $\nabla J$ is the result of the difference between mass fluxes ($\Delta J$) entering and leaving a small segment of the conductor, ≅ one grain diameter ($d$), given by

$$\nabla J = \Delta J/d \quad (3)$$

The rate of void growth ($dV/dt$) can then be expressed in terms of $\Delta J$

$$dV_i/dt = \Omega\,\Delta J_i\,A \quad (4)$$

where

$dV_i/dt$ = volumetric rate of void growth,
$\Omega$ = atomic volume,
$\Delta J_i$ = mass flux difference, assumed to be locally constant for each void,
$A$ = $WT$, cross-section of conductor sustaining mass flux.

The subscript $i$ denotes type of void. Since $V_i$ is in general $V_i = lYT$, the rate of void growth ($dV_i/dt$) for each morphology can be determined from the growth conditions above. For notch void growth ($i$ = 1) and $Y$ = constant,

$$dV_1/dt = TY\,dl/dt \quad (5)$$

or,

$$dl/dt = \Omega\,\Delta J_1\,A/TY \quad (6)$$

and,

$$l(t) = \{\Omega\,\Delta J_1\,W/Y\}\,t \quad (7)$$

This morphology will not produce an open circuit failure and will not be considered further. Note however that edge notch voids may retain their shape as they grow to at least several times the grain size, Fig. 5.

For erosion void growth ($i$ = 2) and $Y(t) \cong l(t)$,

$$dV_2/dt = 2\,T\,l\,dl/dt = \Omega\,\Delta J_2\,A \quad (8)$$

$$Y(t) = l(t) = \{\Omega\,\Delta J_2\,W\,t\}^{1/2} \quad (9)$$

Failure occurs when $Y = W$ at time $t_2$ given by

$$t_2 = W/(\Omega\,\Delta J_2) \quad (10)$$

Note the dependence of erosion void failure times on linewidth $W$ for this model. This dependence is observed experimentally for conductors with increasing $W$ at constant grain size.[16,17,27]

For slit void growth ($i = 3$) and $l$ = constant,

$$dV_3/dt = l\,T\,dY/dt = \Omega\,\Delta J_3\,A \qquad (11)$$

$$Y(t) = (\Omega\,\Delta J_3\,W\,t)/l \qquad (12)$$

Failure time due to a slit void ($Y = W$) is independent of linewidth and is given by

$$t_3 = l/(\Omega\,\Delta J_3) \qquad (13)$$

The observed damage and failure morphologies can be discussed in terms of this model under several limiting conditions. Assume in one instance that local mass flux divergence producing an erosion void at one site is equal to the flux divergence producing a slit failure at another unrelated site, *i.e.* $\Delta J_2 \cong \Delta J_3$. Then from Eq. (10, 13) above

$$t_2 = (l/W)\,t_3 \qquad (14)$$

Slit widths varied from about 0.05 to 0.2 $\mu$m, and linewidths varied from 1.3 to 6.0 $\mu$m. We choose a nominal ($l/W$) of 0.05 for discussion. Under the assumption of equivalent flux divergences, the model yields $t_3 \cong 0.05\,t_2$. That is, slit voids produce failure at much earlier times than erosion voids. This obvious result corresponds to the consistency of failures produced by slit voids. However, the assumption that $\Delta J_2 = \Delta J_3$ requires that all voids seen, if initiated at the same time, will have the same volume. This was in general not observed. Further it is expected that local variations in microstructure will produce flux divergences of varying magnitude, making the initial assumption of equal local fluxes unrealistic.

Alternatively, assume that the mass flux difference that creates a slit failure is much less than that for an erosion void, $\Delta J_3 \cong (0.05)\,\Delta J_2$. Then from above, erosion failure time will be on the order of slit failure time, $t_2 \cong t_3$. For voids initiated at the same time erosion failures would be expected with the same frequency as slit failures. This was not observed. This simple model, applied to the observed void and failure morphologies, suggests that slit voids are initiated at times later than large erosion voids. Once 'nucleated' slits rapidly grow to product failures under relatively small flux divergences. This is consistent with the lack of incipient slit failures seen either post mortem or during test interruptions. Large flux divergences are usually not fatal, while other small divergences rapidly produce slit failures. Electromigration lifetime in narrow interconnects is thus attributed to the effects of microstructure, flux driving forces and mobility on the incubation time for slit voiding rather than on the magnitude of mass flux divergence.

Techniques for electromigration lifetime prediction and monitoring include resistometric[2,28] and $1/f$ current noise[29,30] methods. However the variation of void and damage volumes complicates the interpretation of these monitoring techniques. We have shown extensive voiding away from failure sites. Resistance increase measured prior to open circuit can be shown to be principally due to the large and numerous non-fatal erosion voids. Other microstructural changes such as grain growth, precipitation, and defect annealing[31] may also contribute to resistance and noise power measurements. These are expected to be small in comparison to electromigration-induced voiding.

Resistance drift can be defined as $\Delta R/R_o = [R(t) - R_o]/R_o$, where $R(t)$ is resistance measured during test and $R_o$ is initial resistance. The resistance change in a conductor of overall length $L$, with resistivity $\rho$ and with a single void of volume ($lYT$) in the geometry in Fig. 11, is given by

$$\Delta R/R_o = \{\rho l/T(W - Y) + \rho(L - l)/TW - \rho L/TW\}/\{\rho L/TW\} \qquad (15)$$

or,

$$\Delta R/R_o = \{l(t)/L\}\{[W/W - Y(t)] - 1\} \qquad (16)$$

Resistance drift during void growth can be simulated using Eq. (9) for $l(t)$ and $Y(t)$ during erosion void growth. Mass flux difference $\Delta J_2$ is chosen to arbitrarily produce an erosion failure at 10 hr. Total resistance drift for a 1.0 mm long 10 $\mu$m wide conductor with an erosion void, Fig. 12, is calculated. For comparison, resistance drift due to the growth of a slit void is calculated using Eq. (13) for

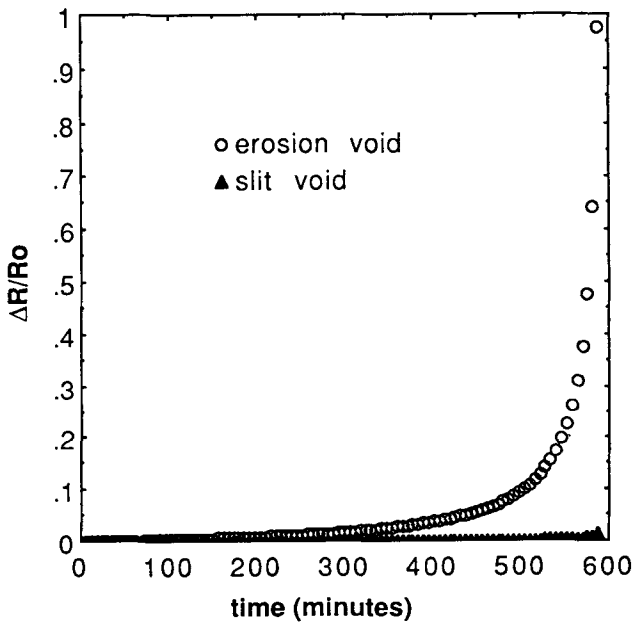


Fig. 12 — Simulated resistance increase ($\Delta R/Ro$) in a 1.0 mm 10 $\mu$m wide conductor due to the growth of an erosion void (O) and a slit void ($\Delta$). Mass flux divergences were chosen in the simulation to produce a failure at 10 hr for both the erosion void and slit void cases.

$Y(t)$, Fig. 12. Mass flux difference $\Delta J_3$ for the slit failure is also chosen to produce failure at 10 hr. Since the total resistance drift is measured, the resistance due to an erosion void essentially masks that from a growing slit void. This simulation is similar to data reported for resistance drift in single Al conductors under electromigration testing.[2] Gradual resistance drift is thus attributed to multiple erosion void growth until slit void initiation and growth rapidly produces an open circuit. Resistance drift is expected to be larger for wider lines since the extent of non-fatal voiding was observed to increase with linewidth. Resistance measurements therefore largely monitor the extent of mass flux divergence and void growth, not failure processes per se.

A similar discussion is applicable to noise and current noise power measurement techniques. The source of noise in solids undergoing electromigration is still a matter of contention. However it may be assumed that the noise power as measured during electromigration is dependent on the magnitude of the processes (*i.e.* mass flux, *etc.*) occurring. Noise power spectra typically show significant increases prior to failure during electromigration testing, presumably due to void growth.[29] Noise from slit void growth would probably be masked by noise generated during the growth of large erosion voids. These techniques therefore monitor the extent of voiding which may be correlated with median failure behavior. However they may not directly monitor the failure processes in thin film conductors.

Further work is required to determine which aspects of narrow conductor microstructure determine the mass flux devergences responsible for the distinct void morphologies shown. Also of interest are the effects of linewidth and $W/d$ on the extent of non-fatal voiding, and the mechanism for transgranular slit failure in the narrowest conductors.

## CONCLUSIONS

Electromigration-induced damage produces distinct void and failure morphologies in Al, Al-2% Cu and Al-2% Cu-1% Si narrow interconnects. Equiaxed erosion and edge notch voids and slit open circuit failures were seen for all films under all testing conditions. The extent of non-fatal voiding varied inversely with MTF for each conductor type and test (accelerating) conditions of temperature and current density. Individual void growth rate and direction varied during testing, and void motion was observed. In general voids grew and migrated towards the cathode terminal. The void morphologies and the results of void growth modelling suggest that slit voids once initiated rapidly produce failure under relatively small mass flux divergence. Electromigration lifetime in narrow interconnects is proposed to be determined by the incubation period for slit void nucleation. Test conditions, conductor microstructure and electromigration driving forces determine this incubation period. Resistometric and noise techniques monitor the extent of mass flux divergence and voiding, and may only indirectly monitor electromigration failure processes.

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