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Electrical and Structural Characterization of GaAs Vertical-Sidewall Epilayers Grown by Atomic Layer Epitaxy*

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Electrical and structural measurements have been performed on novel test structures incorporating *p*-type GaAs epilayers grown by organometallic vapor phase atomic layer epitaxy on the vertical sidewalls of semi-insulating GaAs rods formed by ion-beam-assisted etching. Preliminary results indicate that the vertical-sidewall epilayers have excellent crystal quality and sufficient electrical quality to support a sidewall-epitaxy device technology. Some examples of candidate electronic, electrooptic, and photonic devices for vertical-sidewall fabrication are FETs, resistors, waveguides, modulators, and quantum-wire and quantum-dot lasers.

Key words: Sidewall epitaxy, atomic layer epitaxy, organometallic vapor phase epitaxy, and GaAs

INTRODUCTION

Over the past decade, materials growth and fabrication techniques utilizing very thin planar semiconductor epilayers have been applied to improve the performance of microelectronic and photonic devices. These advances have led to high-density, high-performance integrated electronic and photonic circuits. However, the long-term need for increased device density and performance will require the development of vertical integration schemes in combination with the improved planar integration technologies. Therefore, we have investigated the possibility of growing device-worthy epilayers on etched sidewalls of GaAs rods. A vertical-sidewall epitaxy and fabrication technology could not only enable increases in circuit density but could also lead to a variety of interesting sidewall devices including FETs, resistors, waveguides, modulators, and a new generation of quantum-wire and quantum-dot lasers.

In this paper, we report our progress in developing compatible techniques for growing, isolating, and contacting vertical-sidewall epilayers. These procedures have been demonstrated in the fabrication of a novel test structure designed to determine the carrier-concentration/thickness product of the epilayers by means of current saturation measurements. The test structure, shown schematically in Fig. 1, consists of a semi-insulating (SI) GaAs rod about 2 μm high and 75 μm long with *p*-type conducting epilayers grown on the two long vertical sidewalls. Electrical connections are provided at both ends of the rod by wraparound ohmic contacts. The rod is formed by chlorine ion-beam-assisted etching (IBAE) a SI (100) GaAs substrate, and the *p*-type epilayers are grown by organometallic vapor phase epitaxy (OMVPE) atomic layer epitaxy (ALE). The wraparound contact pads are created by a lift-off and anneal process using a two-layer resist and an angled-evaporation metallization scheme. The horizontal epilayers formed by ALE on the substrate and on the top of the rod not covered by the contacts are then removed by chlorine IBAE. The second etch isolates the test structures from one another and restricts conduction between the ohmic contacts to paths that are solely in the sidewall epilayers. A scanning electron micrograph (SEM) of a completed test structure is shown in Fig. 2.

The techniques used for rod formation, ALE overgrowth, wraparound contact formation, device/sidewall isolation, and electrical measurements are described in the following sections of the paper. We also discuss methods used to determine the carrier concentration and electrically active thickness of the vertical-sidewall epilayers.

ROD FORMATION

The rods that provide the sidewalls of the test structures are formed by chlorine IBAE. In this process, Ar^+ ions generated with a Kaufman ion gun impinge on a photoresist-masked sample that is simultaneously exposed to chlorine gas. The Ar^+ ions break As and Ga bonds on exposed GaAs horizontal surfaces, which in turn react with the chlorine to form $AsCl_3$ and $GaCl_3$. These species have high vapor pressures and in the vacuum of the etcher rapidly desorb from the sample surface. The direction of the impinging Ar^+ ions determines the slope of the sidewall, while the chlorine pressure determines the amount by which the etch rate is enhanced relative to the ion-milling rate. Typically, enhancements of 10 to 50 times the milling rate are observed. The crystallographic orientations of the wafer surface and sidewall play a secondary role in determining sidewall slope, so nearly vertical sidewalls can be generated by aligning the plane of the

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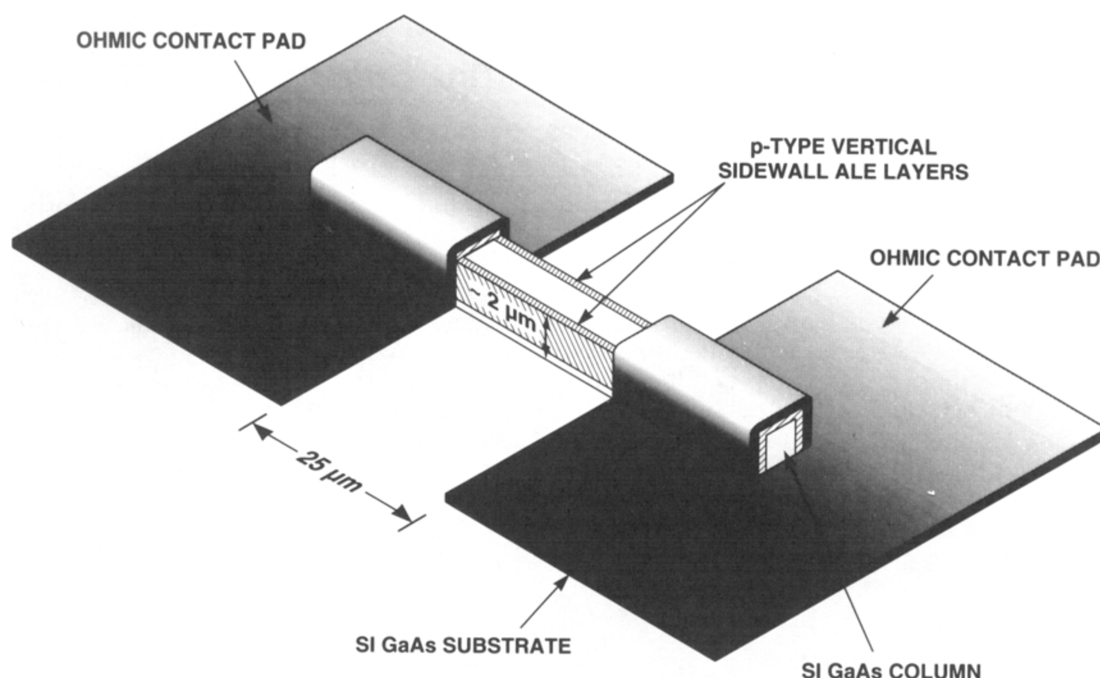

Fig. 1 — Schematic diagram of a test structure consisting of a GaAs rod with vertical-sidewall epilayers and wraparound ohmic contacts.

wafer-surface normal to the Ar^+ ion beam. Further details related to this process are available in the literature.[1,2]

The samples are patterned and masked by standard photolithographic techniques and etched using our typical IBAE parameters. An Ar^+ ion beam at 500 V, which produces a beam current density of 40 $\mu A\ cm^{-2}$, is employed in combination with a two-jet chlorine dispensing system. The pressures of the chlorine and Ar^+ at the sample surface as measured by a manometer are 2.8 and 0.1 mTorr, respectively. The measured etch rate of the (100) GaAs is about 100 nm min^{-1}.

An SEM of a portion of the sidewall and cleaved cross-section of an as-etched rod is shown in Fig. 3. The sidewall morphology is typical for our standard resist process. The slight departure of the sidewall from the wafer-surface normal is caused by divergence in the ion beam resulting from the grid configuration of the Kaufman gun which was configured for a high etch rate. The small undulations in the sidewall are due to edge roughness in the photoresist etch mask. The undulations can be reduced by using master photolithographic masks instead of copies during printing and by using a photoresist that yields more nearly vertical etch-mask sidewalls.

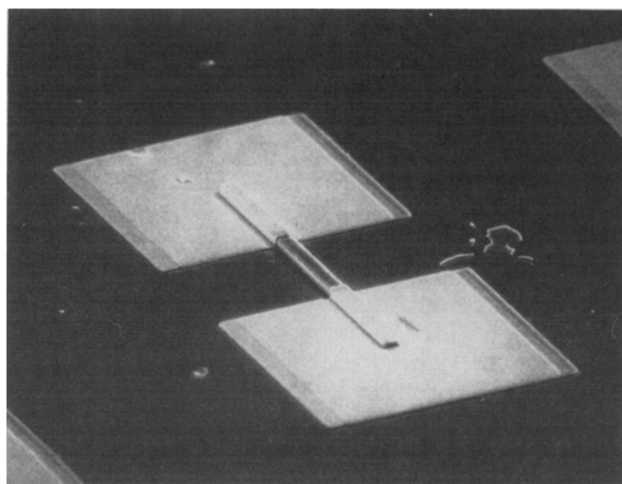

Fig. 2 — SEM showing a vertical-sidewall test structure.

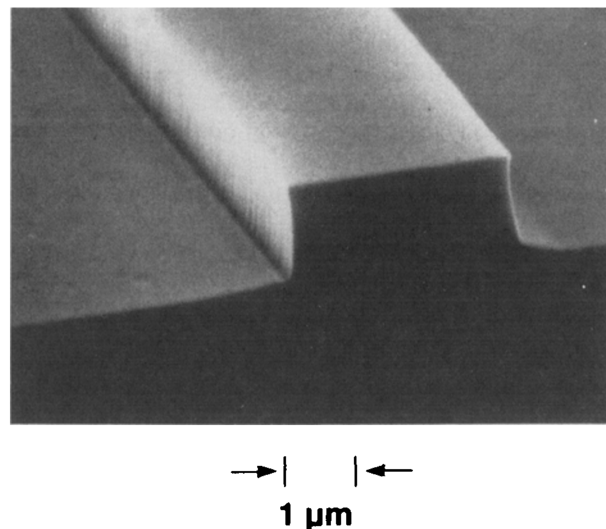

Fig. 3 — SEM showing a portion of the sidewall and cleaved cross section of an etched rod.

ALE OVERGROWTH

After the rods are formed, the wafer is overgrown by OMVPE ALE. Molecular beam epitaxy (MBE) and standard OMVPE were also considered as candidate growth techniques. OMVPE ALE was chosen because of its ability to produce conformal growth around the rods,[3] which enabled us to characterize the horizontal portions of the epilayers and use the results obtained in characterizing the vertical portions. The major shortcomings of the ALE process at this time are that it has a very low deposition rate and does not yield epilayers with very low background carrier concentrations. We chose to investigate *p*-type vertical-sidewall epilayers because our OMVPE ALE system produces such layers when no intentional doping is employed. As systems and source materials improve, however, OMVPE ALE should be able to produce *n*- and *p*-type doped epilayers with very low background carrier concentrations.

The rods were prepared for overgrowth by removing oxide buildup with a 1:1 HCl:deionized water dip followed by heat treatment at 700° C for 15 min in a hydrogen atmosphere with arsine overpressure to prevent decomposition of the GaAs. The heat treatment, which was performed in the OMVPE reactor just prior to overgrowth, caused a slight rounding of the corners of the rods, as shown in Fig. 4. The OMVPE reactor is a vertical rotating-disk unit that has been described previously.[4]

To optimize the ALE process for conformally overgrowing the rods and horizontal surfaces, we measured the ratio of vertical-sidewall epilayer thickness to horizontal epilayer thickness as a function of rod orientation. The rods were formed on a SI GaAs wafer with a surface orientation of (100), tilted 2° toward (110), in a spoke-like pattern and then overgrown with an interface marker epilayer of AlGaAs followed by 200 nm of GaAs. Reasonably conformal growth was obtained for rods aligned along the $[0\bar{1}1]$ direction. Figure 5 is an SEM of a cleaved cross section of one of the overgrown $[0\bar{1}1]$ rods. The AlGaAs layer has been enhanced by a mild selective etch. Other orientations gave various thickness ratios, indicating that our ALE process was not self-limiting for all orientations. Orientations for which the sidewall growth and horizontal growth rates are significantly different may be useful in fabricating low-dimensionality structures without further processing. Depending on the orientation, the structures could be fabricated either on the sidewalls or tops of the rods.

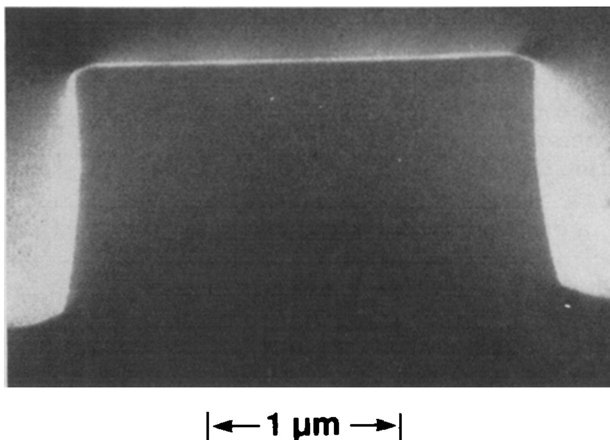

Fig. 4 — SEM showing a cleaved cross section of an annealed rod before overgrowth. Notice the slight rounding of the corners as compared to Fig. 3.

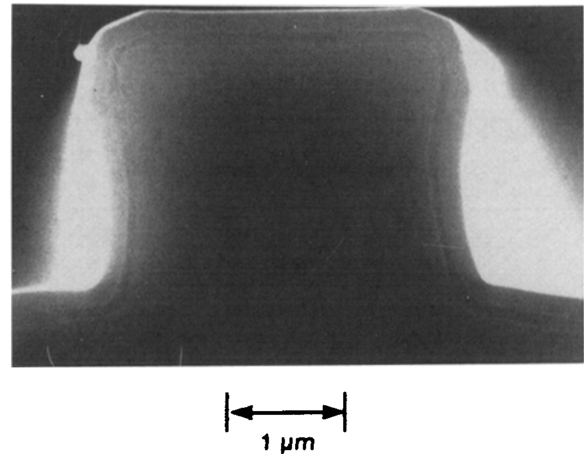

Fig. 5 — SEM showing a cleaved and stained cross section from an overgrown $[0\bar{1}1]$-oriented rod. AlGaAs was used as an interface marker layer.

During ALE growth the reactor pressure was 0.2 atm and the substrate temperature was 490° C. The trimethylgallium and arsine gas flow rates were 3 and 25 sccm, respectively, and the hydrogen-carrier and purge-gas flow rates were maintained at 10 l min^{-1}. Epitaxial GaAs was deposited on the rods and horizontal surfaces by using the following GaAs monolayer growth cycle: admit trimethylgallium for 1 s, purge with hydrogen for 3 s, admit arsine for 3 s, and purge with hydrogen for 3 s. Using the above parameters, we grew 200 nm of unintentionally doped GaAs around the rods, forming a *p*-type layer with a carrier concentration of about 2×10^{17} cm^{-3}. Transmission electron micrograph (TEM) and SEM characterization revealed that the epilayers were of excellent crystal quality with no mechanical defects.

WRAPAROUND CONTACT FORMATION

To make direct ohmic contact to the sidewall epilayers, we developed the procedure shown schematically in Fig. 6 for angled electron-beam evaporation and lift-off; the technique uses a thick, two-layer resist process and an annealed Au/Zn/Au metallization scheme.[5] The two-layer resist process, illustrated in Fig. 6(a) and 6(b), produces a resist sidewall profile with a large top-surface overhang. The overhanging structure protects the top portions of the resist sidewall from angled metal deposition and allows lift-off of metals deposited at angles up to 45° with respect to the normal of the wafer sur-

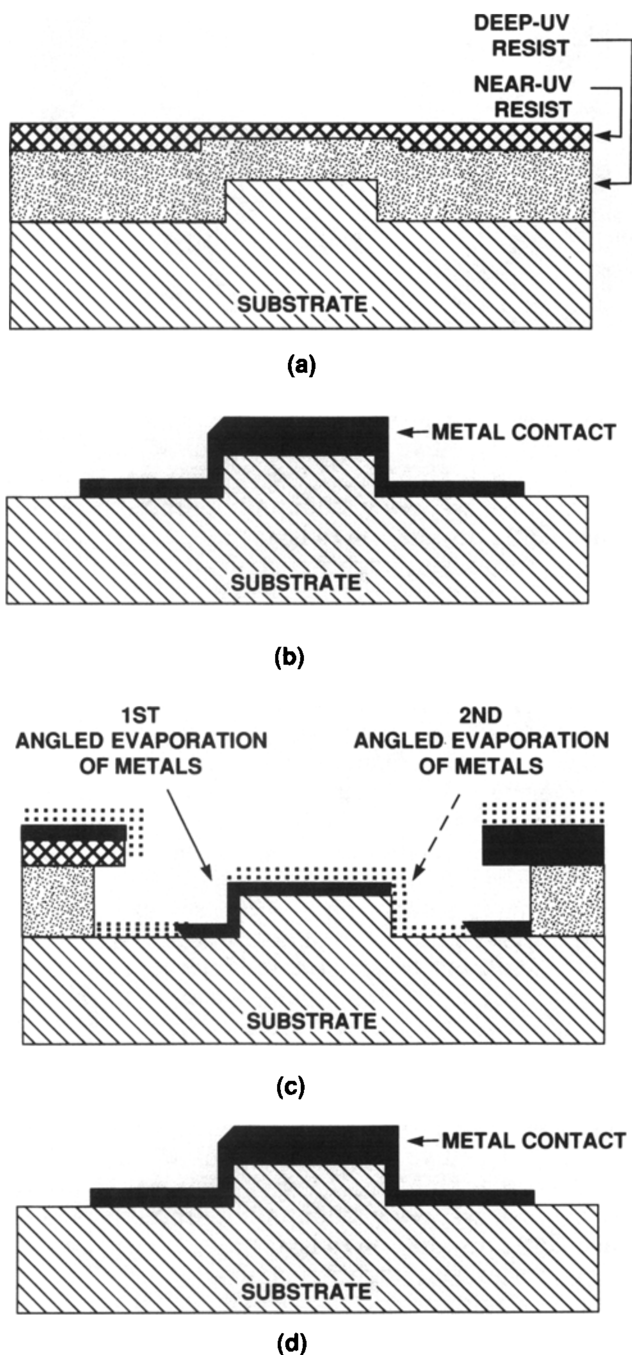

Fig. 6 — Schematic cross-sectional diagrams showing (a) two layers of resist applied over a rod, (b) the resists after exposure and development, (c) the coverage of the angled metal evaporations, and (d) a completed lift-off.

face. As shown in Fig. 6(c), metals are first deposited on one side of the rod, the wafer is turned 180°, and metals are then deposited on the other side, without stripping and reapplying the resists. The structure after lift-off is shown in Fig. 6(d).

In the two-layer resist process, a near-UV resist (AZ 1370sf) is spun over a deep-UV resist (polymethyl methacrylate). Figure 7(a) and 7(b) are SEMs showing gratings printed with the near-UV and deep-UV resists, respectively. After exposure and development of the near-UV resist, the wafer is ashed in a helium/oxygen plasma to remove near-UV resist scum in opened areas and then overexposed with deep-UV radiation using the near-UV resist pattern as the mask. The deep-UV resist is then developed with chlorobenzene, which undercuts the near-UV resist mask, forming the overhanging structure shown in Fig. 6(b). SEMs showing a sidewall and cross section of a grating line printed with this process are shown in Fig. 7(c) and 7(d), respectively.

After the formation of the lift-off mask, contacts consisting of 30 nm of Au, 50 nm of Zn, and 100 nm of Au are deposited with an evaporation angle of 45° to the ends of the rods in two applications, as shown in Fig. 6(c). After lifting off the excess metals with acetone, the contacts are annealed in nitrogen for 20 s at 420° C. The specific resistance of contacts to the horizontal portions of the epilayers, as measured by using a transmission-line pattern, is $5 \times 10^{-5}\ \Omega\ cm^2$. Figure 8 is a TEM showing the boundary of an annealed sidewall contact to the epilayer. The contact appears to be uniformly alloyed into the epilayer with an interface roughness of about 80 nm.

DEVICE/SIDEWALL ISOLATION

Before current saturation measurements can be performed, the test structures must be isolated from one another by removing the portions of the epilayers covering the horizontal surfaces between the rods. The portions deposited on the tops of the rods must also be removed. We chose to remove these horizontal portions by IBAE. The ohmic contacts were used as etch masks to protect the underlying portions of the horizontal and vertical surfaces, and the horizontal epilayers on the tops of the rods served as etchable masks to protect the vertical layers between the ohmic contacts. The etching time was sufficient to remove a layer of GaAs approximately 50 nm thicker than the measured epilayer thickness.

Isolation was confirmed by two types of electrical measurements. First, the resistance between contact pads on different rods was found to be in the mega-ohm range. Second, the saturation currents of single-rod structures (as shown in Fig. 1) and devices consisting of five rods connected in parallel were compared. A significant contribution to the saturation current by the horizontal epilayers would increase the saturation current of the five-rod device to more than five times that of a single rod. However, within the spread in the values measured for individual rods, the current saturation value for the five-rod devices was found to be just five times higher than that for the single-rod structures. This result leads us to conclude that the horizontal epilayers between the rods had been removed. We further conclude that the epilayers on the tops of the rods had also been removed since they were of the same thickness as the epilayers between the rods.

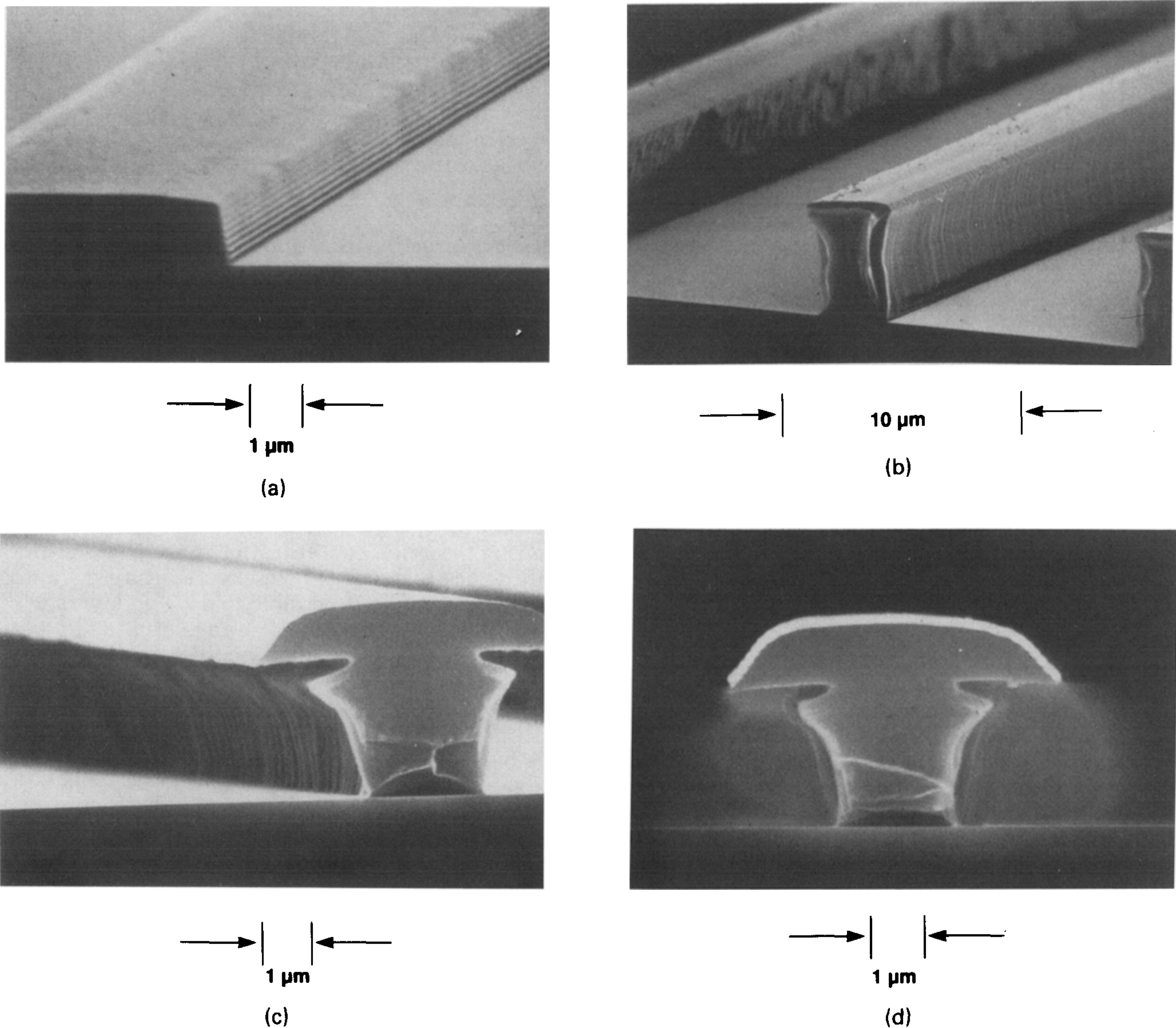

Fig. 7 — SEMs showing (a) near-UV resist patterned into a grating line, (b) deep-UV resist patterned into a grating line, (c) the sidewall of the near-UV resist over the deep-UV resist patterned into a grating line, and (d) a cross section of the grating line in (c).

ELECTRICAL MEASUREMENTS

Current saturation measurements performed on one-rod structures were used to determine the product of carrier concentration and channel thickness for the vertical-sidewall epilayers. The saturated current I_{sat} is given by

$$I_{sat} = 2qV_sZaN \tag{1}$$

where q is the electronic charge, V_s the carrier saturation velocity, Z the width of the channel, a the channel thickness less the depletion width, and N the carrier concentration.[6] The factor of 2 is included because each rod has two vertical-sidewall channels. By measuring I_{sat} and Z for the rod structure and determining V_s by an independent experiment, we are able to calculate the product of the carrier concentration and channel thickness.

The value of V_s was determined by performing current saturation measurements on structures formed by two large ohmic pads separated by 25 μm on two p-type 2×10^{17} cm^{-3} epilayers of different thicknesses grown by MBE on SI substrates. Applying Eq. (1) to the two layers gives two equations in two unknowns: V_s and the depletion width, which is assumed to be the same in both cases. Solving these equations gives $V_s = 2.4 \times 10^6$ cm s^{-1}.

Figure 9 shows a typical current-voltage (I–V) characteristic for a single-rod structure. From the measured value of I_{sat}, the carrier-concentration/thickness product for this structure is found to be 1.5×10^{12} cm^{-2}. Hall and transmission-line measurements on the horizontal epilayers between the test structures give a carrier concentration of 2.2×10^{17} cm^{-3}, a total depletion width of 145 nm (which includes both substrate and surface depletion), and a carrier-concentration/thickness product of $1.2 \times$

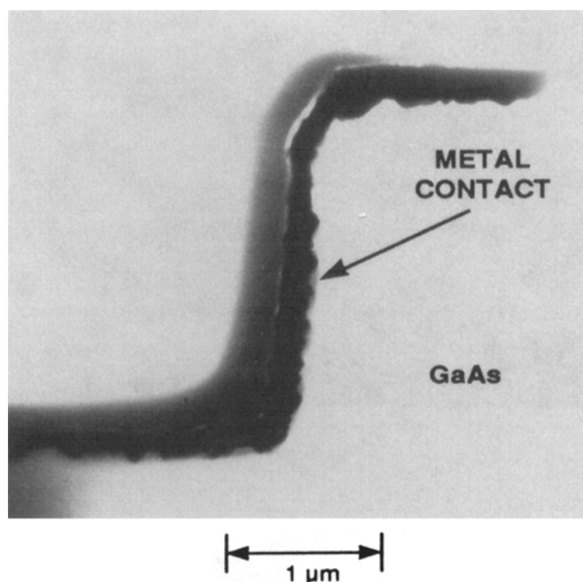

Fig. 8 — Cross-sectional TEM showing the interface between a GaAs ALE layer and an annealed ohmic contact. The interface roughness is about 80 nm.

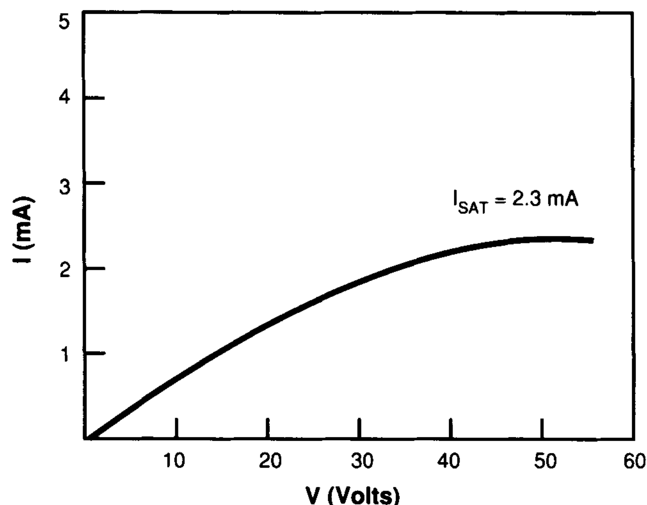

Fig. 9 — I-V characteristic of a typical single-rod device.

10^{12} cm^{-2}. The discrepancy in the two carrier-concentration/thickness products may be either due to measurement errors or differences in the properties of the vertical and horizontal epilayers. The variations may be in the carrier concentrations, the depletion widths or a combination of both. Assuming the same depletion widths for the vertical epilayers as the horizontal epilayers, we obtain an active channel width for the device of 55 nm (200 nm–145 nm), which corresponds to a vertical-epilayer carrier concentration of about 2.8×10^{17} cm^{-3}. We believe that the difference between the carrier-concentration/thickness products may be real. The interface between the vertical epilayers and the substrate may be of higher quality than that between the horizontal epilayer and the substrate, because the etch damage on the sidewalls of the rods is less than that on the horizontal surfaces[6] and therefore may be fully annealed during overgrowth. The sidewall orientation may also affect the amount of dopant in the vertical-sidewall epilayer. The effect of orientation on dopant incorporation has been observed in both MBE[7] and OMVPE.[8]

SUMMARY

We have developed techniques for device fabrication on the vertical sidewalls of etched rods in GaAs and demonstrated these techniques by the fabrication of rod test structures. Current-saturation measurements of the product of carrier concentration and channel thickness in the *p*-type vertical-sidewall epilayers show that these epilayers have sufficient carrier concentration to support a sidewall device technology. We expect future advances in ALE will make it possible to dope epilayers with a wide carrier-concentration range of *n*- and *p*-type dopants. With this capability, a high-device-density vertical-sidewall technology would be feasible. Further work in this area could lead to discrete devices with properties uniquely different from those that can be obtained with planar technology. For example, the fabrication of laser, waveguide, and quantum-confinement structures grown with reduced dimensionality could be considered.

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REFERENCES

1. M. W. Geis, G. A. Lincoln, N. Efremow and W. J. Piacentini, J. Vac. Sci. Technol. *19,* 1390 (1981).
2. W. D. Goodhue, G. D. Johnson and T. H. Windhorn, in Gallium Arsenide and Related Compounds 1986, ed. W. T. Lindley (IOP Publishing, Bristol, England, 1987), p. 349.
3. Y. Ide, B. T. McDermott, M. Hashemi, S. M. Bedair and W. D. Goodhue, Appl. Phys. Lett. *53,* 2314 (1988).
4. C. A. Wang, S. Patnaik, J. W. Caunt and R. A. Brown, J. Cryst. Growth *93,* 228 (1988).
5. H. J. Gopen and A. Y. C. Yu, Solid-State Electron. *18,* 331 (1975).
6. S. W. Pang, W. D. Goodhue, T. M. Lyszczarz, D. J. Ehrlich, R. B. Goodman and G. D. Johnson, J. Vac. Sci. Technol. *B6,* 1916 (1988).
7. D. L. Miller, J. Vac. Sci. Technol. *B4,* 655 (1986).
8. K. Okamoto, M. Furuta and K. Yamaguchi, Jpn. J. Appl. Phys. *27,* L2121 (1988).