Journal of Electronic Materials, Vol. 21, No. 12, 1992

High Gain AlInAs/GaAsSb/AlInAs NpN HBTs on InP

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We report the first growth and characterization of high gain double heterojunction NpN HBTs on InP with a lattice-matched $GaAs_{.5}Sb_{.5}$ base layer. This AlInAs/GaAsSb heterojunction has almost no discontinuity in the conduction band edge, eliminating the need to grade the emitter-to-base heterojunction to achieve optimal carrier injection. The layers were grown in a solid source MBE system, using tetramer As_4 and Sb_4 sources. Be is an efficient acceptor in the GaAsSb, but the mobility is about half that measured in *p* type GaAs on GaAs substrates. The HBTs fabricated were large area mesa isolated transistors, with a beta of 80 at a current density of 2 kA/cm^2, and the gain remained high at lower current densities. The turnon voltage, V_{be}, is only 0.45 V at a current density of 2 A/cm^2.

Key words: GaAsSb, InP, HBT

I. INTRODUCTION

AlInAs/InGaAs/InP NpN HBTs lattice-matched to InP have been demonstrated to have higher speed than AlGaAs HBTs.[1] This higher performance is expected because of the higher electron mobility in InGaAs which reduces the base transit time, and the high saturated electron velocity in the InP collector drift region. The $Al_{.48}In_{.52}As/Ga_{.47}In_{.53}As$ heterojunction has a conduction band edge discontinuity of 0.55 eV, and the $InP/Ga_{.47}In_{.53}As$ heterojunction has a conduction band edge discontinuity of 0.23 eV. To get optimal electron injection and hole blockage at an emitter-to-base junction, both of these heterojunctions should be graded. The lattice-matched $GaAs_{.51}Sb_{.49}/Al_{.48}In_{.52}As$ heterojunction has a conduction band edge discontinuity of only 10 meV,[2] which is negligible at room temperature. This ungraded heterojunction has the optimal lineup for NpN HBTs. In this paper, we report on the MBE growth and properties of GaAsSb, and the first NpN HBTs fabricated using lattice-matched GaAsSb as the base layer.

Early work on growth of GaAsSb by LPE and OMVPE studied the tendency of GaAsSb to separate into two phases and found that this tendency was most pronounced in the alloys with similar As and Sb concentrations.[3-7] Lower OMVPE growth temperature resulted in less phase separation, but the reduction in the OMVPE growth rate at lower growth temperatures limited the minimum growth temperature to values in excess of about 530° C.[3]

GaAsSb/InGaAs superlattices lattice-matched to InP have grown by MBE at 500° C and have been characterized by a variety of techniques.[8] The undoped superlattices were n-type, so no data about hole transport in GaAsSb could be inferred. Thicker, not intentionally doped layers of GaAsSb have been grown by MBE over the temperature range 470° to 560° C. These resulted in *n* type layers, with the best electron transport properties for a growth temperature of 510° C.[9] The very narrow low temperature photoluminescence line width (7 meV)[9,10] for MBE GaAsSb grown at this low temperature suggests that the phase separation is minimal. Other reports on GaAsSb layers grown by MBE did not describe the hole transport properties of the GaAsSb.[11-15]

II. MBE GROWTH AND BULK PROPERTIES

The layers were grown in a solid source MBE system, using tetramer As_4 and Sb_4 sources. The substrates were (100) oriented semi-insulating Fe doped InP. The growth temperature was measured using a pyrometer and is believed to be accurate to within a few degrees. The alloy composition of the GaAsSb was controlled by adjusting the Sb flux to the desired value using a calibrated flux ion gauge (assuming unity Sb incorporation coefficient), and supplying slightly more than the minimum As_4 flux necessary for group V stabilized growth. Any arsenic which is not required should reevaporate.[16]

In preparation for the growth of NpN HBTs, the properties of GaAsSb doped with Be were studied. The typical sample consisted of a 0.5 μm undoped AlInAs buffer layer, a 0.2 μm Be doped GaAsSb layer, and a 200Å undoped AlInAs cap. The results of this doping study are summarized in Table I. The initial two growths (#2861 and 2862) were identical except for growth temperature. The lower growth temperature resulted in much higher conductivity material, due to much higher hole mobility. This may be due to reduced phase separation at the lower growth temperature resulting in reduced alloy scattering. However, x-ray measurements discussed below suggest that the higher growth temperature sample may have dislocations in the GaAsSb. The better mobility at the lower growth temperature prompted a series of growths at the lower temperature to study Be incorporation.

(Received June 5, 1992)

0361-5235/1992/1401-1123$5.00©92 TMS

Table I. Room Temperature Hall Measurements of GaAsSb

Sample	Growth Temp. [° C]	Hole Conc. [cm^{-3}]	Hole Mobility [cm^2/Vs]	Comment
2861	470	5.8e18	78	Random Alloy
2862	520	8.0e18	32	Random Alloy
2863	470	6.1e18	75	Random Alloy
2864	470	2.4e19	44	Random Alloy
2865	470	2.4e19	38	Superlattice
2866	470	5.3e19	29	Random Alloy

A series of layers were then grown at 470° C with different Be fluxes to verify doping efficiency. These resulted in layers where the hole concentration scaled with the Be flux, indicating efficient incorporation of the acceptors. For sample #2865, the As and Sb shutters were sequenced in a manner which should have produced a short period superlattice, consisting of alternately two monolayers of GaSb and two monolayers GaAs. We hoped that intentional separation of the random alloy into the two phases in a superlattice would reduce alloy scattering and improve the low field Hall mobility. The mobility of the attempted superlattice layer structure was somewhat lower than the random alloy mobility. X-ray characterization of this layer found no satellite peaks, so that it is not clear whether intentional modulation of the As and Sb fluxes resulted in a GaAs/GaSb superlattice.

The hole mobility at a given concentration of these GaAsSb layers was about half the hole mobility in bulk Be doped GaAs on GaAs or InGaAs on InP. This is very significant because good high frequency performance of an HBT depends on the thin base layer having high sheet conductivity. How much the mobility of GaAsSb can be improved by optimizing growth conditions is not clear.

Double crystal (400) X-ray characterization of these layers was difficult to interpret. The two peaks expected were an AlInAs peak and a GaAsSb peak, in addition to the InP substrate peak. The 520° C growth (#2862) is the only layer showing the expected two additional peaks. The peak associated with the AlInAs is 400 arcsec from the substrate with a FWHM of 85 arcsec, which is consistent with this layer being pseudomorphic. The peak associated with the GaAsSb was 1400 arcsec from the substrate peak with a FWHM of 300 arcsec. If the GaAsSb is assumed to be pseudomorphic, this peak separation corresponds $GaAs_{.59}Sb_{.41}$. It is more likely that the layer has relaxed, in which case the alloy composition would be $GaAs_{.66}Sb_{.34}$. This shift in alloy composition is consistent with greater loss of Sb at this higher growth temperature. Lower growth temperatures should result in less Sb evaporation, improving the lattice match. All of the samples grown at 470° C have only a single additional peak, located a few hundred arcsec from the substrate peak on the side of smaller unstrained lattice constant. The FWHM of this single peak is typically 100 to 200 arcseconds. One hundred arcseconds of peak separation corresponds to a mismatch ($\Delta a/a$) of 8×10^{-4}. While these thicker layers may not be fully pseudomorphic, the GaAsSb layer in the base of the transistors discussed below almost certainly is pseudomorphic. We suspect that the GaAsSb is autolattice matching to the AlInAs, resulting in a single additional peak. It is also possible that one of the epitaxial layers failed to produce a resolvable x-ray peak at the lower growth temperature.

III. HBT FABRICATION AND CHARACTERIZATION

Several HBT layer structures were grown at 470 and 500° C. The layer structure is listed in Table II. Silicon doped GaInAs is used in the subcollector because it has a higher maximum electron concentration and higher mobility, relative to AlInAs. AlInAs is desirable in the collector drift region, because its larger band gap should result in a larger breakdown field in the collector depletion region. The undoped "setback" layers on either side of the doped GaAsSb base layer are to prevent any diffusion of the beryllium into the wide gap AlInAs, which would produce a spike in the conduction band edge and interfere with transistor operation. To determine the low frequency current gain characteristics, large area (70 μm × 70 μm) mesa isolated transistors were fabricated.

Figure 1 shows the Gummel plot of the transistor with the best characteristics. It was grown at 500° C. It has a very low turn on voltage of 0.45 V at J =

Table II. The Epitaxial Layer Structure for Lattice Matched AlInAs/GaAsSb/AlInAs NpN HBT on InP

Layer	Material	Thickness (Å)	Composition [X]	Doping (cm^{-3})
Ohmic contact	$Ga_xIn_{1-x}As$	500	.47	5E18
Emitter	$Al_xIn_{1-x}As$	500	.48	1E18
Base setback	$GaAs_xSb_{1-x}$	100	.51	undoped
P type base	$GaAs_xSb_{1-x}$	800	.51	2e19
Base setback	$GaAs_xSb_{1-x}$	100	.51	undoped
Drift	$Al_xIn_{1-x}As$	2000	.48	5E16
Collector	$Al_xIn_{1-x}As$	500	.48	1E18
Subcollector	$Ga_xIn_{1-x}As$	5000	.47	5E18
Substrate	(100)InP	—	—	semi-insulating

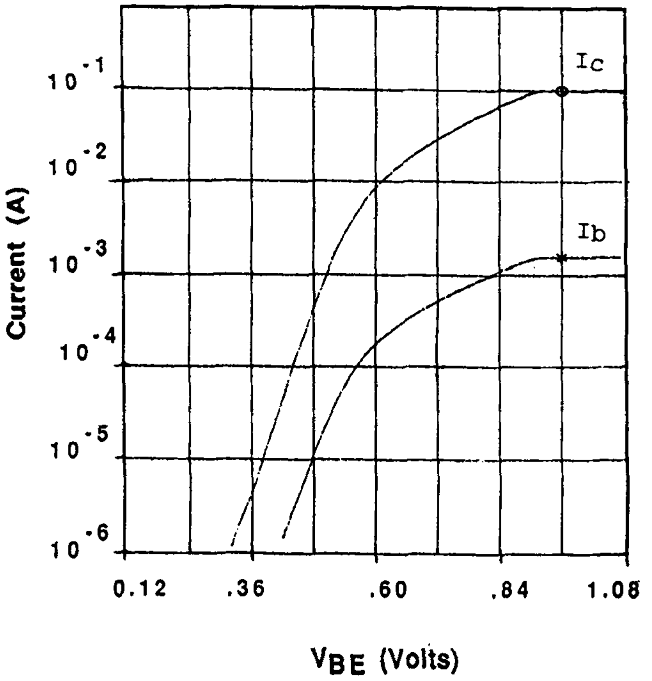

Fig. 1 — Gummel plot of an AlInAs/GaAsSb NpN HBT grown at 500° C.

2 A/cm^2, a gain greater than 80 at J = 2 KA/cm^2, and retains good gain to low current density. This turnon voltage is similar to the lowest turnon voltages measured for graded junction AlInAs/GaInAs HBTs. Figure 2 shows the common emitter transistor characteristics of this HBT. The breakdown voltage is larger than 6 Volts. The output conductance in the characteristics is believed to be due to a spike forming in the conduction band edge on the collector side of the base, caused by beryllium diffusion into the AlInAs collector. This spike is pulled down with increasing reverse bias on the collector, improving the collection of electrons from the base. The HBTs grown at 470° C showed a similarly low turnon voltage, but much lower gain.

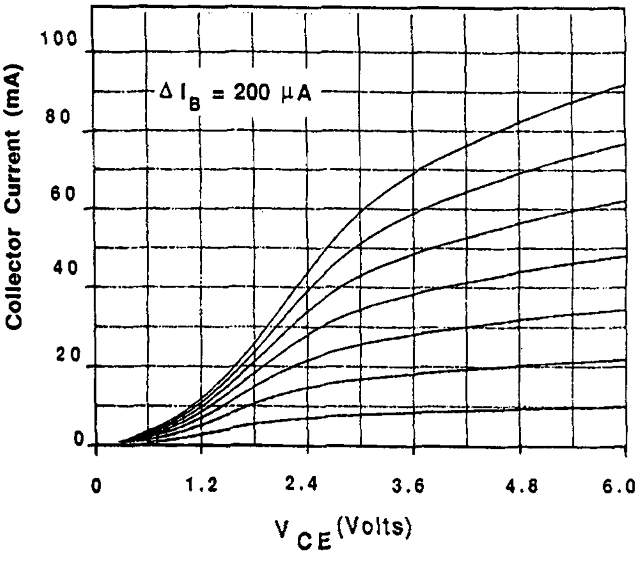

Fig. 2 — Common emitter transistor characteristics of an AlInAs/GaAsSb NpN HBT grown at 500° C.

IV. SUMMARY

In summary, GaAsSb layers lattice matched to InP have been grown by MBE. Be is shown to be an efficient acceptor, but the low field Hall mobility is about half the hole mobility in similarly doped GaAs on GaAs or InGaAs on InP. High gain AlInAs/GaAsSb NpN HBTs have been demonstrated on InP substrates. The HBTs show very low turnon voltages, high gain, and retain high gain to low current densities.

REFERENCES

1. J. F. Jensen, W. E. Stanchina, R. A. Metzger, T. Lui and T. V. Kargodorian, Device Research Conference, Boulder, CO (1991).
2. Y. Nakata, Y. Sugiyama, O. Ueda, S. Sasa, T. Fuji and E. Miyauchi, J of Cryst. Growth *99*, 311 (1990).
3. M. J. Cherng, Y. T. Cherng, H. R. Jen, P. Harper, R. M. Cohen and G. B. Strinfellow, J. Electron. Mater. *15*, 79 (1986).
4. M. Astles, H. Hill, A. J. Williams, P. J. Wright and M. L. Long, J. Electron. Mater. *15*, 41, (1986).
5. M. J. Cherng, G. B. Strinfellow, D. W. Kisker, A. K. Srivastava and J. L. Zyskind, Appl. Phys. Lett. *48*, 419 (1986).
6. A. I. Kazakov, I. N. Kishmar, A. E. Bochkarev and L. M. Dolginov, J. Cryst. Growth *116*, 204 (1992).
7. I. T. Ferguson, A. G. Norman, B. A. Joyce, T-Y. Seong, G. R. Booker, R. H. Thomas, C. C. Phillips and R. A. Sttradling, Appl. Phys. Lett. *59* (25), 3324, (1991).
8. J. F. Klem, S. R. Kurtz and A. Datye, J. Cryst. Growth *111*, 628, (1991).
9. Y. Nakata, T. Fujii, A. Sandhu, Y. Sugiyama and E. Miyauchi J. Cryst. Growth, *91*, 655 (1988).
10. J. Klem, D. Huang, H. Morkoc, Y. E. Ihm and N. Otsuka, Appl. Phys. Lett. *50*, 1364 (1987).
11. Y. Sugiyama, T. Fujii, Y. Nakata, S. Muto and E. Miyauchi, J. Cryst. Growth *95*, 363 (1989).
12. H. Sakaki, L. L. Chang, R. Ludeke, C-A. Chang, G. A. Sai-Halasz and L. Esaki, Appl. Phys. Lett. *31*, 211 (1977).
13. C-A. Chang, R. Ludeke, L. L. Chang and L. Esaki, Appl. Phys. Lett. *31*, 759, (1977).
14. T. Waho, S. Ogawa and S. Maruyama, Jpn. J. Appl. Phys. *16*, 1875, (1977).
15. H. Yamaguchi, Y. Takeda and H. Oyanagi, p. 389, Inst. Phys. Conf. Ser. #120; "GaAs and Rel. Compounds" (1991).
16. K. R. Evans, C. E. Stutz, P. W. Yu and C. R. Wie, J. Vac Sci. Tech. B *8*, 271, (1990).