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Cadmium Sulfide Surface Stabilization for InP-Based Optoelectronic Devices

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Thin layers of chemical bath deposited cadmium sulfide were used to improve the surface and interface properties of InP and its latticed-matched III-V compounds. X-ray photoelectron spectroscopy indicates chemical reduction of surface oxides and the prevention of subsequent group III or V oxide formation. Photoluminescence spectra, measured between 1.0 and 1.3 μm, indicate a dramatic reduction in phosphorus vacancies following CdS treatment. Metal-insulator-semiconductor capacitors fabricated on *n*-type InP substrates with CdS interlayers display near-ideal quasi-static response and interface-state densities in the low 10^{11}/eVcm^2 range. Thin CdS layers were used to passivate the surface of InAlAs/InGaAs high electron mobility transistors (HEMTs) and metal-semiconductor-metal (MSM) photodetectors. After CdS treatment, Schottky diode barrier heights of 0.6 eV were regularly obtained. For HEMTs, drain-to-gate current ratios of 8×10^4 were observed after CdS treatment. For a new backside illuminated MSM design, the dark current of CdS-treated samples was reduced three orders of magnitude to below 1 nA.

Key words: III-V semiconductors, cadmium sulfide, InP, interface, metal-insulator-semiconductor (MIS), passivation, Schottky barrier

INTRODUCTION

InP and lattice-matched III-V compounds are recognized as desirable materials for high frequency opto-electronic circuits. Lattice-matched and strained ternaries and quaternaries of InGaAlAs or InGaAsP on InP allow the production of high electron mobility transistors (HEMTs), heterojunction bipolar transistors (HBTs), optical detectors, lasers, and other critical opto-electronic devices. Although high quality epitaxial material is commercially available, the ability to form well-behaved interfaces between the epitaxial semiconductor and insulators or Schottky metals remains elusive.

A variety of techniques have been used to reduce or eliminate the effects of problematic surface chemistry on device behavior. Thin interfacial layers of elemental silicon (~1 nm) have been used to improve the performance of GaAs- and InGaAs-based metal insulator semiconductor field effect transistors (MISFETs).[1] The silicon interfacial layer terminates the III-V semiconductor surface, reducing the interface-state density. After insulator deposition, the resulting MIS structure exhibits modulation of the surface Fermi level throughout the bandgap.[2] Others have investigated various compounds, such as zinc selenide, to improve the surface properties of GaAs. ZnSe, a wide bandgap II-VI semiconductor which nearly lattice matches GaAs, was used as the insulator in an MIS structure.[3] Interface-state densities obtained for the ZnSe/GaAs system were comparable to densities obtained for the well established AlGaAs/GaAs system. Annealing the epitaxial layers after growth, resulting in the formation of Ga_2Se_3 at the ZnSe/GaAs (100) interface, is believed to be the critical factor in obtaining good electrical performance.

The electrical characteristics of GaAs/AlGaAs-based HBTs,[4] InP-based MISFETs,[5] and InP/InGaAs metal-

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semiconductor-metal (MSM) photodetectors[6] have been improved by treating samples in sulfur-bearing solutions. Sulfur passivation is typically performed in a heated chemical bath of ammonium sulfide. In the case of InP, sulfur has been shown to replace phosphorus at the surface, resulting in a thermodynamically favored and stable In_2S_3 passivating layer.[7] Chemical vapor deposited gallium sulfide has also been proposed as a possible passivant for GaAs surfaces.[8]

We are investigating the use of cadmium sulfide (CdS) as an interlayer to improve the electrical characteristics of the InP/insulator interface and the InP-based III-V/Schottky-metal junction. CdS is a wide-bandgap (2.42 eV) II-VI semiconductor. The lattice constant of the zinc-blende crystal matches within 0.6% of crystalline InP. Metastable zinc-blende CdS layers have been grown epitaxially on (110) InP by molecular beam epitaxy[9] and (100) InP by pulsed laser deposition.[10] Recently, hexagonal phase CdS grown on (111) InP by chemical bath deposition (CBD) has been reported.[11] The CBD technique, originally developed for solar cell applications, is readily adapted for use as a passivating process. As with previously reported sulfur passivation procedures, the chemical bath technique chosen for this investigation uses an ammonia-rich solution.

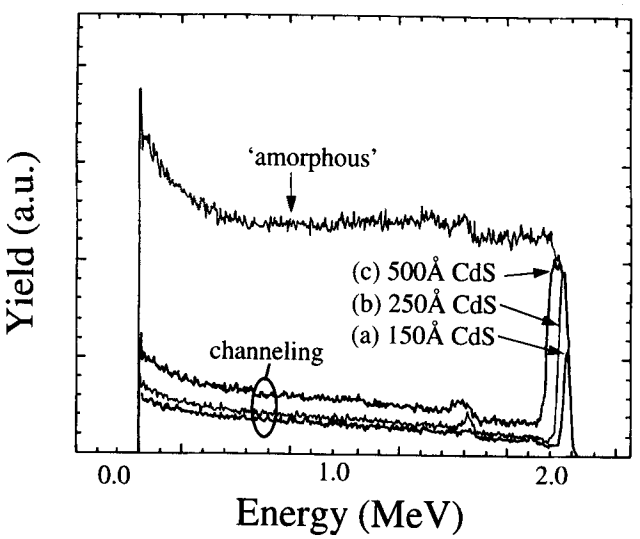

Fig. 1. Backscattering yields from simulated amorphous and (a) 150, (b) 250, and (c) 500Å CdS films on (100) InP substrates.

EXPERIMENTAL

The samples were prepared by chemical bath deposition in a solution of VLSI grade ammonium hydroxide (NH_4OH), hydrated cadmium sulfate ($3CdSO_4 \cdot 8H_2O$), and thiourea ($CS(NH_2)_2$). Concentrations used in this study were 0.028M thiourea, 0.014M $CdSO_4$, and 11M NH_3. Growth times ranged from 10 s to 10 min at growth temperatures of 60–80°C. The growth rate is sensitive to the concentration of NH_3, decreasing as the NH_3 concentration is raised.[12] A relatively high concentration of NH_3 was selected for this study, as only very thin layers of CdS (approximately 50–70Å) were desired for surface passivation; in addition, high NH_3 concentrations promote the removal of native oxides. Growth rates of CdS layers studied were approximately 20Å/min. Our standard growth for passivation consisted of a 3.5 min deposition at 75°C with the above concentrations. Following growth, the samples were rinsed in deionized water and dried with nitrogen.

Surface topography was investigated with a TopoMetrix model TMX2000 Discoverer atomic force microscope (AFM). A 9 mm scanner was used in constant force mode at approximately 1.0 nN. X-ray photoelectron spectroscopy (XPS) was performed with a Physical Electronics PHI 5100 XPS system with non-monochromatic Mg K_α radiation at 1253.6 eV. The anode was operated at 15 KV with an incident power of 400W. Spectra were recorded at normal

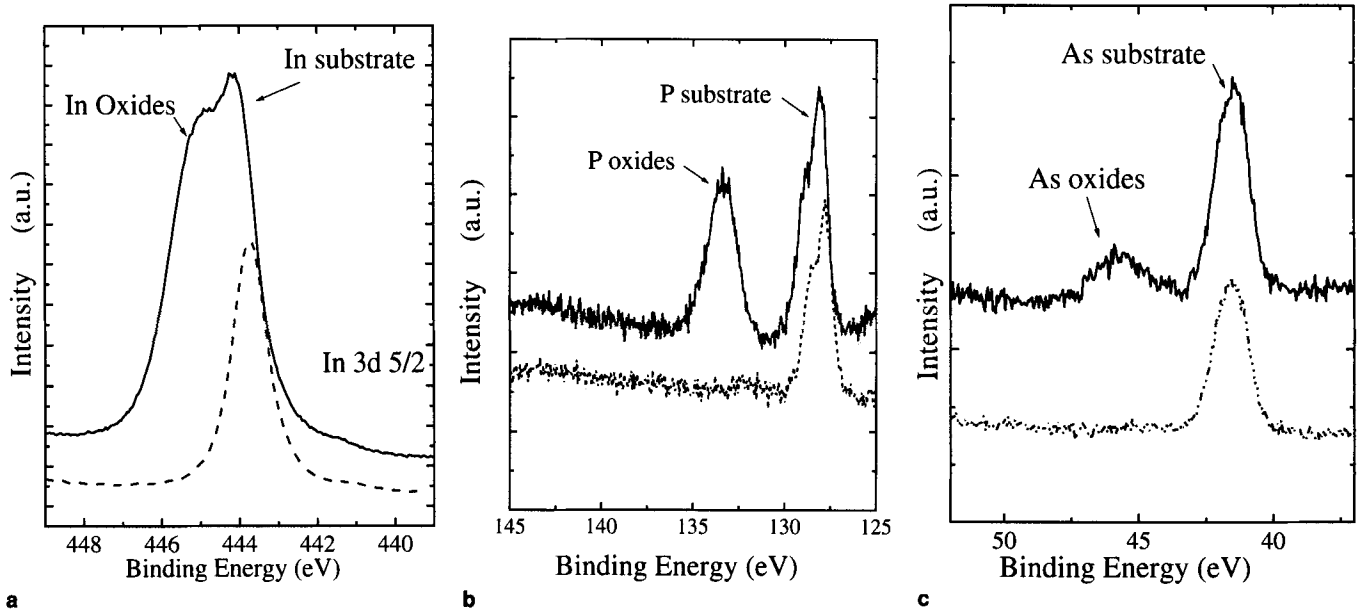

Fig. 2. XPS analysis of CdS-treated InP and InAlAs (a) In 3d, (b) P 2p, (c) As 3d. Upper curves are before CdS treatment, lower curves are after CdS treatment.

incidence to the surface. The spectra were corrected for charging effects by referencing the carbon 1s peak to 284.8 eV. After baseline subtraction, the widths, heights, and positions of Pearson peaks were fitted to the spectra for nonlinear least square optimization. Auger analysis was performed with a Perkin Elmer PHI 660 scanning Auger microprobe. An argon ion-beam was used to sputter samples for depth profiling. Photoluminescence (PL) spectra were measured at 4K by immersing the samples in liquid helium. An optical fiber in contact with the sample surface delivered the chopped signal from a 5145Å Ar laser and also collected the generated luminescence.

RESULTS

AFM was used to determine the average roughness of deposited films on InP substrates. For a CdS film grown for 3.5 min, with a layer thickness of 50–70Å, AFM scans revealed an increase in average peak-to-peak roughness from 6Å for HF-etched InP to 15Å for the CdS-treated sample. XPS measurements of the deposited layers revealed peak energies for the Cd $3d_{5/2}$ and S 2p signals that agreed with XPS measurements of pure CdS, as well as previously published data for evaporated CdS films.[13] Auger measurements on ~500Å films also showed bulk cadmium to sulfur ratios near unity. Strong suppression of the In and P substrate XPS peaks with CdS films of approximately 150Å, in addition to AFM profiles, suggests complete and relatively smooth coverage.

Rutherford backscattering (RBS) was used to investigate the crystalline quality of CdS films deposited on (100) InP substrates. Figure 1 shows the backscattered signals for an incident 2.275 MeV $^4He^{++}$ beam off a simulated amorphous sample and three InP substrates with different CdS layers. The angle between the incident $^4He^{++}$ beam and the detector was 100°. The random (amorphous) signal was simulated by precessing a rotating substrate about a cone tilted from the channeling orientation. The three channeled curves display a lack of crystallinity in the deposited layer, as indicated by the peaks in the backscattered signals at high energies. Figure 1, curves (a), (b), and (c) correspond to approximate CdS layer thicknesses of 150, 250, and 500Å, respectively. Magnitude and width of the backscattered peaks increase monotonically with layer thickness, indicating the films are not single crystalline.

XPS was used to investigate the effects of the CdS deposition process on the native oxides of InP. An InP sample was oxidized in an ozone-rich atmosphere at 300°C for 10 min. The oxide peaks of In and P are clearly shown in the upper XPS curves of Fig. 2a and 2b following the ozone-assisted oxidation. The sample was then placed in the CdS chemical bath for 3.5 min under standard conditions. The group III and V oxide peaks are greatly reduced, as shown in the lower curves of Fig. 2a and 2b. Similar results were obtained for InAlAs lattice matched to InP. The As 3d signals are shown in Fig. 2c before (upper curve) and after (lower curve) treatment. The group III oxides (not shown) were also greatly reduced after CdS treatment. The InAlAs sample was not intentionally oxidized prior to CdS treatment.

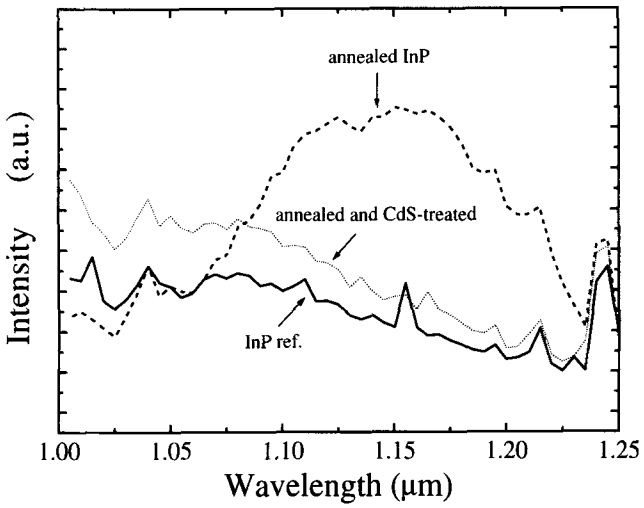

Fig. 3. 4K PL spectra of cleaved InP (solid), InP after 400°C anneal (dashed), and InP after anneal and CdS treatment (dotted).

PL at 4K was used to investigate the role of sulfur in passivating the surface of *n*-type (100) InP. If phosphorus vacancies are present near the sample surface, a broad luminescence peak centered at 1.15 μm should be observed.[14] The solid line spectrum of Fig. 3 was taken from a sample cleaved from the center of a wafer before any processing steps that might be detrimental to the surface were performed. Within the sensitivity of our instrumentation, there was no luminescence observed at the wavelengths associated with phosphorus vacancies. Phosphorus vacancies were intentionally created in this sample by annealing at 400°C for 1 min in forming gas (3% H_2 in N_2), as shown in the dashed line spectrum of Fig. 3. A distinct peak centered at 1.15 μm is observed. Treating the thermally damaged sample in the CdS chemical bath for 3.5 min at standard concentrations restored the spectrum to its original shape, as shown in the dotted line spectrum of Fig. 3. A probable explanation for the elimination of the 1.15 μm peak is that sulfur fills phosphorus vacancies in the initial phase of CdS film growth. Auger depth profiles also indicate a sulfur-rich interfacial layer at the CdS/InP interface.

The effect of thin CdS interlayers on the electrical characteristics of MIS structures was investigated with standard capacitance-voltage (C-V) analysis. For fabrication of MIS structures, the substrates were undoped (100) InP ($n = 1 \times 10^{16}$ cm^{-3}). Samples were prepared with and without CdS treatment. A 600Å SiO_2 insulator was deposited by a previously reported low-temperature, low-pressure CVD technique at 270–290°C and a pressure of 3 Torr.[15] TiAu contacts were then deposited by electron-beam evaporation through a shadow mask. After metallization, the samples were annealed at 350°C in dry nitrogen for 12 h.

For the CdS-treated samples, well-defined regions

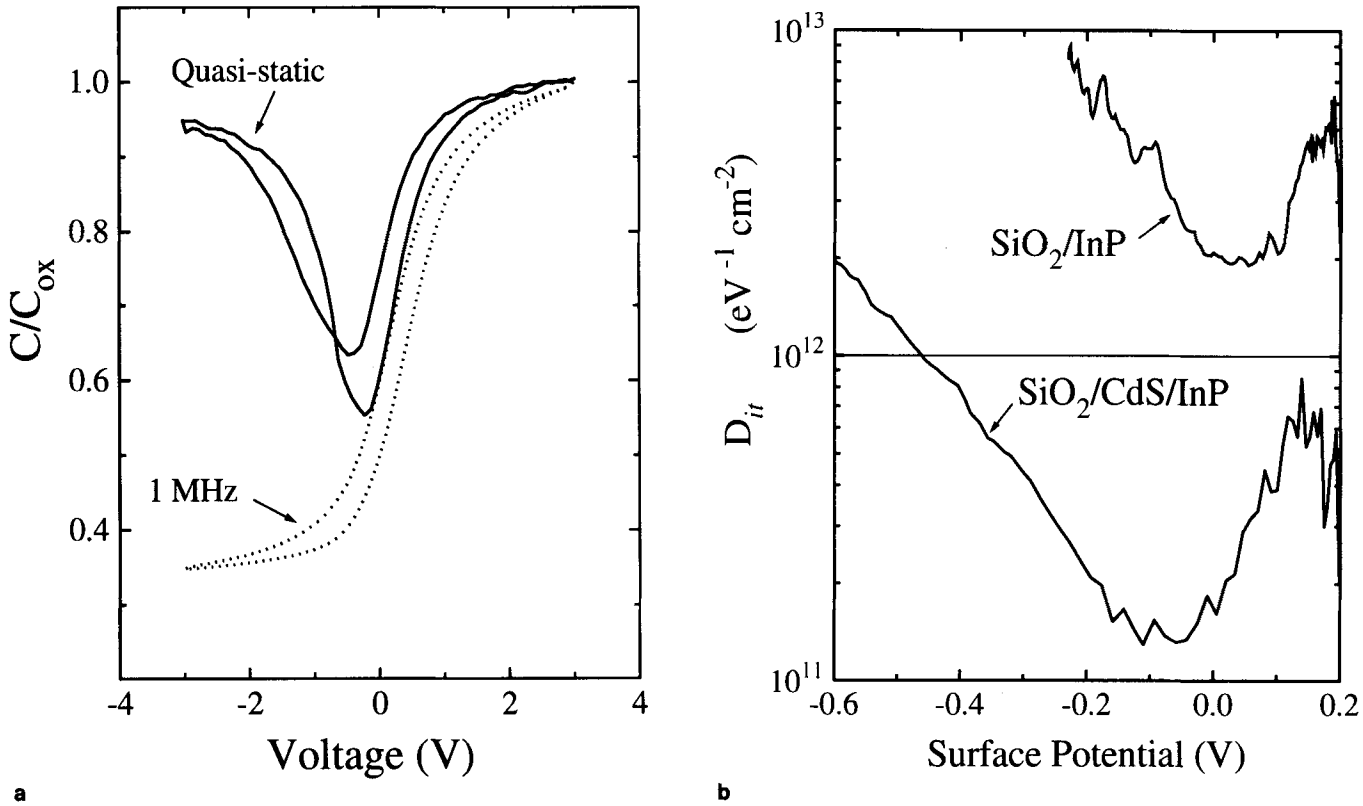

Fig. 4. (a) Quasistatic and 1MHz C-V curves of CdS-treated InP MIS capacitor, (b) D_{it} vs surface potential for an SiO_2/InP reference, and an SiO_2/CdS/InP structure using high-low method.

of accumulation, depletion, and inversion were observed in the room temperature quasi-static C-V response, as shown in Fig. 4a. D_{it} values calculated using the combined high-low frequency method of Castagné and Vapaille[16] are shown in Fig. 4b. The minimum interface-state density of a reference SiO_2/InP structure is typically above 10^{12} /eVcm^2. The minimum interface-state density of an SiO_2/CdS/InP structure is typically reduced by an order of magnitude, to 10^{11}/eVcm^2. We believe the lower interface-state density can be attributed to the reduction of substrate oxides and the filling of phosphorus vacancies at the InP surface. More detailed investigations of the SiO_2/CdS/InP capacitor have been reported.[17,18]

HEMT FABRICATION AND RESULTS

The CdS interlayers were used in an InGaAs/InAlAs HEMT process. HEMT layers were grown lattice matched on (100) semi-insulating InP by molecular beam epitaxy (MBE) in the following sequence: 2000Å InAlAs buffer, 400Å InGaAs channel, 40Å InAlAs spacer, 200Å InAlAs donor ($n = 4 \times 10^{18}$ cm^{-3}), 200Å InAlAs barrier, and 100Å InGaAs cap. The epitaxial layers are shown in Fig. 5a. Mesas were formed with a phosphoric acid-based etch. After removing the photoresist, our standard CdS surface treatment was used on some samples. SiO_2 was deposited at 270°C to encapsulate the sample surface (Fig. 5a). AuGeNi contacts were formed with a liftoff process after etching openings in the oxide layer.

Oxide deposition was found to have an adverse effect on mesa isolation. Samples treated with CdS prior to oxide deposition were seen to have less leakage between InAlAs/InGaAs mesas. Figure 6 compares the surface leakage of CdS-treated and untreated samples after oxide deposition and contact metal evaporation. Surface leakage was measured between 1000 μm long mesas that are separated by 100 μm, after a 1 min, 350°C, forming gas anneal. For CdS-treated samples, surface leakage current was two orders of magnitude lower than that of untreated samples. Surface current may be explained by field-assisted movement of electrons through traps or by the accumulation of carriers at the oxide/semi-insulating InP interface. Both treated and untreated *n*-type MIS test structures exhibited a positive flatband voltage shift, corresponding to a negative fixed-oxide charge, which prohibits an accumulation layer of electrons. The lower surface current of the CdS-treated sample is likely the result of lower interface-state density.

After contact metallization, a second SiO_2 layer was deposited (Fig. 5b). The channel regions were exposed by etching openings in the double oxide layer, then recessed with a succinic acid-based etch to remove an InGaAs cap layer and half of the InAlAs barrier layer. Selected samples were then placed in a CdS bath for our standard treatment to passivate the exposed channel region. The second oxide layer protects the ohmic contacts during the channel treatment. After CdS treatment, the gate fingers were aligned to the recess openings and TiAu metal was patterned with a

resist lift-off process (Fig. 5c).

Typical I-V characteristics for TiAu Schottky diodes, with and without CdS channel treatment, are shown in Fig. 7. Samples without channel treatment were subjected to an 11M NH_3 solution for 3.5 min at 75°C in lieu of CdS deposition. The test diodes have 200 μm^2 gate areas defined by optical lithography and fabricated with the same processing sequence as the HEMTs. CdS-treated diodes required some annealing before acceptable I-V characteristics were obtained.

Higher turn-on voltage and lower reverse leakage were routinely observed for the CdS-treated samples after annealing at 150°C. The I-V data of Fig. 7 was taken after a 1 min, 300°C forming gas anneal. Note that reverse leakage of the CdS-treated samples is reduced by well over one order of magnitude. Schottky barrier height was determined by the activation energy method.[19] For a given forward bias voltage, the slope of the $\ln(I_f/T^2)$ vs 1/T plot yields the barrier height, ϕ_{Bn}. For $V_f = 0.5$ V, a barrier height of ~0.6 V was calculated for the CdS-treated channels; the barrier height of the reference sample was ~0.45 V.

Figure 8 compares the common source I-V characteristics of HEMT devices without and with channel treatment. Both samples were treated with CdS before the first oxide deposition and did not display excessive mesa leakage. Figure 8a shows the drain families for untreated and treated channels; Fig. 8b

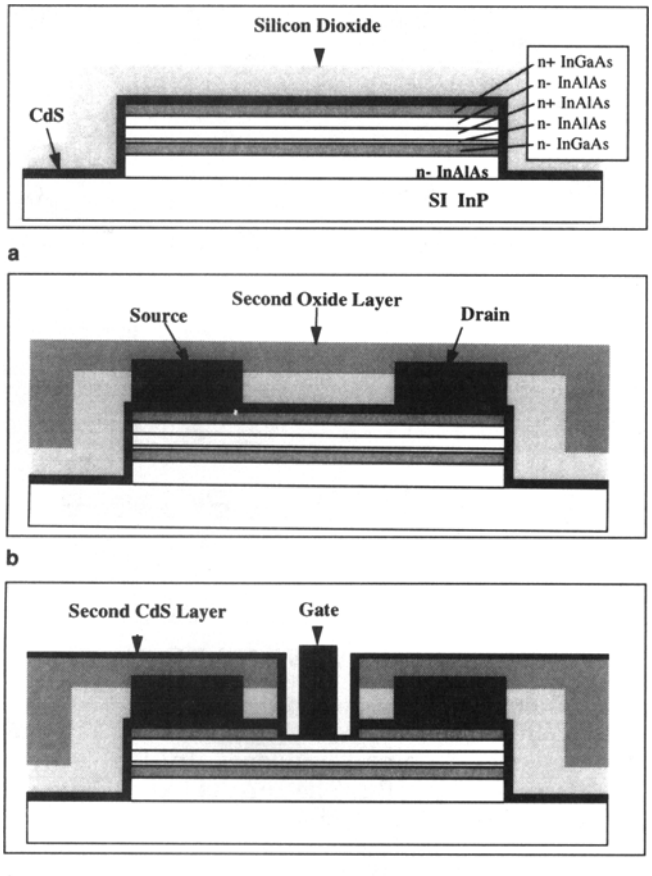

Fig. 5. InGaAs/InAlAs HEMT process with CdS passivation (a) after first oxide deposition, (b) after ohmic contact definition and second oxide deposition, and (c) after second CdS treatment and gate liftoff.

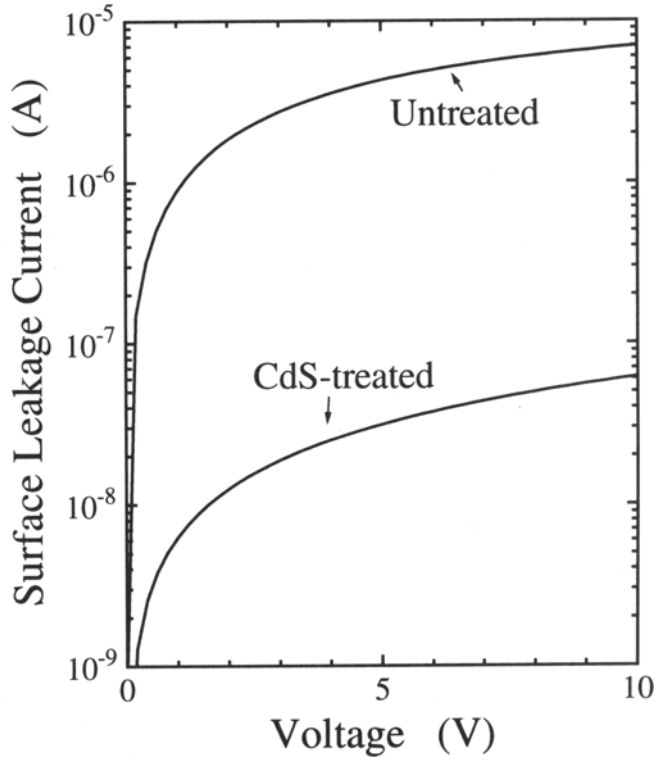

Fig. 6. Leakage current between HEMT mesa layers with and without CdS passivation.

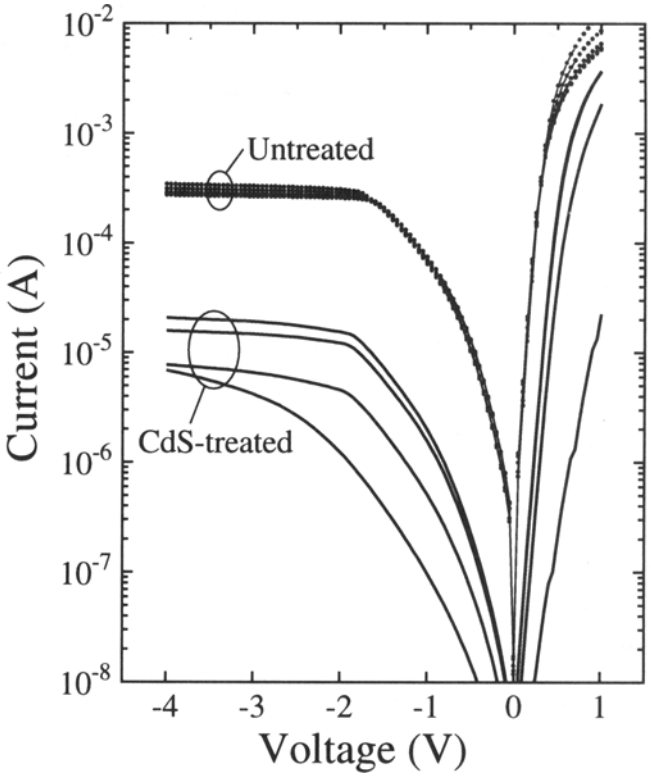

Fig. 7. TiAu Schottky diode I-V curves for untreated and CdS-treated HEMT channels.

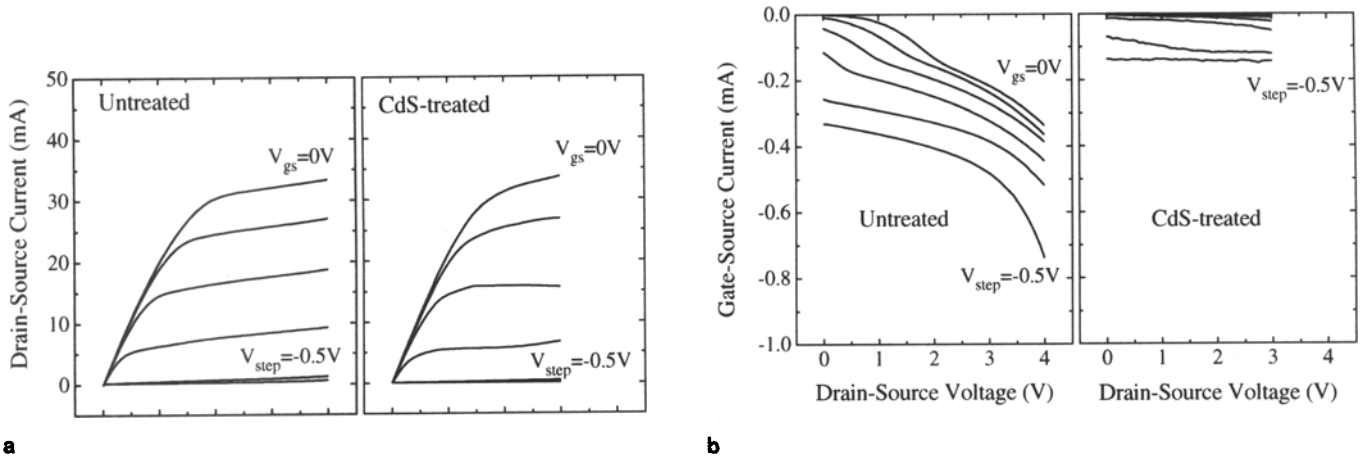

Fig. 8. Results of untreated and CdS-treated HEMTs: (a) drain current,and (b) gate current.

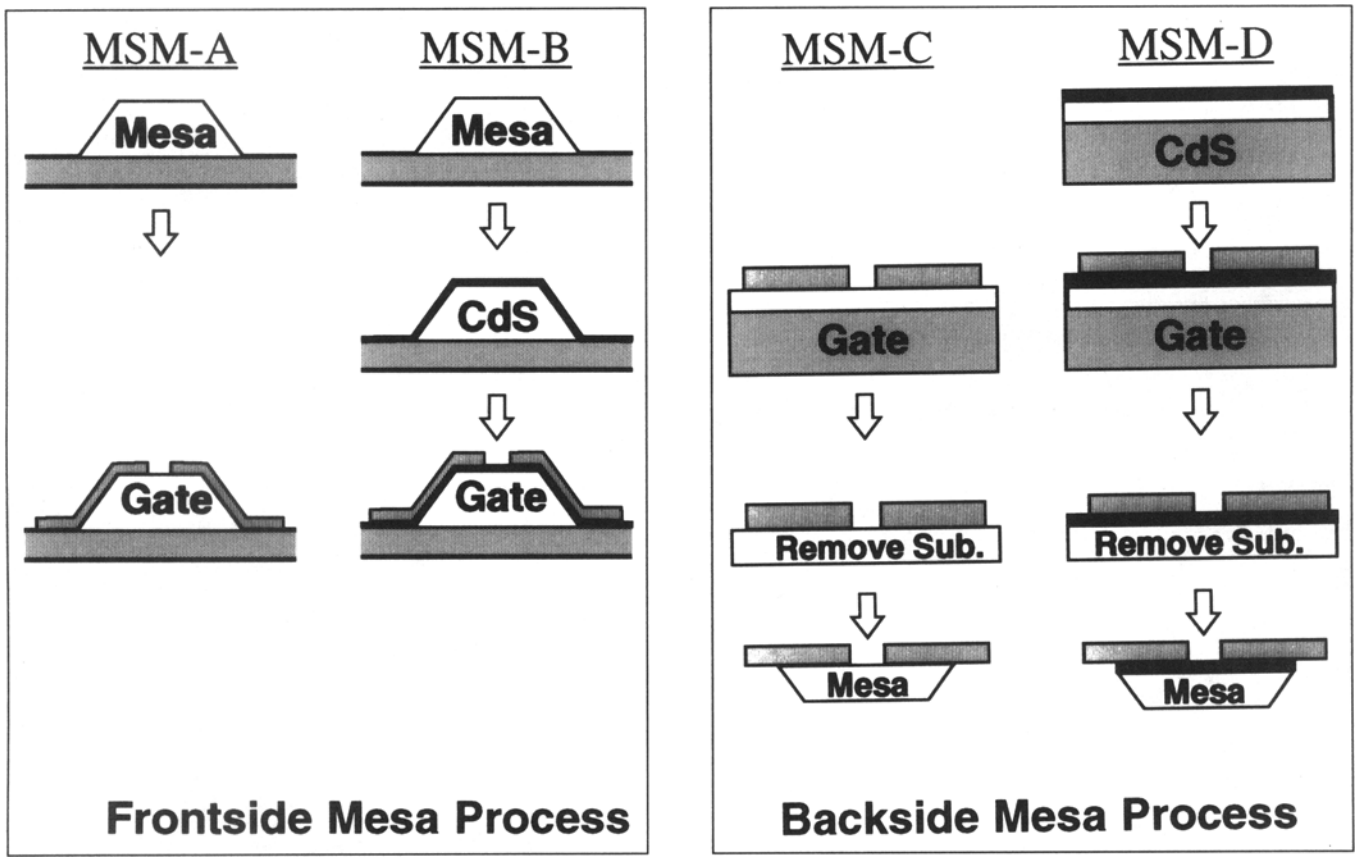

Fig. 9. MSM fabrication processes with substrate removal and CdS treatments.

shows the corresponding gate currents. The gates are 100 μm wide by 1 μm long and the source-gate spacing is 3.5 μm. The characteristics were measured after a 1 min, 225°C forming gas anneal. HEMTs with channel passivation show reduced gate leakage and good pinch-off characteristics, without degradation in transconductance. Maximum transconductance for the treated and untreated samples was approximately 200 mS/mm. For the CdS-treated device, with V_{ds} = 3V and V_{gs} = 0, the drain-to-gate current ratio (I_{ds}/I_{gs}) is 8.2×10^4.

MSM FABRICATION AND RESULTS

MSM detectors were fabricated with the four processes illustrated in Fig. 9. The detector starting material was nominally undoped InAlAs/InGaAs/InAlAs grown by MBE. The InAlAs barrier layer is 500Å, the InGaAs absorbing layer is 1 μm, and the InAlAs buffer layer is 2000Å. MSM-A is our standard process: mesa definition followed by the positioning of TiAu fingers with a resist lift-off process. MSM-B is similar to MSM-A, but treated with CdS after the mesa step, but before metallization. For MSM-C, the

fingers are placed first, the sample is secured to a glass substrate with epoxy, the substrate is removed to expose the epitaxial layers, and the mesas are aligned from the backside of the sample. MSM-D is processed as MSM-C but the surface is CdS treated before the fingers are placed. Mesas are 50 μm × 50 μm. Finger width to spacing ratios (w/s) are 1/1, 2/1, 1/2, and 2/2; the smallest length is 1 μm. Typical responsivities were 0.5 A/W.

Reverse leakage currents for the MSM samples are shown in Fig. 10. The CdS treated samples, MSM-B and MSM-D, demonstrate greatly reduced dark currents. The backside mesa processed samples, MSM-C and MSM-D, avoid contacting the low bandgap InGaAs absorbing layer at the mesa sides with the finger metal. The combination of CdS treatment and backside mesa (MSM-D) produced the most promising results. The dark current of MSM-D is more than three orders of magnitude lower than that of the standard process. The reverse leakage of MSM-D was reduced further by treating the exposed mesa in the CdS chemical bath, thereby completely enclosing the mesa in CdS. Leakage current dropped below 1 nA for 50 μm × 50 μm mesas, as shown in Fig. 10.

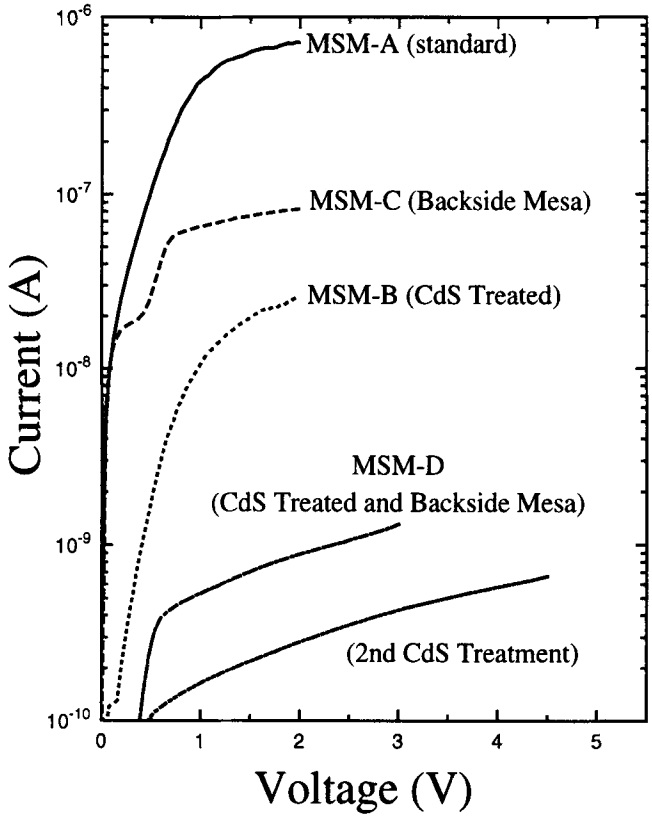

Fig. 10. Dark current measurements of MSM structures illustrated in Fig. 9.

CONCLUSIONS

We have deposited thin layers of CdS on a variety of III-V semiconductors. We found that native oxides were greatly reduced by the CdS treatment. MIS capacitors fabricated on *n*-type InP substrates with CdS interlayers display near-ideal quasi-static response and interface-state densities in the low 10^{11}/eVcm^2 range. Thin CdS layers were effective in eliminating the deleterious effects of the SiO_2 deposition process on mesa isolation. CdS-treated and untreated HEMTs and MSMs were compared. Thin, 50Å CdS layers were effective in reducing Schottky gate and surface leakage. Backside processing of InGaAs/InAlAs MSMs allows complete coverage of the InAlAs/InGaAs mesas, resulting in detectors with less than 1 nA of dark current. The CBD process for depositing CdS is inherently adaptable to a wide range of optoelectronic device processes.

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