MBE Growth and Device Processing of MWIR HgCdTe on Large Area Si Substrates

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The traditional substrate of choice for HgCdTe material growth has been lattice matched bulk CdZnTe material. However, as larger array sizes are required for future devices, it is evident that current size limitations of bulk substrates will become an issue and therefore large area Si substrates will become a requirement for HgCdTe growth in order to maintain the cost-efficiency of future systems. As a result, traditional substrate mounting methods that use chemical compounds to adhere the substrate to the substrate holder may pose significant technical challenges to the growth and fabrication of HgCdTe on large area Si substrates. For these reasons, non-contact (indium-free) substrate mounting was used to grow mid-wave infrared (MWIR) HgCdTe material on 3″ CdTe/Si substrates. In order to maintain a constant epilayer temperature during HgCdTe nucleation, reflection high-energy electron diffraction (RHEED) was implemented to develop a substrate temperature ramping profile for HgCdTe nucleation. The layers were characterized ex-situ using Fourier transform infrared (FTIR) and etch pit density measurements to determine structural characteristics. Dislocation densities typically measured in the 9×10^6 cm^{-2} to 1×10^7 cm^{-2} range and showed a strong correlation between ramping profile and Cd composition, indicating the uniqueness of the ramping profiles. Hall and photoconductive decay measurements were used to characterize the electrical properties of the layers. Additionally, both single element and 32×32 photovoltaic devices were fabricated from these layers. A RA value of 1.8×10^6 Ω-cm^2 measured at –40 mV was obtained for MWIR material, which is comparable to HgCdTe grown on bulk CdZnTe substrates.

Key words: HgCdTe, Si, molecular beam epitaxy (MBE), MWIR, alternative substrate, infrared detectors, reflection high-energy electron diffraction (RHEED)

INTRODUCTION

Through the continued advancement of HgCdTe/Si material growth and device fabrication processes, the fabrication of large focal plane arrays (FPA) (512 × 512 and 1024 × 1024) on Si substrates has been demonstrated in recent years.[1,2] In order to continue the progress toward the everyday production of these and larger size FPAs necessary for higher image resolution and system performance, growth on larger area substrates will be a requirement so that cost effectiveness can be maintained. For example, a 1024×1024 array with a pitch of 18 μm requires only a 2×2 cm area substrate, but six such chips can be grown and fabricated at one time if a 3″ diameter substrate is utilized instead. Additionally, as the technology requirements advance toward the development of even larger array sizes, such as

(Received November 25, 2000; accepted December 19, 2000)

2048 × 2048, it is clear that only large area substrates (3″ diameter or greater) will be suitable for HgCdTe growth.

However, the mounting of larger area substrates can pose significant technical challenges during molecular beam epitaxy (MBE) growth of HgCdTe that are not present when small area substrates are utilized. Currently, the standard mounting technique is to use colloidal graphite or some other chemical compound to adhere the substrate to the substrate holder. Once in place the graphite also acts as a good thermal conductor that is able to efficiently transfer heat from the substrate heater to the substrate surface. However, when mounting large area substrates, it is much more difficult to apply the colloidal graphite uniformly. Therefore, the possibility of having areas on the substrate that are not in good thermal contact with the substrate holder is greatly enhanced. This would cause non-uniformities in substrate temperature across the wafer guaranteeing that some regions of HgCdTe growth would occur under poor growth conditions leading to sections of highly defected material. These types of temperature non-uniformity issues have already been reported for large area substrates.[3] In addition, the initial substrate temperature has been observed to vary from run-to-run as measured by infrared pyrometry due to the graphite mounting technique[3] making it extremely difficult to maintain HgCdTe layer reproducibility on a daily basis. Besides substrate temperature related issues, graphite mounting is also undesirable from a device fabrication point of view. After the completion of HgCdTe growth, it is necessary to remove any residual graphite from the back of the wafer prior to the processing steps. The chance for material damage during this process exists, which can result in serious device-related issues. Furthermore, the future development of non-equilibrium device structures requires very low-doped material[4,5] and it is unknown at this time what effect possible graphite contamination might have on these types of layers. For all of these reasons, it is necessary to move to non-contact methods of substrate mounting for MBE grown HgCdTe.

In this work, we report the growth of n-type MWIR HgCdTe material on 3″ diameter CdTe/Si substrates, mounted on indium-free substrate holders utilizing an empirically derived substrate ramping profile obtained from reflection high energy electron diffraction (RHEED) observations. To demonstrate the feasibility of such a growth method, both single element and 32 × 32 arrays were fabricated from this material.

EXPERIMENTAL DETAILS

HgCdTe growth was carried out in a Riber 32P MBE system equipped with CdTe, Te, and In effusion sources and a valved Hg source. A simple layer structure was grown for these studies, which consisted of an approximate 8 μm thick mid-wave infrared (MWIR) layer followed by the growth of an approximate 1 μm short-wave infrared (SWIR) cap layer. Both layers were n-type doped in-situ with indium. Finally, an ~1000 Å CdTe cap layer was grown.

Three-inch CdTe(211)B/Si substrates, grown in a separate chamber by EPIR Ltd., were used as sub-

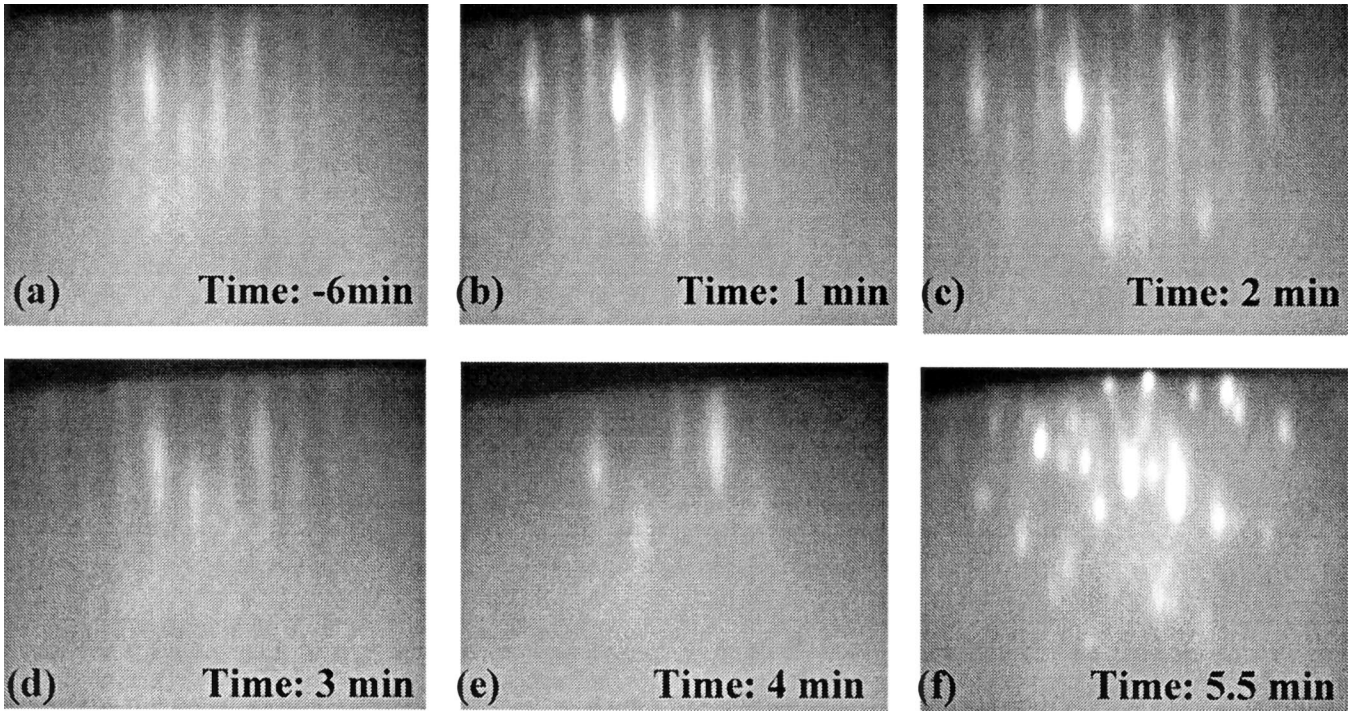

Fig. 1. RHEED images taken from a sample nucleated by maintaining a constant thermocouple set point. The layer goes from low temperature growth (b and c) to high temperature growth (e and f) within approximately five minutes.

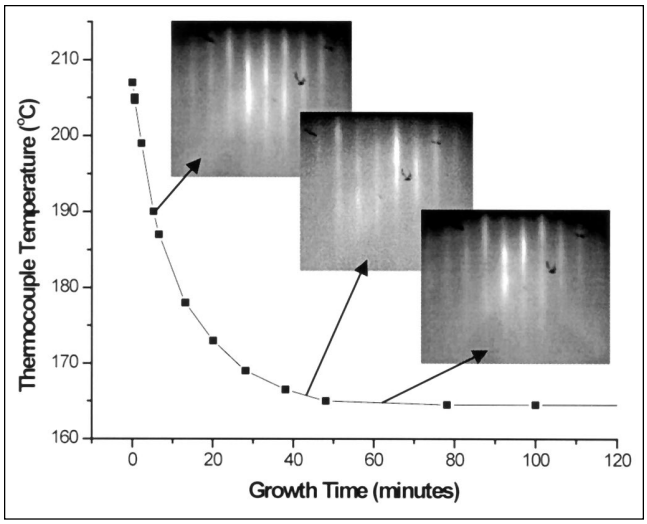

Fig. 2. RHEED images taken during a HgCdTe growth run utilizing the substrate thermocouple ramping profile. RHEED images remained constant throughout the nucleation and growth.

strates for these experiments. The wafers were prepared by first degreasing in two separately heated trichlorolethylene baths followed by rinses in two methanol baths. A five second etch in an approximate 1% bromine/methanol solution to remove the topmost ~500 Å of CdTe was then performed, followed by several methanol and deionized (DI) water rinses. Finally, the substrate was dried with nitrogen and loaded into the MBE system. Once inside the growth chamber, the sample was heated slowly to the CdTe growth temperature where a thin CdTe layer was regrown and annealed to ensure a smooth and clean initial surface prior to HgCdTe nucleation. A 12 keV RHEED system was used to monitor CdTe and HgCdTe growth in-situ. Etch pit density (EPD) measurements were conducted on selected samples to characterize the structural properties of the HgCdTe material. To characterize the electrical properties, Hall measurements were made using the van der Pauw technique for temperatures ranging from 300 K to 50 K on both as-grown and annealed samples using a magnetic field of 0.35 T. Sample annealing for Hall measurements took place at 235°C for 12 hours under a Hg-saturated atmosphere. Finally, layer thickness and x-value determination were calculated from fittings of Fourier transform infrared transmission (FTIR) measurements.

HgCdTe MATERIAL GROWTH AND CHARACTERIZATION

By using indium-free mounting, the substrate is not chemically adhered to a solid, opaque substrate holder, but is, instead, held in place by a "snap-ring" that clamps only the edge of the substrate to the edge of the indium-free substrate holder. Since this is a non-contact mounting method, all of the issues associated with graphite mounting are removed. However, in this mounting configuration, the back of the substrate is now directly exposed to the substrate heating filament instead of remaining in thermal contact with the substrate holder. Hence, maintaining a constant surface temperature during the nucleation of HgCdTe is not a straight-forward proposition. It is known that the emissivity of the epilayer will change as HgCdTe begins to nucleate on the CdTe surface causing a subsequent change in surface temperature. In addition to this effect, the difference in substrate heating mechanisms (radiative as opposed to conductive) due to the non-contact mounting method is also speculated to affect the substrate surface temperature invariant of the substrate thermocouple setting.

Figure 1 shows the RHEED evolution of a layer nucleated by maintaining a constant thermocouple temperature and substrate heater power. As clearly seen in the figure, the RHEED pattern changes significantly during the nucleation of this layer. Figure 1a shows the surface before HgCdTe growth has been initiated. The layer is exposed only to Hg flux at this point and the RHEED pattern indicates a smooth surface. In Fig. 1b and c, one and two minutes of HgCdTe nucleation have occurred, respectively. Large spots are now visible on the streaks and even faint twinning is observed. These RHEED patterns are indicative of low temperature HgCdTe nucleation. However, after 3 minutes of nucleation has occurred, these features disappear and a streaky RHEED image reappears, as shown in Fig. 1d, indicating that HgCdTe growth is occurring within the proper temperature window. Figure 1e was taken after 4 minutes of HgCdTe nucleation and the RHEED image now shows sign of surface deterioration due to high temperature growth conditions. Note that the streaks have become less bright and much shorter in length. Finally, a highly disordered surface with some faceting is seen in Fig. 1f, which was taken after only five and a half minutes of HgCdTe growth. Clearly, within only 5 minutes the HgCdTe surface conditions

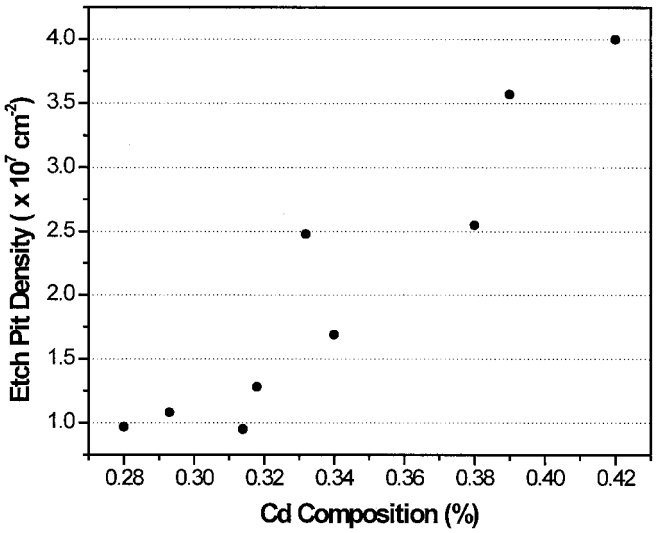

Fig. 3. Plot of etch pit density measurements versus Cd composition for several layers nucleated with the same substrate ramping profile.

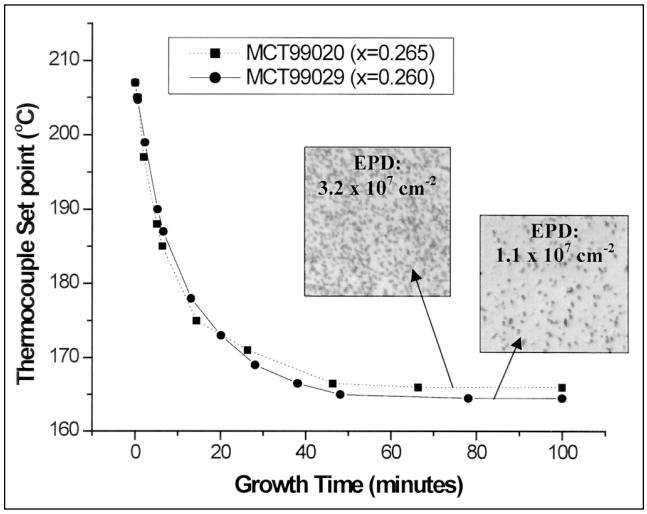

Fig. 4. Different substrate ramping profiles used to nucleate two HgCdTe layers with nearly identical alloy compositions. The insets show the respective surfaces at 800 times magnification after etch pit dislocation revealing etches.

as determined by RHEED dramatically change from a low temperature growth regime to a high temperature growth regime. The magnitude of this temperature change is due to the absence of any conducting layer, such as graphite, between the substrate heater and the substrate and to the fact the thermocouple is no longer in direct contact with the substrate/holder system. Therefore, if non-contact mounting methods are to be used, a mechanism needs to be developed to compensate for this effect.

To meet the needs of growing quality HgCdTe on indium-free mounted CdTe/Si substrates, an empirically derived substrate ramping profile was developed to maintain the proper growth conditions during the initial nucleation stages. A similar method has been successfully implemented in growing SWIR HgCdTe material on indium-free mounted substrates by using spectroscopic ellipsometry to monitor and maintain a constant x-value with respect to growth time.[6] However, both the shape of the ramping profile and the change in initial to final substrate temperatures are expected to differ as the Cd composition is decreased. As seen in Fig. 1, RHEED is a capable tool for monitoring the surface growth conditions and determining whether the growth is occurring in the low temperature, optimized temperature, or high temperature regimes. Through careful observation of the RHEED pattern during the nucleation of several HgCdTe growth runs, we were able to develop a substrate ramping profile that successfully compensated for the increase in surface temperature and produced high quality MWIR material growth. Figure 2 shows such a substrate ramping profile and the resultant RHEED images. As seen in the figure, the RHEED images from this growth run remained constant throughout the entire nucleation and growth process.

However, it is important to note that the proper substrate ramping profile necessary to maintain a constant surface temperature is dependent on the x-value of the layer being grown. Figure 3, which is a plot of EPD values versus Cd composition for layers nucleated with virtually identical ramping profiles and under similar growth conditions, depicts this fact. In these growth runs, the EPD values reach a minimum for HgCdTe that was grown with an x-value ranging from 0.28 to 0.31. Dislocation densities from 9×10^6 cm^{-2} to 1×10^7 cm^{-2} were routinely obtained for HgCdTe nucleated within this range of x-value and with this specific ramping profile. In contrast, as higher x-value material was grown with this same ramping profile, the EPD values of the material increases almost linearly as a function of the deviation from the proper x-value window (0.28–0.31) indicating the degradation of the material quality. Figure 4 depicts the corollary situation in which two

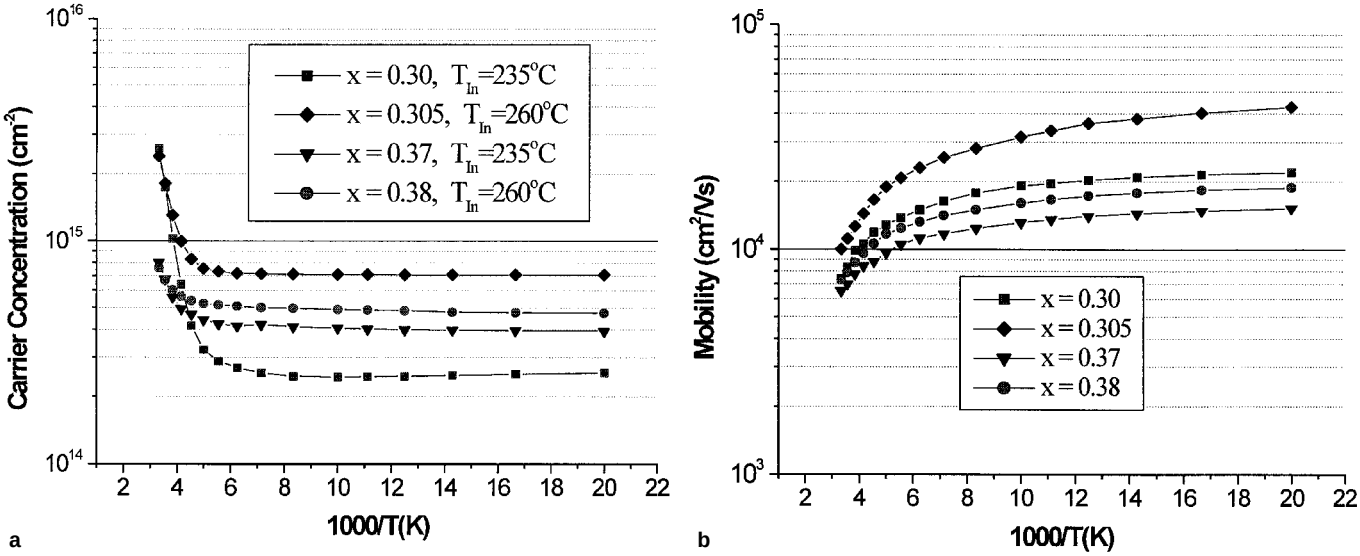

Fig. 5. Plot of (a) carrier concentrations and (b) mobilities versus inverse temperature for several annealed HgCdTe layers nucleated using the appropriate ramping profiles.

different ramping profiles were used to grow layers with nearly identical x-values. Again, as deviations occur from the near optimum ramping profile needed to grow the appropriate x-value layer, the dislocation density is seen to increase dramatically.

Although these results are not unexpected, they highlight the importance of tailoring the substrate ramping profile with the Cd composition of the layer. In general, for each different x-value grown a unique ramping profile will have to be derived. However, in practice one ramping profile should be adequate to grow HgCdTe material within a small range of Cd composition. As the x-value is changed outside this range of Cd composition, another ramping profile will have to be utilized. Furthermore, these results indicate the importance of developing a model to explain and predict the change in the epilayer surface temperature as a function of x-value and growth time when using non-contact substrate mounting.

Hall measurements were conducted to further characterize the material grown using the empirically derived substrate ramping profiles. Carrier concentrations in the 10^{14} cm^{-3} range were obtained for several of the layers grown with mobilities in the low to mid 10^4 $cm^2/Vsec$ range. Figure 5 shows both the carrier concentration and mobility measurements of several annealed layers. As seen in the figure, well behaved Hall characteristics are observed with carrier concentrations increasing as the In cell temperature was increased, as expected, for similar x-value material. Additionally, lifetime measurements were conducted using photoconductive decay on one of the samples grown using the appropriate substrate ramping profile. At 80 K, a lifetime of 2.8 μsec was obtained for an x = 0.37 sample. The electrical characterizations conducted during this study correlate well with the EPD data and confirm that high quality HgCdTe material can be grown by utilizing the substrate ramping profiles to maintain a constant epilayer temperature during the nucleation stages of HgCdTe mounted on indium-free holders.

HgCdTe DEVICE FABRICATION AND RESULTS

To further demonstrate the quality of the HgCdTe material and the applicability of the ramping profiles, both single element and 32 × 32 photovoltaic devices were fabricated from these layers using a planar configuration. Each of the epitaxial structures was processed into photodiodes using conventional photolithographic techniques. Arsenic ion implantation at 350 keV using a dosage of 10^{14} ions/cm^2 and a three-step post implant annealing was used to form the planar p-on-n junction. Sample passivation was conducted using CdTe deposited by MBE. Ohmic contacts were formed by e-beam evaporation on both p-type top layer and n-type absorber layer using Au and In, respectively.

Processed device characteristics were assessed by measuring current-voltage curves and checking the device response to external radiation. The results of the current-voltage measurements for a typical 40 μm × 40 μm single diode are shown in Fig. 6. The cut-off wavelength of this specific diode is 5.8 μm at 77 K. The 300 K background photocurrent at zero bias is measured to be –0.75 pA and the breakdown voltage is in excess of –500 mV. A tunneling mechanism is responsible for breakdown at the larger reverse bias. The RA for this device was calculated using the electrical junction area and was measured to be 1.8×10^6 Ω-cm^2. This peak RA value is obtained, as expected, for a slightly negative voltage of –40 mV. The majority of single element devices measured also show very well behaved I-V curves, with electrical properties comparable to HgCdTe processed on CdZnTe bulk substrates.

The photomask used for single element device fabrication included five different diode sizes: $40\times40\,\mu m^2$, $100\times100\,\mu m^2$, $250\times250\,\mu m^2$, $500\times500\,\mu m^2$, and 1000 × 1000 μm^2. The separation between individual elements is larger than the diffusion length in order to avoid any cross talk effects. An area dependence study of these device characteristics suggests a

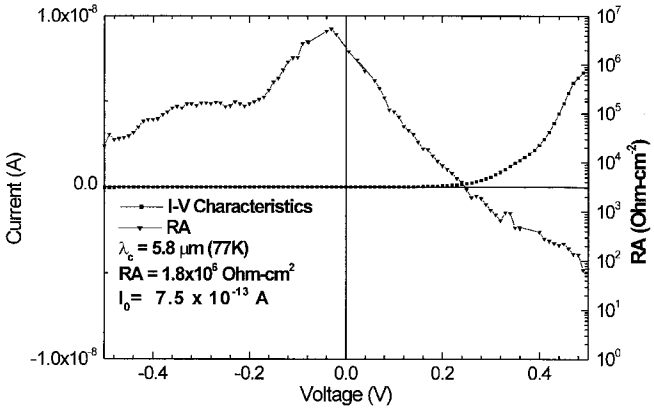

Fig. 6. Current-Voltage plot for an MWIR diode fabricated from a HgCdTe layer grown using the appropriate substrate ramping profile. RA measures 1.8 × 10^6 Ω cm^2 for this diode at –40 mV which is comparable to devices fabricated from HgCdTe grown on bulk CdZnTe substrates.

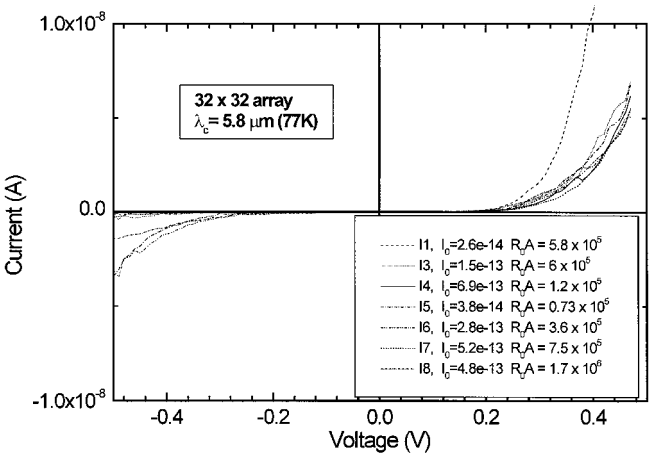

Fig. 7. Current-Voltage plots of several diodes from a 32 × 32 MWIR array showing good uniformity across the array near the operating range of the device.

bulk limited behavior,[7] with smaller area devices showing better electrical properties. The temperature dependence of the R_0A product for these devices was also studied. Low breakdown voltage and zero bias currents are maintained up to 200 K. Diffusion limited behavior has been observed for temperatures larger than 140 K.

32×32 arrays have also been fabricated from HgCdTe layers grown using the substrate ramping profile. The arrays have been designed for use in the backside-illuminated configuration where the array is hybridized onto a silicon readout-integrated circuit (ROIC) by an indium bump interconnect. The pitch size is 53 μm and the separation between individual pixels is 18 μm. Our mask design allowed for the testing of ten diodes from every array. In Fig. 7 we show the I-V characteristics for several individual pixels from the array. The figure shows good uniformity of the array near the operating range of the device. The average 300 K background photocurrent at zero bias for the tested diodes is 0.33 pA with a standard deviation of 0.25 pA. The mean R_0A product is 5.9×10^5 Ω-cm^2 with a standard deviation of 5.4×10^5 Ω-cm^2. The spread in R_0A values indicates the presence of bulk defects. By understanding and modeling the mechanism for the epilayer surface temperature increase during nucleation which will lead to further optimization of the substrate ramping profiles, we expect to substantially reduce material defects induced during HgCdTe growth and improve the overall device quality. The operability of the array is reasonably good with an average of two failed test pixels per array.

CONCLUSIONS

We have demonstrated the growth of MWIR HgCdTe material on 3″ CdTe/Si substrates mounted using non-contact mounting techniques. To compensate for the increase in the surface temperature of the epilayer during growth, we have empirically derived a substrate ramping profile from RHEED observations from several HgCdTe growth runs. This technique has been successfully employed to nucleate and grow device quality HgCdTe. Etch pit density measurements indicate good material quality and also demonstrate that the appropriate ramping profile is a function of HgCdTe alloy composition as well as growth time. Single element and 32×32 array devices have been fabricated with characteristics that are comparable to HgCdTe grown on bulk substrates.

ACKNOWLEDGEMENTS

We wish to acknowledge the support and funding from the Army Research Laboratory for this program under contract number DAAL01-98-2-0079. Additionally, we wish to thank L.A. Almeida at NVESD for his assistance with some of the data acquisition.

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