Metalorganic Chemical Vapor Deposition CdTe Passivation of HgCdTe

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CdTe epilayers are grown by metalorganic chemical vapor deposition (MOCVD) on bulk HgCdTe crystals with x ~ 0.22 grown by the traveling heater method (THM). The THM HgCdTe substrates are (111) oriented and the CdTe is grown on the Te face. The metalorganic sources are DMCd and DETe, and the growth is performed at subatmospheric pressure. Ultraviolet (UV) photon-assisted hydrogen radicals pretreatment plays a dominant role in the electrical properties of the resulting heterostructures. The requirements of a good passivation for HgCdTe photodiodes vis-a-vis the passivation features of CdTe/HgCdTe heterostructures are discussed. The effect of valence band offset and interface charges on the band diagrams of p-isotype CdTe/HgCdTe heterostructures, for typical doping levels of the bulk HgCdTe substrates and the MOCVD grown CdTe, is presented. Electrical properties of the CdTe/HgCdTe passivation are determined by capacitance-voltage and current-voltage characteristics of metal-insulator-semiconductor test devices, where the MOCVD CdTe is the insulator. It is found that the HgCdTe surface is strongly inverted and the interface charge density is of the order of $10^{12}cm^{-2}$ when the CdTe epilayer is grown without the UV pretreatment. With the *in-situ* UV photon-assisted hydrogen radicals pretreatment, the HgCdTe surface is accumulated and the interface charge density is $-4 \cdot 10^{11}$ cm^{-2}.

Key words: CdTe, HgCdTe, infrared detectors, metalorganic chemical vapor deposition (MOCVD), surface passivation

INTRODUCTION

Second generation infrared focal plane arrays based on HgCdTe photodiodes coupled to silicon signal processors, have led to increased interest in CdTe passivation.[1-3] Clearly, CdTe has become the preferred passivation technology for HgCdTe photodiodes, but the published work in the open literature addressing this passivation is rather limited (Refs. 4 and 5 and references therin).

The CdTe layers are deposited by different techniques (liquid phase epitaxy [LPE], molecular beam epitaxy [MBE], metalorganic chemical vapor depositon [MOCVD], hot wall epitaxy, sputtering, e-beam evaporation, and electrodeposition). In addition to the deposition process, there are several major issues that determine the passivation properties of the resulting CdTe/HgCdTe heterostructures. These include the HgCdTe surface preparation and *in-situ* pretreatment, deposition-induced surface damage, interface charges, CdTe film stoichiometry, and electrical properties. Additional issues are related to adherence, step coverage, and thermal stability.[1,4]

The surface and interface pretreatments are a very important part of the MOCVD CdTe deposition technology. In principle, heterostructures that are grown in a single run in the well controlled environment of MOCVD (or MBE) systems should yield high quality interfaces with reduced interface charges. However, in the currently used device designs and architectures,[1] the CdTe passivation is deposited after the required processing steps. The HgCdTe surface is necessarily nonstoichiometric, contaminated (with foreign impurities and oxides) and damaged (in crystallinity). The chemical, structural, and electronic defects induce high density of fixed, fast, and slow

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Table I. Requirements of a Good Passivation and Passivation Featurs of CdTe/HgCdTe Heterostructure

Requirements of a Good Passivation	Passivation Featurs of CdTe/HgCdTe
Interface Properties	
Surface Potential: near flat band	Band diagram depends on: CdTe and HgCdTe doping, valence band offset, interface charges and traps can be engineered to near flat band
Fixed, fast, slow states: low density	Determined by *in-situ* pretreatment
Surface Recombination Velocity: low	Barriers to electrons and holes are formed
Dielectric, Insulating, and Mechano-Chemical Propeties	
Good Insulator	Compensated or fully depleted
Excellent Adhesion	Similar chemistries
Chemical and Mechanical Stability	Lattice Matching (0.3%) Matching in thermal expansion Adequate mechanical hardness
Thermal Stability	Stable up to 150°C
Optically Transparent	Above 0.8 μm
Exhibits Radiation Hardening	High Z materials (48, 52), efficient absorber of high energy radiation
Deposition Technology	
Low Temperature Nondamaging	MOCVD, MBE, LPE, hot wall epitaxy Sputtering, evaporation, electrodeposition.

interface traps. Hence, an *in-situ* pretreatment that forms a reproducible and well-behaved hetero-interface, is a crucial part of the deposition process. Finally, it is important to develop a deposition process that will not introduce a deposition damage at the interface.

In this study, we grow CdTe epilayers (by the MOCVD growth technique) on bulk HgCdTe substrates and characterize the resulting interfaces. Metal-insulator-semiconductor test structures are processed and measured by capacitance-voltage and current-voltage characteristics. The ultraviolet (UV) photon-assisted hydrogen radicals pretreatment is studied and reported.[6,7]

THE REQUIREMENTS OF A GOOD PASSIVATION AND THE CORRESPONDING FEATURES OF CdTe/HgCdTe HETEROSTRUCTURE

The requirements of a good passivation for HgCdTe photodiodes and the passivation features of the CdTe/HgCdTe heterostructure are summarized in Table I. The required interface properties must be achieved without any compromise. These include: a well controlled and close to flat band surface potential and hence a low density of fixed surface charges to reduce tunneling currents (accumulated surfaces impose tunneling at the periphery of the junction and inverted surfaces impose tunneling to the substrate); a low density of fast and slow surface states to reduce low frequency noise currents; a low surface recombination velocity to reduce surface generated dark currents.

The required dielectric, insulation, and mechano-chemical properties are also highly stringent so that the passivation will be fully compatible with device processing, bonding and packaging, prolonged outgassing, storage, and exposure to harsh environments. Finally, a low temperature nondamaging deposition technology is a must in the case of a passivation film for HgCdTe.

The major passivation features of the CdTe/HgCdTe heterostructure that are summarized in Table I indicate why CdTe has recently become the industry-favored passivation technology for HgCdTe photodiodes.[1] The calculated band diagram (and thus the surface potential at the HgCdTe side of the hetero-interface) depends on the valence band offset, doping levels of CdTe and HgCdTe, surface charges and traps at the hetero-interface and deep traps in the CdTe. Precise control of the electrical properties of the CdTe and the interface charges must be achieved to obtain the required interface properties. A low surface recombination velocity is readily achieved because potential barriers for electrons and holes are formed. In particular, the large conduction band offset forms a large barrier for electrons. The band diagram of CdTe/HgCdTe abrupt heterostructure is calculated and further evaluated in the following section.

CdTe is not hygroscopic (like ZnS), it is mechanically harder than HgCdTe, the heterostructure is nearly lattice matched (within 0.3%), the thermal coeffi-

cients of expansion of both materials are nearly the same and the chemistries are similar. Hence, CdTe films are negligibly stressed and adhesion is excellent (between CdTe and HgCdTe, CdTe, and subsequent metallization lines, CdTe and anti-reflection coatings for front-illuminated photodiodes). Chemical, mechanical, and thermal stability (up to 150°C) is reported. The high average atomic number of CdTe (Z_{Cd} = 48, Z_{Te} = 52) renders this material an efficient absorber of high energy radiation and efficient for radiation hardening.

A large number of low temperature deposition technologies are available for epitaxial CdTe (including MOCVD, MBE, LPE, hot wall epitaxy) as well as polycrystalline CdTe films (including e-beam evaporation, sputtering, electrodeposition).[4]

The preferred CdTe technology for passivation should be determined and tailored to the specific device design and architecture. The present study focuses on MOCVD CdTe because it is a dry process with high throughput and energetic species are not incorporated in the deposition process. The MOCVD process yields reproducible hetero-interfaces as well as CdTe epilayers which can be engineered to the exacting requirements discussed above. In addition, excellent step coverages are obtained and the morphology is mirror like. Surface recombination velocity of less than 5000 cm/s, obtained with MOCVD CdTe, is the lowest reported value for p-type long wavelength infrared (LWIR) HgCdTe.[5]

BAND DIAGRAM OF A CdTe/HgCdTe ABRUPT HETEROSTRUCTURE

Two equations govern the interface potentials in the two sides of the hetero-interface. These two equations enable us to calculate the total band bending (relative to the bulk) of each material, and thus the interface potentials of HgCdTe and CdTe (denoted by $\phi_{o,HgCdTe}$, $\phi_{o,CdTe}$, respectively).

The first equation is based on the lineup considerations of the bands of the two materials across the common Fermi level, as shown in Fig. 1.

$$E_{FV_{CdTe}} - E_{FV_{HgCdTe}} - \Delta E_V = q(\phi_{o,HgCdTe} - \phi_{o,CdTe}) \quad (1)$$

where ΔE_V is the valence band offset and $E_{FV_{CdTe}}$, $E_{FV_{HgCdTe}}$ are shown in Fig 1.

The second equation is based on the neutrality condition

$$Q_{CdTe}(\phi_{o,CdTe}) + Q_{HgCdTe}(\phi_{o,HgCdTe}) + q\sigma = 0 \quad (2)$$

where Q_{CdTe} and Q_{HgCdTe} are the total charge per unit area in the CdTe and HgCdTe, respectively and σ is the interface charge density.

These two charges can be expressed by the total band bending in each material (relative to the bulk of each material). Therefore, we have two equations and two variables, $\phi_{o,HgCdTe}$,$\phi_{o,CdTe}$, that can be obtained provided ΔE_V and σ are given. In practice, the valence band offset and the interface charges are not determined with the required accuracy. Measured values of the valence band offset ΔE_V range from 0 to 0.35 eV but there is more or less a consensus around 0.1 eV.[8,9] The interface charge density σ is partly fundamental (due to the difference in chemical bonding and 0.3% lattice mismatch across the hetero-interface) and partly technological (due to mechanical damage, non-stoichiometric surface, surface oxides and adsorbed impurities). It strongly depends on processing, pretreatment and deposition technology. Accordingly, σ can vary by several orders of magnitude.

Following the methodology previously developed for the calculation of a HgTe-CdTe abrupt heterostructure,[10,11] we present the calculated interface potentials of CdTe and HgCdTe, with ΔE_V and σ taken as parameters. This approach enables us to calculate the band diagram of the hetero-interface and to consider quantitatively the effects of ΔE_V and σ on the total band bending in each material. The detailed

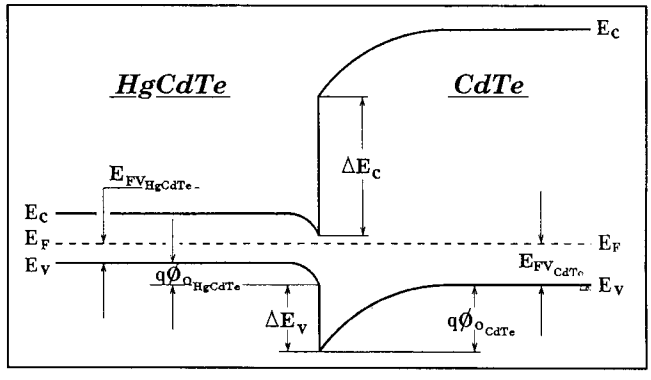

Fig. 1. Schematic energy band diagram of an abrupt CdTe/HgCdTe heterostructure.

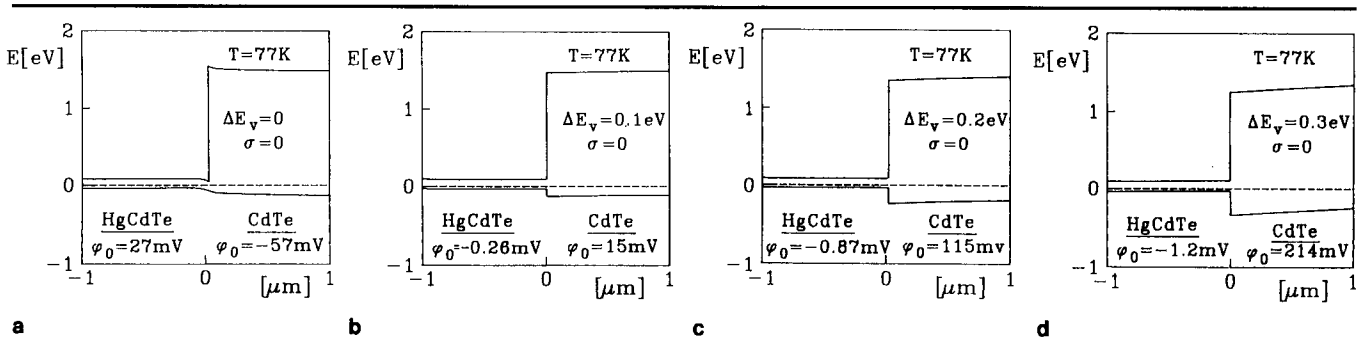

Fig. 2. Calculated band diagrams and surface potentials, (ϕ_o) at 77K, of p-CdTe (N_a = 10^{13} cm^{-3} and E_a = 0.15 eV/p-HgCdTe (x = 0.225 and N_a = 10^{16} cm^{-3}) heterostructures with the valence band offset as a parameter (a) ΔE_V = 0; (b) ΔE_V = 0.1 eV; (c) ΔE_V = 0.2 eV; (d) ΔE_V = 0.3 V. The interface charge density σ is taken as zero.

calculation of the band diagram of an abrupt CdTe-HgCdTe heterojunction are reported elsewhere.[12]

The calculated band diagram and the surface potentials of HgCdTe and CdTe, at 77K, with the valence band offset as a parameter, are shown in Fig. 2. The HgCdTe and CdTe doping levels and parameters are indicated in Fig. 2. We assume that the acceptor level of the MOCVD CdTe is 0.15 eV, corresponding to doubly ionized cadmium vacancy. The calculations take into account the freezeout in the CdTe as determined by the energy of the acceptor level. The interface charge density is assumed to be zero. In the wide range of the assumed valence band offset values (0–0.3 eV), the HgCdTe surface is practically at flat band. Only at zero offset, the surface is depleted and the band bending is 30 mV. The effect of the valence band offset on the surface potentials of HgCdTe and CdTe is exhibited in Fig. 3.

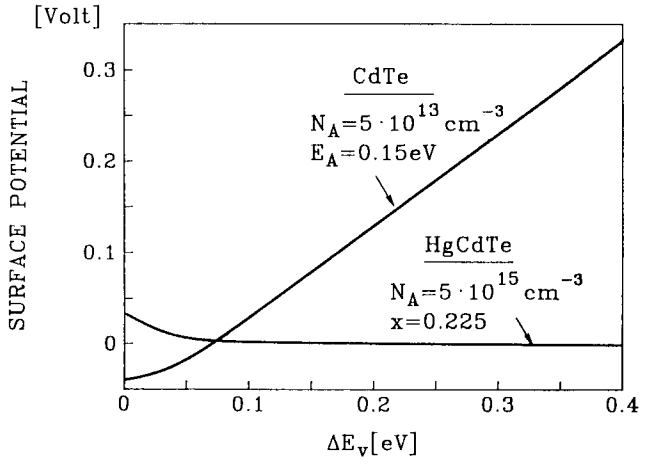

Fig. 3. The dependence of the calculated surface potentials of HgCdTe and CdTe, at 77K, upon the valence band offset. The interface charge density is taken as zero.

The band diagrams and surface potentials of CdTe and HgCdTe are hardly affected by varying the doping levels, as shown in Fig. 4. Depletion or close to flat band conditions are predicted, as long as the interface charge density is zero, even when the doping level of HgCdTe changes by an order of magnitude and the doping level of CdTe changes by two orders of magnitude. The drastic effect of the interface charges upon the band diagrams and surface potentials is shown in Fig. 5 and Fig. 6. Negative interface charges induce accumulation in the HgCdTe side while positive interface charges induce inversion. Figure 6 exhibits that interface charge density of thc order of $5 \cdot 10^{11}$ cm^{-2} causes large deviations from flat band conditions.

The calculated band diagrams and surface potentials of Figs. 2–6 indicate that near flat band conditions can be obtained on p-type HgCdTe, provided that the electrical properties of the hetero-interface and the CdTe are carefully engineered and controlled. The theoretical and experimental uncertainty in the valence band offset introduces a variance in the surface potential of HgCdTe of the order of 30 mV. However, positive interface charges of even moderate density of the order of 10^{11} cm^{-2} induce strong inversion in p-type HgCdTe and strong accumulation in n-type HgCdTe and render the heterostructure use-

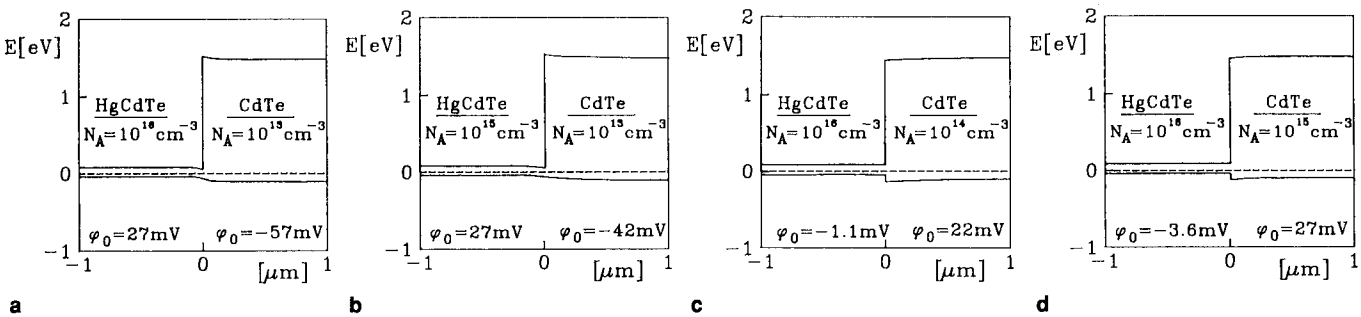

Fig. 4. Calculated band diagrams and surface potentials, (ϕ_0) at 77K, of p-CdTe/p-HgCdTe heterostructures for different doping levels of HgCdTe and acceptor concentrations in CdTe. (x = 0.225; E_A = 0.15 eV)(ΔE_V = 0; σ = 0) (a) HgCdTe: $N_a = 10^{16}$ cm^{-3}, CdTe $N_a = 10^{13}$ cm^{-3}; (b) HgCdTe: $N_a = 10^{15}$ cm^{-3}, all other parameters are the same; (ΔE_V = 0.1 eV; σ = 0) (c) CdTe: $N_a = 10^{14}$ cm^{-3}; (d) CdTe: $N_a = 10^{15}$ cm^{-3} and all other parameters are those of (c). The interface charge density σ is taken as zero and the valence band offset is either zero or 0.1 eV, as indicated.

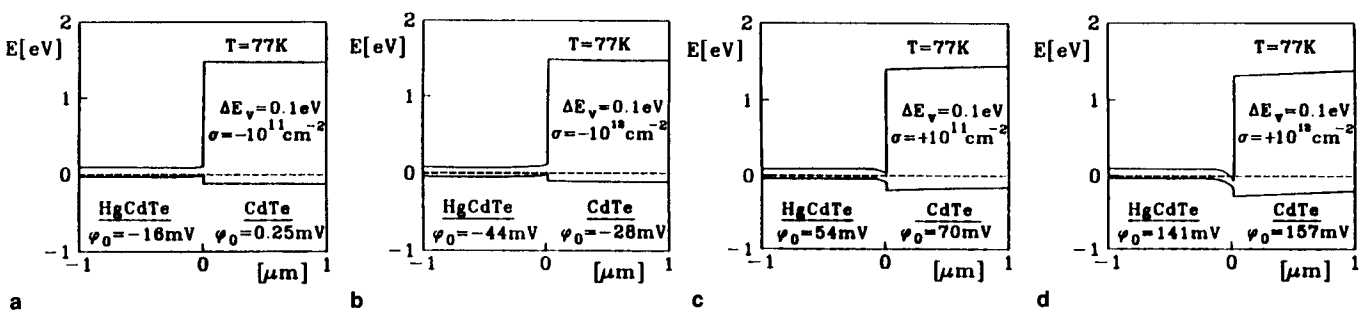

Fig. 5. Calculated band diagrams and surface potentials, at 77K, of p-CdTe ($N_a = 10^{13}$ cm^{-3} and E_a = 0.15 eV)/p-HgCdTe (x = 0.225, $N_A = 10^{16}$ cm^{-3}) heterostructures, for different interface charge densities: (a) $\sigma = -10^{11}$ cm^{-2}; (b) $\sigma = -10^{12}$ cm^{-2}; (c) $\sigma = 10^{11}$ cm^{-2}; (d) $\sigma = 10^{12}$ cm^{-2}. The valence band offset is taken as 0.1 eV.

less for passivation. Similarly, negative interface charges of the order of 10^{11} cm^{-2} induce accumulation in p-type HgCdTe and strong inversion in n-type HgCdTe. Hence, it can be concluded that the valence band offset and the exact values of the doping levels of CdTe and HgCdTe play a minor role in determining the exact values of the surface potentials. For the p-isotype heterostructure discussed here, close to flat band conditions are achieved for a wide range of doping levels and valence band offsets. However, the effect of the interface charge is drastic, and it is the most dominant parameter that controls the surface potentials.

MOCVD GROWTH OF CdTe ON HgCdTe

Substrates

Two types of (111) oriented (±2°), bulk p-type $Hg_{1-x}Cd_xTe$ wafers ($x \cong 0.225$), were used in this study: single crystals grown by modified slush recrystallization and single crystals grown by traveling heated method (THM).[13,14] The electrical characteristics of typical wafers are: $N_a = 10^{16}$ cm^{-3}, $\mu_p \cong 600$ cm^2V^{-1} s^{-1} and $\tau_n \cong$ (5–20) ns, at 77K. The HgCdTe substrates were mechanically polished with 0.3 μm alumina powder and subsequently chemically etched for 30 s with 10% bromine in methanol solution. The CdTe epilayers were grown on the Te face of the $Hg_{1-x}Cd_xTe$ substrates and the face was determined with the Polisar etch.

MOCVD System and CdTe Growth Process

The MOCVD system was manufactured by Thomas Swan Inc., England, and has a horizontal quartz reactor. The graphite susceptor is heated with infrared lamps. The metalorganic sources, DETe and DMCd, supplied by Morton, are kept at 25°C. Palladium diffused hydrogen serves as the carrier gas. Growth runs, at 430°C, are performed at a subatmospheric pressure of 300 Torr and the total flow rate is 1.2 l/min. The partial pressures of DETe and DMCd in the reactor are 1 and 0.26 Torr, respectively.

The HgCdTe wafers are exposed to the following temperature cycle: the susceptor is heated to 430°C within 7 min. The susceptor temperature is stabilized at 430°C for additional 5 min. At 430°C, approximately 0.4 μm CdTe are grown in 3 min (the exact thickness depends on the pretreatment). After growth, the susceptor is cooled to 260°C in 6 min by flowing hydrogen (130 cc/min at 300 Torr) and after additional 15 min the susceptor temperature drops below 50°C. Under these conditions, 3000–5000Å CdTe are grown in 2.5–4 min. With the UV pretreatment described below, ~4000–6000Å are grown in 2.5–4 min. Mirror-like epilayers, with excellent morphology and no hillocks are observed on the Te face of (111) oriented substrates. The effect of the MOCVD growth parameters, including deposition temperature, duration, partial pressures of the metalorganic sources, and Hg and misorientation of HgCdTe substrates, will be reported elsewhere.[15]

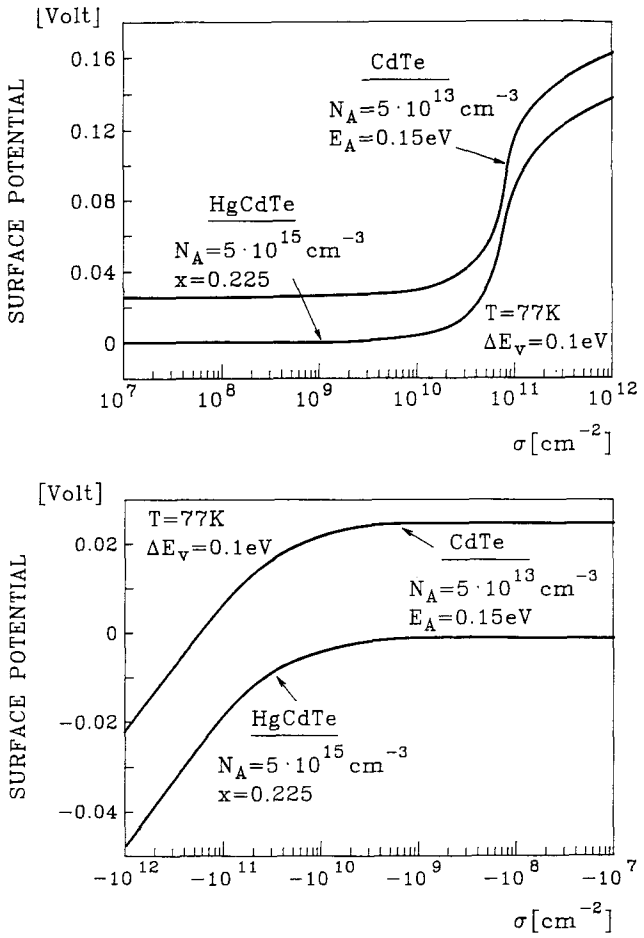

Fig. 6. The dependence of the calculated surface potentials of HgCdTe and CdTe, at 77K, upon the interface charge density: (a) positive charges, and (b) negative charges. The valence band offset is taken as 0.1 eV.

UV Photon Assisted Hydrogen Radicals Pretreatment

Ultraviolet radiation for an *in-situ* pretreatment prior to the growth of the epilayers is provided by a high pressure Hg lamp operating at 450 W, with a wide emission spectrum between 190 and 300 nm. In this pretreatment, the HgCdTe substrate, at 50°C, is irradiated by the UV lamp for 1 h while the reactor and the HgCdTe substrates are flushed in hydrogen, flowing at 250 cc/min, at a tolal pressure of 300 Torr. Prior to the subsequent growth of CdTe, the UV photons are shut off.

ELECTRICAL CHARACTERIZATION

MIS Test Devices

Metal-insulator-semiconductor devices were fabricated on p-type HgCdTe and used to characterize the electrical properties of the interface. The insulator of the MIS device consisted of the MOCVD grown CdTe epilayer, approximately 0.4 μm thick. The combination of evaporated titanium (500Å) and gold (1 μm) was used for bulk and gate metallization. The gate electrodes of ~500 μm diameter were evaporated

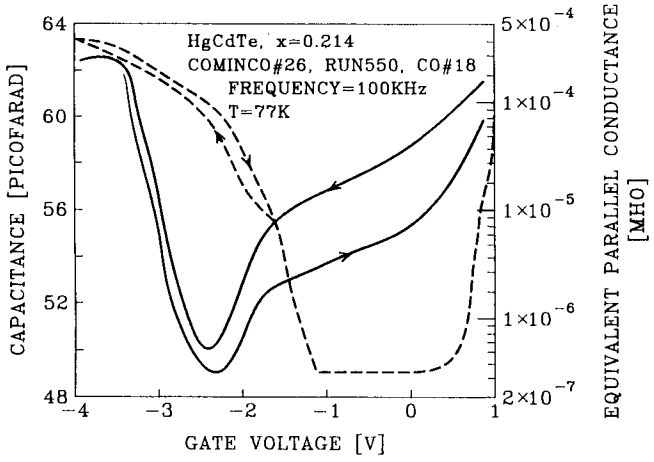

Fig. 7. Measured capacitance-voltage (solid line) and equivalent parallel conductance (dashed line) characteristics of MIS device that was not exposed to UV pretreatment. The measurement temperature is 77K and the measurement frequency is 100 kHz. Gate area is 0.002 cm².

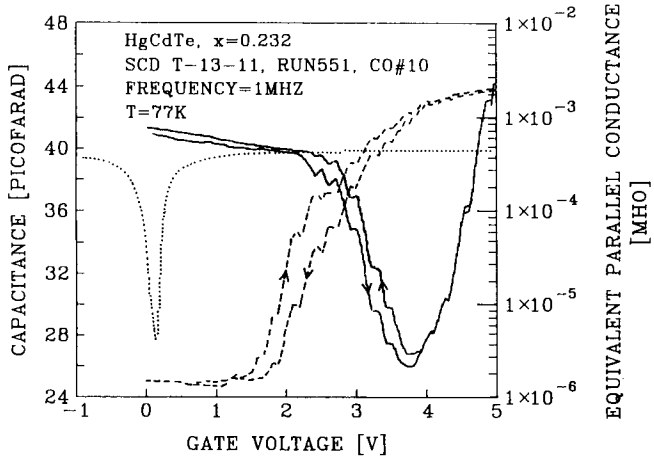

Fig. 8. Measured capacitance-voltage (solid line) and equivalent parallel conductance (dashed line) characteristics of MIS device that was exposed to UV pretreatment. The measurement temperature is 77K and the measurement frequence is 1 MHz. Gate area is 0.002 cm². Dotted line is the theoretical C-V curve.

through a metal mask and the bulk contact was evaporated on the rear side of the HgCdTe substrate. The devices were bonded and sealed with a cold shield at 77K, in a dewar. The devices were subject to annealing cycles in vacuum in the temperature range 70–140°C and were characterized repeatedly at several temperatures.

Capacitance and conductance were measured as a function of gate voltage, with frequency as a parameter, with an HP4192A impedance analyzer. The DC gate current was measured as a function of gate voltage with HP signal parameter analyzer. Simple MIS theory neglecting modifications due to the Kane model was applied for the analysis.

Capacitance-Voltage and Conductance-Voltage Characteristics

The surfaces of the CdTe/HgCdTe heterostructures are determined with measured capacitancevoltage and equivalent parallel conductance-voltage charac-

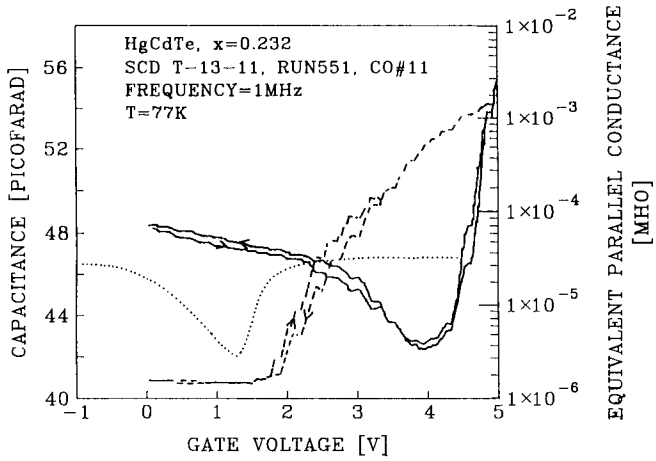

Fig. 9. Measured capacitance-voltage (solid line) and equivalent parallel conductance (dashed line) characteristics of MIS device that was exposed to UV pretreatment. The measurement temperature is 77K and the measurement frequence is 1 MHz. Gate area is 0.002 cm². Dotted line is the theoretical C-V curve.

teristics of MIS devices, as shown in Figs. 7–9.

The drastic effect of the positive interface charges, observed when the MOCVD CdTe is grown without an *in-situ* UV pretreatment, is shown in Fig. 7. At zero gate bias, the HgCdTe surface is inverted. The measured fiat band voltage is –3.3 V and the fixed interface charge density is $Q_{ss} = 6.4 \cdot 10^{11}$ cm^{-2}.

The C-V characteristic is analyzed with the following inputs:

Cinsulator (from Fig. 7) = 62 pF
Cminimum (from Fig. 7) = 49 pF
Gate area (measured) = $2 \cdot 10^{-3}$ cm²
Relative dielectric constant of CdTe = 10.6
Relative dielectric constant of HgCdTe = 18

The following MIS parameters are derived from simple MOS theory:

HgCdTe effective doping concentration = $9.7 \cdot 10^{15}$ cm^{-3}

CdTe thickness = 3000Å
Flat band capacitance = 59 pF
Flat band voltage (from Fig. 7) = –3.3V

Metal-semiconductor (titanium-HgCdTe) work function difference $\Phi_{MS} = 0$V based on: $\Phi_{MS} = \Phi_{MO} - (\Phi_S + E_g/2 + \phi_F)$ where the work functions of titanium and HgCdTe are $\Phi_{MO} = 4.3$ eV and $\Phi_S = 4.23$ eV, respectively.[16] From $V_{FB} = \Phi_{MS} - Q_{SS}/C_{OX}$, we obtain $Q_{SS} = 6.4 \cdot 10^{11}$ electrons/cm².

The interface is very stable with respect to temperature cycles. The devices were repeatedly annealed at temperatures up to 140°C, for 24 h at each cycle. The annealing temperature did not exceed 140°C because of the packaging glues and the experimental dewar and not because of even the slightest interface degradation.

Capacitance-voltage measurements on THM devices often yielded stronger inversion manifested by more negative flat band voltages (of the order of –5 V) and the calculated Q_{SS} is of the order of $1 \cdot 10^{12}$ cm^{-2}.

However, the same general features of the characteristic shown in Fig. 7 and the same high thermal stability were observed. These features include low frequency behavior with little dependence on measurement frequency (in the range of 100 kHz–1 MHz), and low equivalent parallel conductance ($3 \cdot 10^{-7}$mho) around zero gate bias. The equivalent parallel conductance is measured in parallel to the capacitance.

The C-V characteristic of Fig. 7 exhibits correspondence between the calculated and measured characteristics and a small hysteresis at depletion. The apparent hysteresis around zero gate voltage may be attributed to variation in the response time of the minority carriers in inversion. However, C-V characteristics measured on different contacts exhibited a spread in the flat band voltage and hence in the fixed interface charge density, Q_{ss}. This is attributed to small variations in orientations of subgrains in the bulk substrates.[13,14]

The *in-situ* UV photon-assisted hydrogen radicals pretreatment exhibits a significant effect on the heterointerface, as shown in Fig. 8. At zero gate bias, the HgCdTe surface is accumulated. The measured flat band voltage is +3 V and the fixed interface charge density is $Q_{SS} = -3.7 \cdot 10^{11}$ cm^{-2}. At zero gate bias, the equivalent parallel conductance is low and the insulator capacitance exhibits very small hysteresis. At depletion, the conductance increases by three orders of magnitude and 0.2–0.3 V hysteresis is observed, implying slow surface state density of $2.5 \cdot 10^{10}$ cm^{-2}. At strong inversion, the conductance saturates and the hysteresis disappears. The excellent thermal stability is again observed and the C-V and G-V characteristics do not exhibit any shifts even after repeated thermal cycles up to 140°C, where we stopped because of the experimental dewar.

The effective doping level derived from the minimum capacitance is $2 \cdot 10^{14}$ cm^{-3} and this is nearly two orders of magnitude lower than the original doping level of the HgCdTe substrate. Such a reduction in substrate doping level was previously observed during MOCVD growth of CdTe on CdTe substrates, after applying the UV pretreatment.[6] However, not all the MIS devices exhibited this behavior, as shown in Fig. 9. The characteristics of Fig. 9 are similar to those of Fig. 8: the HgCdTe surface is accumulated, the measured flat band voltage is 2.8 V and the fixed interface charge density is $Q_{SS} = -4.1 \cdot 10^{11}$ cm^{-2}. A small hysteresis is observed at depletion where the condutance increases. Again, excellent thermal stability is observed. Analysis of the doping level according to Cminimum yields a value close to the original doping level of the HgCdTe substrate. At this stage, it is not clear if this behavior is also related to different subgrains in the bulk substrates.

In summary, the interface properties of the p-isotype CdTe/HgCdTe heterostructure are very promising. Further optimization of the *in-situ* pretreatment is required to obtain near flat band conditions.

DC Gate Current-Voltage and Differential Resistance Characteristics

The DC gate current-voltage and differential resistance-voltage characteristics of two MIS devices, without and with UV pretreatment, are shown in Fig. 10 and Fig. 11. These curves demonstrate the insulation properties of the MOCVD CdTe at 77K. High values of dynamic resistance are observed at MIS devices grown with the UV pretreatment. The values are two orders of magnitude higher than those observed at MIS devices without UV pretreatment ($10^{11}\Omega$ in Fig. 11 compared to $10^{9}\Omega$ in Fig. 10).

The DC characteristics of Fig. 11 and the AC characteristics of Fig. 8 are measured on the same gate. The DC conductivity increases at positive gate volt-

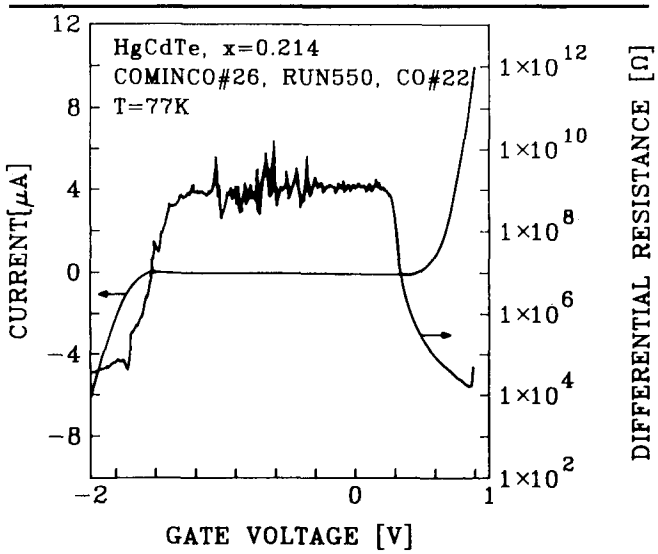

Fig. 10. Measured, at 77K, DC gate current-voltage and differential resistance-voltage characteristics of MIS device that was not exposed to UV pretreatment.

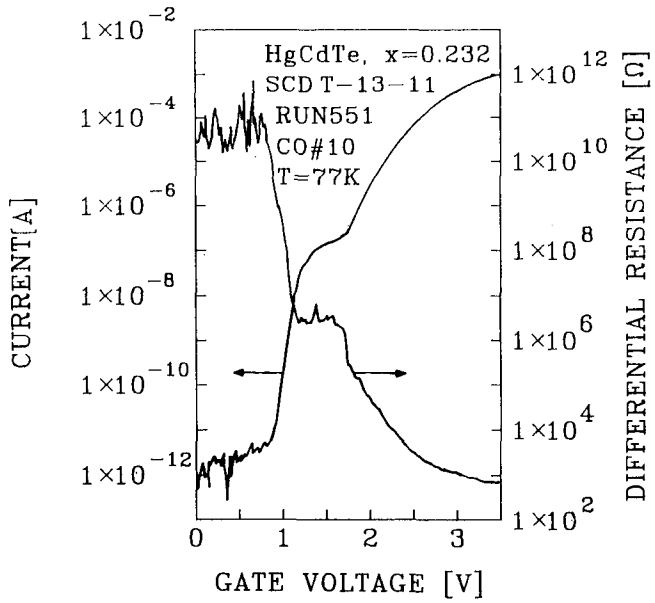

Fig. 11. Measured, at 77K, DC gate current-voltage and differential resistance-voltage characteristics of MIS device that was exposed to UV pretreatment.

ages inducing inversion due to tunneling between the n^+ inversion layer and the substrate (around 0.5 V gate voltage for the untreated device of Fig. 10 and around 3.5 V for the UV pretreated device of Fig. 11). The DC conductivity also increases at strong accumulation (–2V for the device of Fig. 10 and around –1 V for the device of Fig. 11).

The estimated dielectric breakdown field is of the order of 10^5V/cm.

SUMMARY AND CONCLUSION

This paper studies the passivation properties of MOCVD CdTe epilayers grown on the Te face of (111) oriented, bulk HgCdTe wafers. In general, the passivation properties of a specific technology are highly dependent on the orientation, the history, and the origin of the HgCdTe wafers. The present study indicates the potential passivation properties of MOCVD CdTe grown on p-type HgCdTe.

CdTe passivation of HgCdTe in general, and MOCVD CdTe in particular, has been hardly studied in the open literature.[17,18] Bulk HgCdTe wafers are used here since this is a well characterized and reproducible HgCdTe material and it was assumed that a new passivation should be characterized on an established rnaterial. Later on the results can be extended to HgCdTe of different sources and growth techniques. The (111) orientation corresponds to LPE HgCdTe epilayers currently used in production of focal plane arrays.

The study focuses on CdTe passivation that corresponds to the requirements of a wide range of device designs and architectures. Namely, the CdTe passivation is applied during an advanced stage of the processing of the devices and not necessarily as an integral part of the growth of the epilayers. The reported results indicate that MOCVD grown CdTe is a promising passivation technology, provided it is combined with appropriate HgCdTe surface and interface pretreatments. Otherwise, interface charges dominate the surface potential, imposing strong inversion on p-type substrates. With the reported UV photon-assisted hydrogen radicals pretreatment, accumulated interfaces are obtained on the p-type substrates.

It is believed that UV-induced heterogeneous dissociation of hydrogen, on the surface of the HgCdTe substrates, produces highly reactive hydrogen radicals.[6,7] The hydrogen radicals form volatile hydrides with Te atoms. In addition, the hydrogen radicals reduce native oxides that are formed on the surface and remove water molecules that are easily adsorbed on TeO_2 and on the polar surface of (111) HgCdTe. Possibly, additional volatile hydrides are formed of impurity atoms that reside on the HgCdTe surface after exposure to processing. The highly reactive nature of the hydrogen radicals and the photosensitized reaction at the surface, have the potential to form reproducible and controlled hetero-interfaces. The *in-situ* UV photon-assisted pretreatment should be optimized to obtain slightly accumulated or slightly depleted interfaces.

A carefully controlled growth process as well as interface and surface pretreatment tailored to the specific material is required in order to obtain near flat band conditions on p-type as well as on n-type material. The effect of the MOCVD growth parameters (deposition temperature, partial pressures of the metalorganic sources and partial pressure of Hg) in addition to UV photons and pretreatments will be reported elsewhere.[15] Studies of CdTe passivation and 1/f noise as well as CdTe passivation and gate controlled diodes are also essential before this promising technology can be fully assessed. Finally, it should be noted that MOCVD CdZnTe (Zn = 4%) epilayers can provide even superior passivation for $Hg_{1-x}Cd_xTe$ with $x \cong 0.22$, because of perfect lattice matching between the epilayer and substrate and because of the larger bandgap of CdZnTe.

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