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Formation of Silicided, Ultra-Shallow Junctions Using Low Thermal Budget Processing

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The tradeoffs involved in alternative processes for the formation of ultra shallow junctions are described. Low energy implantation, preamorphization to eliminate channeling, and low thermal budget processing are adequate to form junctions that are 0.1 to 0.3 μm deep. For junctions less than about 100 nm, however, the enhanced diffusion resulting from the amorphization implant reduces its benefits. Athermal diffusion can result in considerable junction motion even when low thermal budget processing is used. Junctions this shallow typically require silicide or metal cladding to reduce the sheet resistance; however, the dopant redistribution associated with siliciding pre-existing junctions increases the contact resistance which diminishes the potential benefit of silicidation. In addition, high leakage can result from excessive silicon consumption. While the use of silicide as a diffusion source can overcome some of the limitations of silicided junctions, this technique can be especially hindered by slow dopant diffusion or compound formation in the silicide and by the limited thermal stability of the silicide. One outstanding issue associated with silicide diffusion sources is understanding the seemingly enhanced diffusivity of dopant in the silicon.

Key words: Metal silicides, silicides, shallow junctions, low thermal budget

INTRODUCTION

As device geometries are scaled to smaller dimensions, the fabrication and control of ultra-shallow junctions becomes increasingly more difficult. CMOS and BiCMOS technologies require the formation of both P^+-N and N^+-P junctions with compatible thermal processing. Table I summarizes some of the critical design parameters that are required for several different generations of device technology and shows the need for junctions that are only tens of nanometers deep in the next few years.[1]

For junction depths below about 0.2 μm, three aspects of shallow junction formation become serious issues. First, the use of ion implantation to predeposit dopants is restricted by the higher implant energies associated with commercial machines and by increased dopant channeling, particularly boron, at lower implant energies. Second, the allowable thermal budget, to prevent excessive diffusion, becomes very small and is often not adequate to remove ion-implantation-induced, end-of-range crystal damage; to avoid high leakage, careful engineering must be done to ensure that crystal defects are never within the junction depletion region. The limited thermal budget requirement is satisfied with either very low temperature (<900° C) furnace anneals where dopant solubility and damage removal are low or with rapid thermal processing at elevated temperatures (~1000° C) where uniformity, control, and crystal defect generation are still unanswered issues. Even with low temperature (<900° C) annealing, however, severe enhanced diffusion can occur.[2] Finally, the series and contact resistance of ultra-shallow junctions can severely limit overall device and circuit performance.[3] Although the resistance of scaled devices either decreases or remains constant, depending on whether constant voltage or constant field scaling is employed, the series resistance of junctions increases as the device scaling factor, and the contact resistance increases as the square of the scaling factor as seen in Table II. Table III gives some numerical examples of the scaling of device resistances for technologies ranging from 1 μm[4] down to 0.25 μm.[5] As can be seen in the table, both contact and diffusion resistance are small compared to the resistance of 1 μm devices; however, there is a slight trend, due largely to the desire to maintain higher power supply voltages, towards lower resistance devices at scaled dimensions such that at 0.25 μm dimensions a few squares of diffusion becomes important compared to the raw device resistance, thereby reducing its current drive capability and thus performance.

The use of silicided shallow junctions[6–16] has been shown to lower both the metal to diffusion resistance and the diffusion sheet resistance. Silicide formation also has the potential to reduce the substrate damage associated with ion implantation and junction diffusion.[17–22] Silicide formation prior to ion implantation[23–52] permits the use of higher implant energies, and, under optimized conditions, can be used to eliminate all crystal damage in the silicon. This paper describes the issues associated with the

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Table I. Micron and Submicron Design Parameters

Technology Descriptor	2 μm	1.25–1.5 μm	1.0 μm	0.75 μm	0.5 μm	0.25 μm
Vintage	1980	1984	1987	1990	1993	1996
DRAM capacity	64K	256K	1M	4M	16M	64M
Wafer size	75 mm	100 mm	125 mm	150 mm	200 mm	200 mm
Line/Space Pitch (μm)	4–5	2.5–3	2	1.5–2	1	0.5–0.7
Junction Depth (μm)	0.5	0.3	0.25	0.2	0.15	0.07
Channel Length (μm)	1.8 ± 0.3	1.3 ± 0.3	0.9 ± 0.25	0.7 ± 0.2	0.4 ± 0.1	0.25 ± 0.07
Gate Oxide (nm)	40–50	25	20	15	10	5–7

formation of shallow junctions and how the use of silicide technology, in conjunction with low-thermal-budget processing, might be explored to form junctions that are only tens of nanometers deep.

SHALLOW JUNCTION FORMATION

Preamorphization and Low Energy Implantation

The first step in shallow junction formation, namely the introduction of a shallow layer of dopants can be achieved with low energy ion implantation. The use of molecular BF_2 implants is commonly used to extend conventional ion implanters to shallower p^+ junctions. Since the critical angle for channeling increases as the implant energy is reduced, the impact of channeling must be considered in the design of ultra-shallow junctions. Precise alignment of the wafer[53] can be used to lessen, but not eliminate, channeling. Preamorphization is one widely-examined technique[54–69] to eliminate channeling where species such as Si, Ge, Sn, or In have been used. Silicon and germanium have been the prime candidates for preamorphization due to their complete, isoelectronic solubility in the crystal.

Preamorphization has been shown to occur when the energy deposited via nuclear scattering exceeds a critical value. The depth of the amorphized region can be approximated as the depth at which the concentrations of the preamorphizing species drops to $2.7 \times 10^{19}/cm^3$ for Ge.[66] The amorphization depth has been included in the PREDICT[70] process model. Figure 1 compares experimental and simulated values of the amorphization depth.[60,65–71] While the general trend in experimentally measured values is quite clear, considerable scatter from study to study still exists which, in addition to measurement uncertainly, probably reflects differences in wafer temperature during ion implantation since the amorphization depth is dependent on temperature. The dependence of the amorphization depth on wafer temperature during implantation is especially pronounced for silicon implants. For this reason germanium has been preferred for this work.

Preamorphization is indeed effective in reducing tails in ion-implanted boron profiles as illustrated in Fig 2.[4,71] However, as will be discussed later, the benefit of preamorphization can be offset by enhanced dopant diffusivity during annealing (Fig 2b). Arsenic profiles are not impacted by such preamorphization since arsenic is heavy enough to amorphize the silicon during implantation.

Shadowing during implantation occurs at feature edges whenever ion implantation is done at non-normal incidence to the wafer. Typically wafers are implanted at a nominal 7° tilt. Electrostatic scanning of a 150 mm wafer can contribute another +/−3° to that value. The gate shadowing effect is aggravated in smaller dimension technology where the Poly-Si is anisotropically etched without being fully scaled in thickness. For example a 0.3 μm thick Poly-Si will shadow 26 nm when implanted at 5°. Preamorphization allows the use of normal implantation without having extreme amounts of channeling. A shadowed, underlapped junction leads to asymmetrical device characteristics[72–75] which show reduced current drive capability and increased sus-

Table II. Components of Device Resistance after Scaling

Parameter	Constant E Scaling	Constant V Scaling
Device Current	$1/\alpha$	α
Device Current Density	α	α^3
Device Resistance	1	$1/\alpha$
Contact Resistance	α^2	α^2
Diffusion Resistance	$\sim\alpha$	$\sim\alpha$
Spreading Resistance	~1	~1

Table III. Scaling of Device Resistances

Parameter	1 μm	0.8 μm	0.5 μm	0.25 μm
Device Current (W/L=10/1)	3.8 mA	2.2 mA	1.4 mA	1.6 mA
Voltage	5 V	5 V	3.3 V	2.5 V
Device Resistance (W/L=1/1)	13 KΩ	23 KΩ	24 KΩ	16 KΩ
Contact Resistance*	100 Ω	160 Ω	400 Ω	800 Ω
N^+ Diffusion Resistivity	55 Ω/□	75	135	170
P^+ Diffusion Resistivity	140 Ω/□	100	490	600
$R_c + R_d$ (N^+) w/o silicide	118 Ω			
$R_c + R_d$ (P^+) w/o silicide	367 Ω			
$R_c + R_d$ (N^+) with silicide	59 Ω			
$R_c + R_d$ (P^+) with silicide	170 Ω			

*Assuming $\rho_c = 10^{-6}$ Ω-cm^2.
Data from References 4, 5, 76, 84.

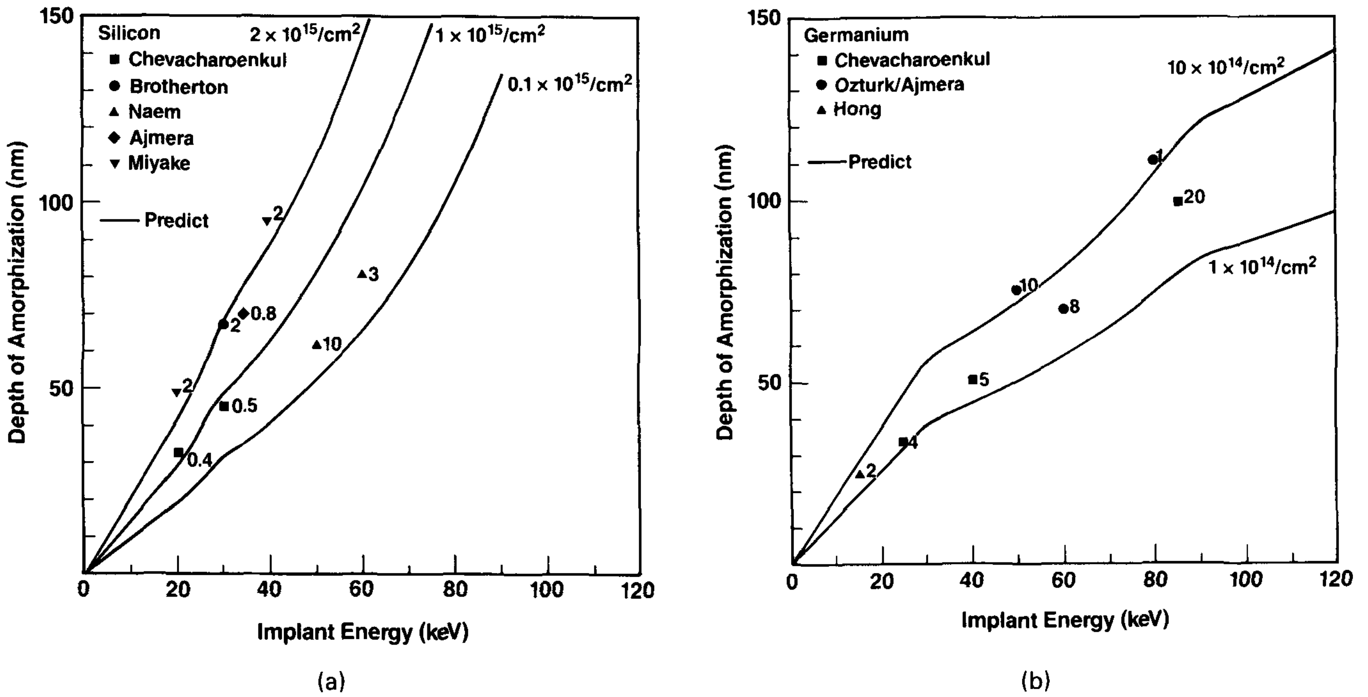


Fig. 1 — Amorphization depth as a function of implant energy and dose for a) Si and b) Ge implants, The lines represent the Predict model,[70] and the points are experimental data.[60,65–71] The number associated with each point represents the dose used in units of $10^{15}/cm^2$ for Si and $10^{14}/cm^2$ for Ge.

ceptibility to hot electron induced instability. Nevertheless, even the implant angle associated with scanning may create a problem, as illustrated in Fig. 3.[76] Furthermore, dual layer gate structures, e.g. polycides, can sometimes undercut during etching to create a shadow for implantation. A more fool-proof technique to eliminate underlap is to rotate wafers during junction implant. Unfortunately, this rotation requires the use of a more sophisticated ion implanter and can impact its throughput.

The process design of the lateral junction edge of a shallow junction is extremely complex. Because of the geometrical shadowing mentioned above, the lateral extent of the amorphization can vary across the wafer and on opposite sides of an individual gate. Unless both the amorphization and the dopant im-

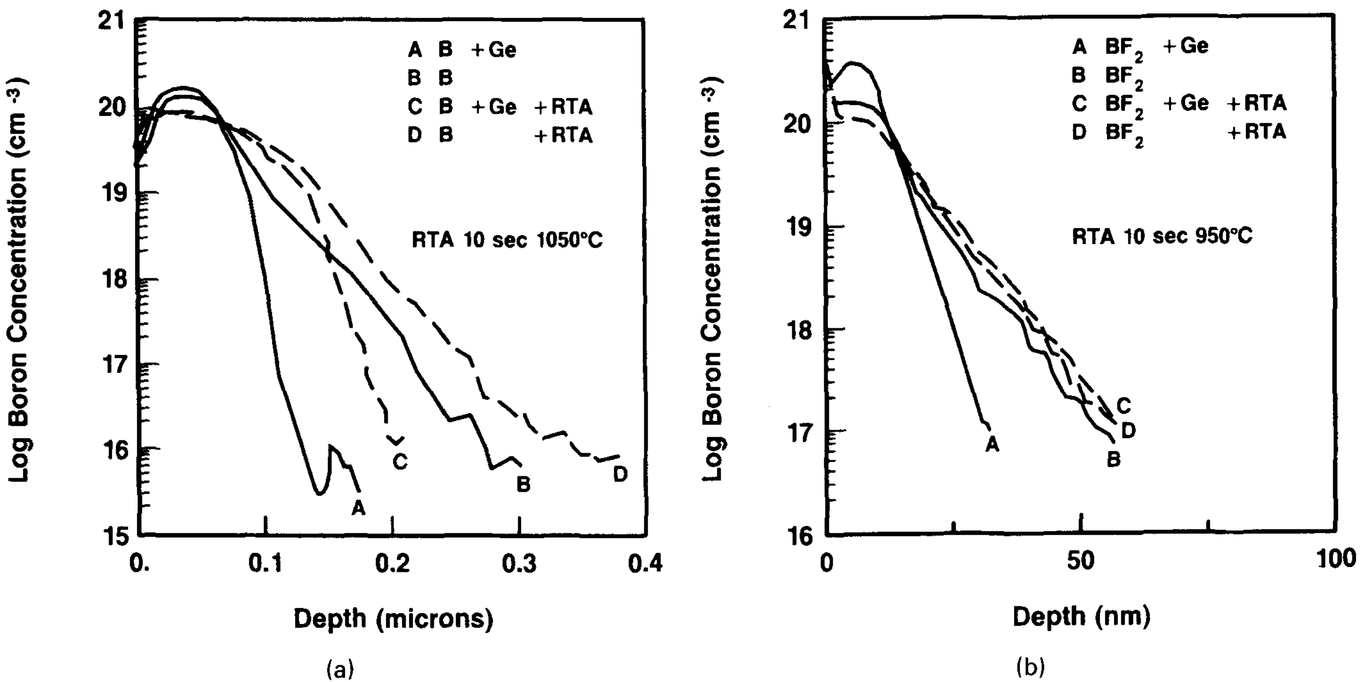


Fig. 2 — Effect of Ge preamorphization on SIMS dopant profiles on a) 10 keV B implants annealed 10 sec at 1050° C[4] and b) 6 keV BF_2 implants annealed at 950° C.[71]

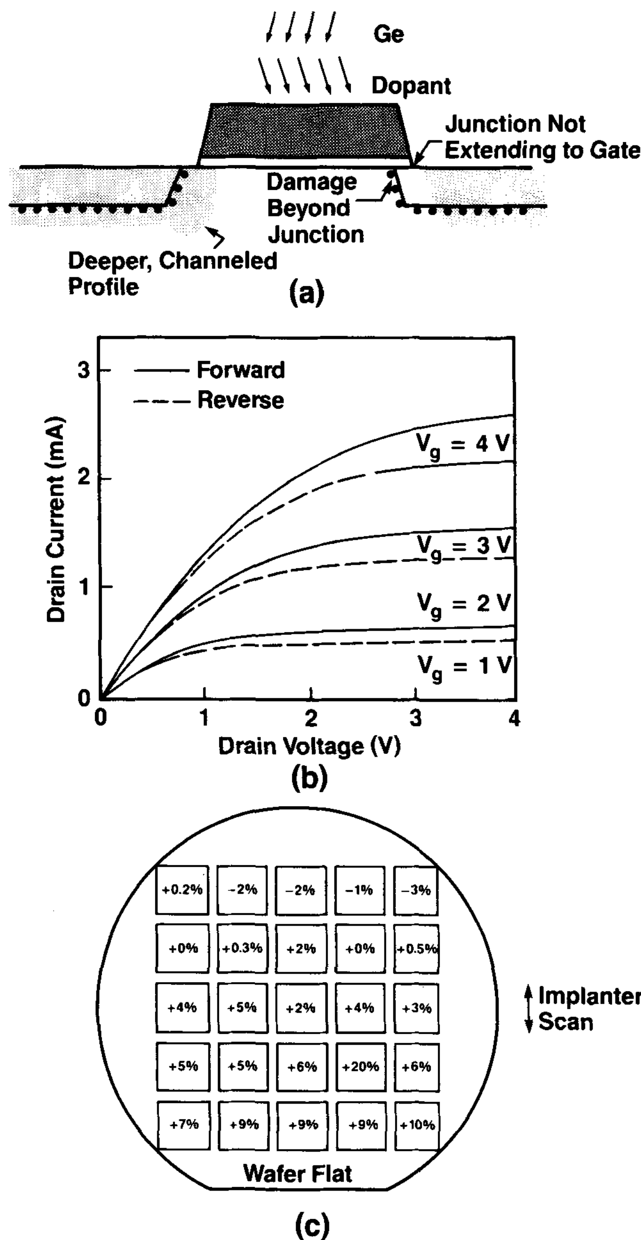


Fig. 3 — Asymmetrical device characteristics due to shadowing of implantation. a) schematic diagram of the origin of asymmetry, b) device characteristics in forward and reverse direction, c) variation of forward/reverse current drive (measured at $V_g = V_d = 3V$) across a wafer due to the systematic variation in implant angle.[76]

plants have the same geometries, lateral channeling of dopant can occur, aggravating the short-channel drop-off in threshold voltage. Nakano[77] found it was necessary to use 30° implant angles plus rotation for amorphization to minimize lateral channeling. On the other hand, angled amorphization implantation, particularly when the Poly-Si gate is tapered, can lead to end-of-range damage beyond the junction depth. Since the Poly-Si gate bias can modulate the lateral location of the junction depletion region and cause it to intersect regions having crystal damage,[78] it is especially critical that the lateral junction edge be considerably beyond the lateral damage. The effects of defects within the junction depletion region will be described in more detail later.

In order to reduce threshold voltage and transconductance shifts caused by hot carrier injection and trapping, current device designs employ one or another variations of a lightly-doped drain design.[79-81] These LDD designs incorporate a lightly-doped region next to the device channel to reduce the drain electric field and thereby to reduce the hot carrier generation and injection. An oxide spacer[81-82] is added to extend the Poly-Si gate dimension to define the conventional, heavily-doped junction. Engineering tradeoffs must be made in the choice of the light doping level, the doping gradient (lateral and vertical), and the length of the spacer to minimize the series resistance of the lightly doped region while producing hot-electron-immune devices. Because of these design tradeoffs, the use of LDD requires even more precise control of the lateral geometries associated with shallow junction formation. In addition to the geometrical shadowing of the implantation discussed previously, the spacer width is strongly dependent on the gate photoresist sidewall angle, the Poly-Si edge slope after etching, conformality of deposition of the spacer oxide (or nitride), and the spacer oxide etching process. When wide spacers are employed, the device short-channel effects are affected only by the depth of the lightly-doped junction region, thereby permitting the use of deeper, higher-conductivity junctions than would be dictated by the simple scaling shown in Table I.

One added benefit of preamorphization is enhanced dopant activation at moderate annealing temperatures. Figure 4 compares the sheet resistances of p^+ and n^+ junctions formed with and without Ge preamorphization.[83-84] Even though the preamorphized p^+ junctions are shallower, they have lower sheet resistances than non-preamorphized junctions especially for low and intermediate temperature annealing cycles. A very large fraction of boron atoms assume substitutional sites during the solid phase epitaxial regrowth, SPE, of the amorphous layer. In contrast, high annealing temperatures are needed to activate the interstitially-implanted boron when no preamorphization is used. Just as with the junction depth, preamorphization has little impact on the sheet resistance of n^+ junctions.

Diffusion with Low Thermal Budget Processing

The process design of shallow junctions requires a careful optimization of both the implant depth and the dopant motion. To maintain shallow junctions, it is essential that subsequent thermal processing be minimized. Rapid thermal processing has been employed extensively in this work even as low as 950° C to restrict dopant motion to only tens of nanometers. On the other hand, some dopant motion is necessary to spatially separate the junction depletion region from the ion-implant damaged region and to provide sufficient lateral diffusion to com-

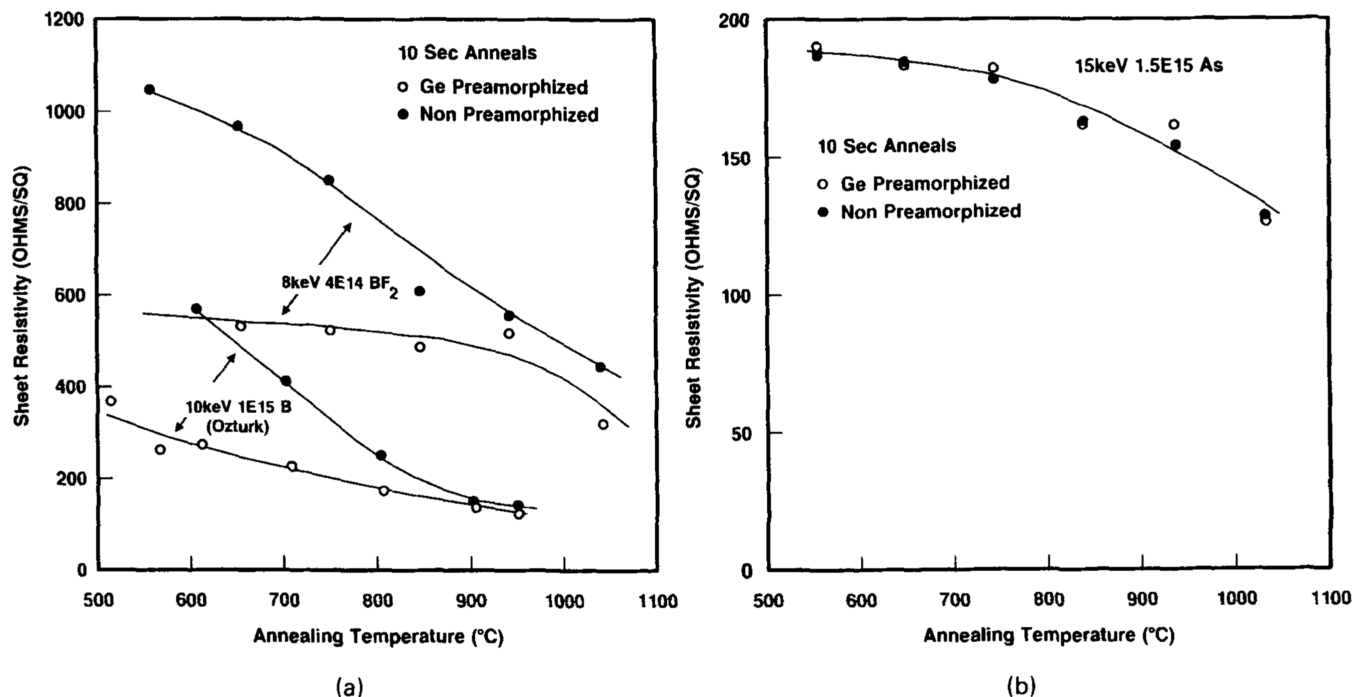


Fig. 4 — Sheet resistance as a function of annealing temperature for different shallow junction implants with and without preamorphization: a) p^+ junctions, b) n^+ junction.[83,84]

pensate for the shadowing that occurs during implantation as discussed earlier. Most typically, however, the processing challenge lies in reducing dopant motion during dopant activation, damage removal, or BPSG glass reflow annealing. The strategy employed in this laboratory is to partition the final, desired junction depth so that both implant depth and diffusion motion were significant contributors.

One of the more serious concerns with restricting dopant motion by reducing the thermal cycle is the tendency for athermal diffusion to occur. Figure 5a presents an example of an 80 nm junction where dopant diffusion is almost independent of the annealing temperature.[84] The temperature dependence for conventional diffusion comes primarily from the energy required to form the point defect species responsible for diffusion. However, when the quantities of point defects created by implantation far exceed the equilibrium concentrations, enhanced, athermal dopant diffusion can occur. Figure 5b shows the junction motion during 10 sec anneals at different temperatures for different boron implant energies.[85] At higher energies, more point defects are created but for decreasing periods of time, and the diffusion appears to be increasingly athermal. However, even with the low energy implants needed for shallow junctions, enough point defects are created to enhance dopant diffusivity. Furthermore, short time annealing is inadequate since the transient excesses in point defects occur over short times, causing considerable junction motion.

The amorphization step has a pronounced effect on subsequent boron diffusion. Figures 2a and 2b contrast the effect of Ge preamorphization-amorphization on 200 and 70 nm junctions.[4,71] In both cases dopant diffusion is enhanced by the amorphization step. This enhancement is attributed to the presence of all the excess point defects created by the amorphizing implant. Despite the enhanced diffusion, preamorphization still results in shallower junctions for the 0.2 μm case. On the other hand, for very shallow junctions, the enhanced diffusion offsets the reduced implant depth so that preamorphization has practically no effect on the final junction depth of the ultra-shallow junctions. Since arsenic is heavy enough to amorphize the substrate anyway, little difference has been observed, at least in the tail region, in arsenic diffusion due to preamorphization.

Damage Removal and Junction Leakage

Junction leakage is determined in large part by the presence or absence of crystal defects within the junction depletion region. The primary objective in shallow junction formation is to eliminate all defects; however, the thermal cycles required to do this are typically excessive to obtain the required junction depth, and many successful processes rely on careful engineering of defects to minimize leakage. Defects can be reduced in size and positioned away from active regions to allow low leakage. Figure 6 shows how even relatively modest annealing (10 sec at 950° C) can be used for scaled junctions to dramatically reduce, but not eliminate, crystal damage.[69] Deeper junctions take correspondingly higher temperatures or longer annealing times to get a similar reduction in defects. Although the mechanism is still somewhat controversial, it has been observed[65,69] that defect elimination, via annealing, is promoted as junction (damage) depths are reduced. The importance of controlling the physical

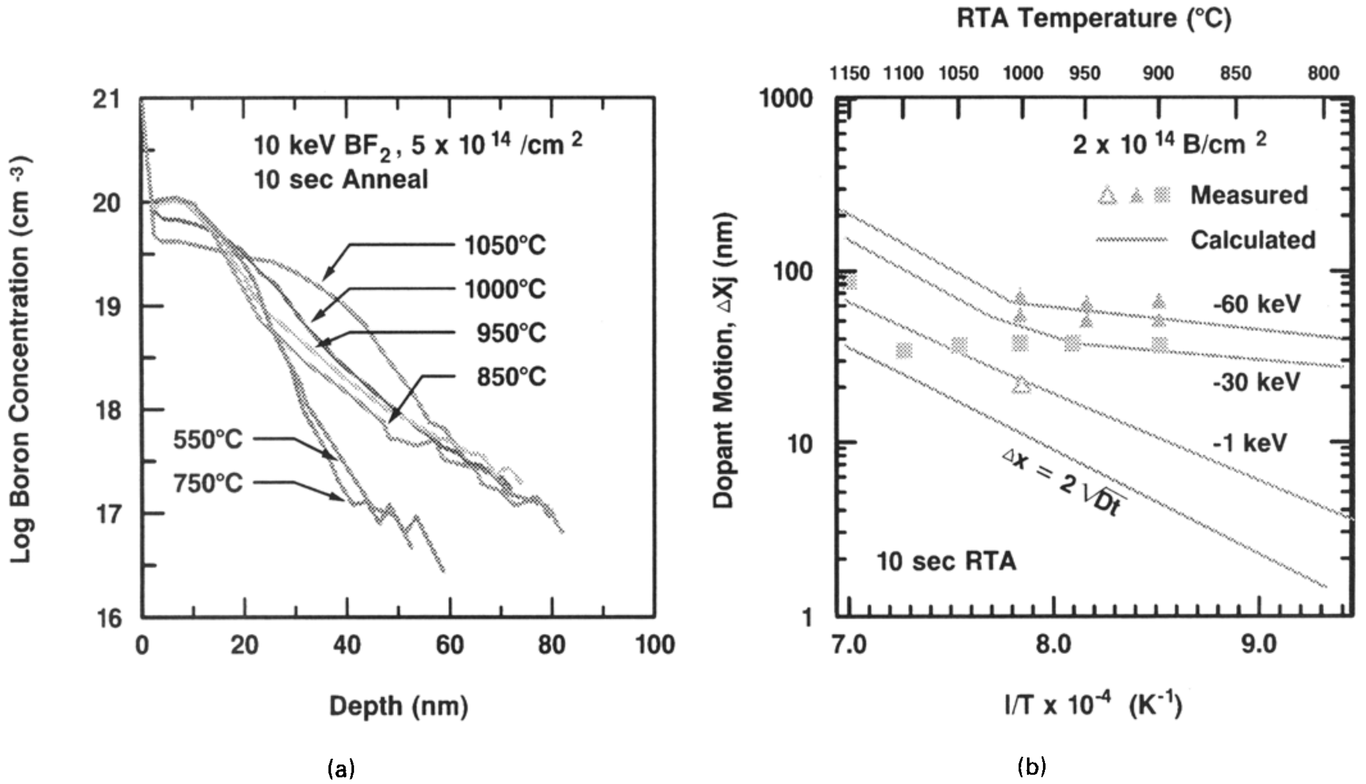


Fig. 5 — Diffusion of boron as a function of RTA temperature for low thermal budget processing. a) SIMS depth profiles of dopant,[84] b) junction motion, ΔX_j, as a function of annealing for different B implantation energies.[85]

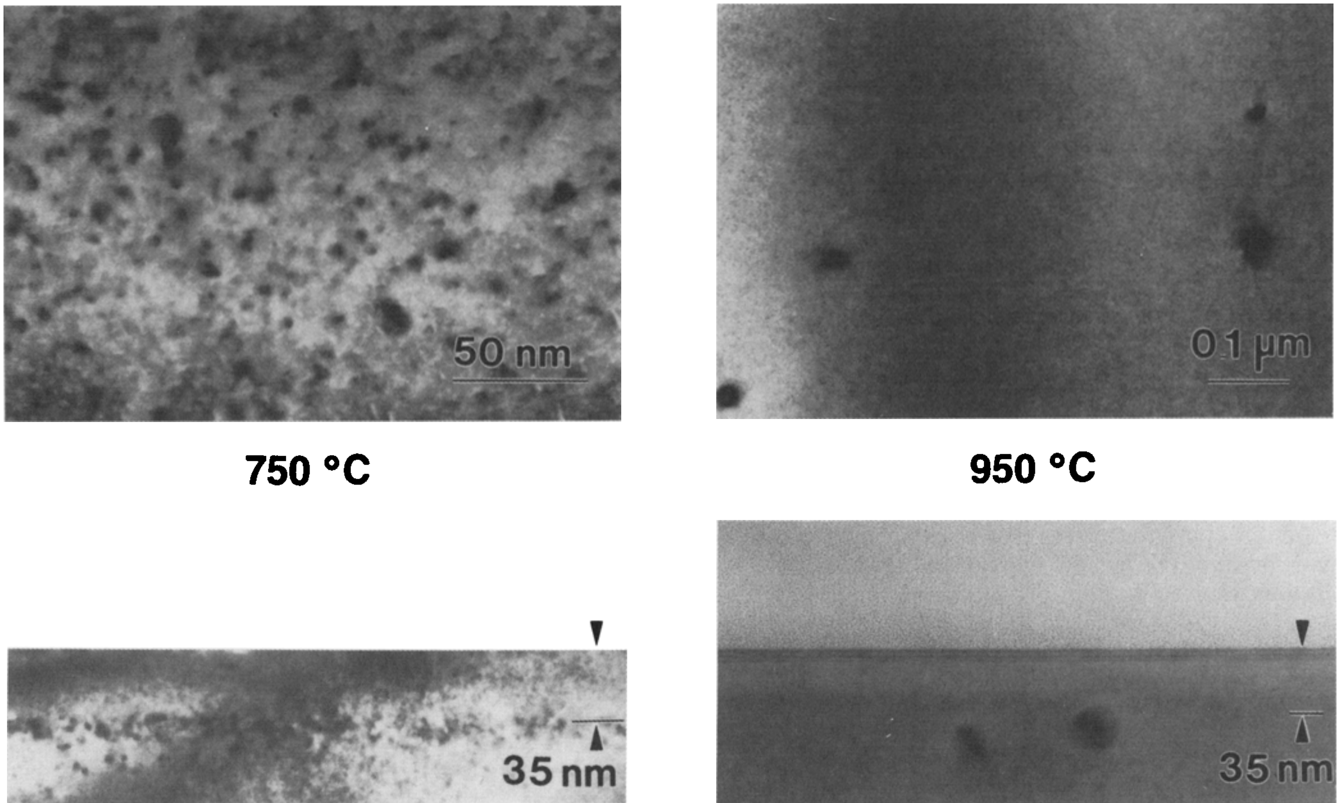


Fig. 6 — XTEM plan and cross sectional views of damage removal after 10 sec 750 or 950° C annealing for ultra-shallow (~70 nm) p^+ junctions.[69] The damage was produced by a 25 keV 4 × 10^{14} Ge/cm^2 implant.

damage is illustrated in Fig. 7.[65,66] In Fig. 7a, n^+ diode leakage is low (~1 na/cm^2) for Ge-preamorphization energies below about 80 keV. At higher energies or doses, the end-of-range damage extends into the junction depletion region and is responsible for high leakage. Once the damage (energy) is shallower than the junction depth, the preamorphization has little impact on leakage. The same kind of behavior is seen in p^+ junctions in Fig. 7b after a typical high temperature anneal. In this case high Si-preamorphization energies result in leaky junctions, while low silicon energies produce good, low leakage diodes. This figure also illustrates another important phenomenon; even though solid-phase recrystallization occurs at low annealing temperatures (~550° C), the diode leakage is high until samples have been annealed at higher temperatures (~800° C). This observation suggests that excess point defects which have not recombined, diffused, or agglomerated can play an important role in enhancing leakage. More sophisticated measurements like photoluminescence[86] show that many of these point defects are still present until quite high annealing temperatures are reached even though normal diode leakage appears good.

While the junction depletion region has a relatively fixed position at the bottom of a junction, the lateral position at a gate edge depends not only on the reverse diode voltage, but also on the gate potential. Thus the depletion region may extend beyond the crystal damage and hence give low leakage at one gate bias; at another gate bias, the depletion region may, in fact, intersect defects and give very high leakage currents. This behavior is illustrated in Figure 8a which compares leakage currents in amorphized and non-amorphized gated-diodes. When the gate voltage is strongly accumulated, high leakage currents result in the amorphized diodes but not in the controls. A detailed analysis[78] has been done to show that this leakage can be quantitatively explained by the presence of mid-gap states within the diode depletion region. Figure 8b illustrates how the gate potential can move the depletion region to cause it to intersect defects. This gate-induced drain leakage has been observed in several studies[87–89] and has proven to be a sensitive indicator of processing defects at gate edges as will be shown later for silicided junctions.

Gate Oxide Degradation During Shallow Junction Formation

Degradation of the gate oxide along the perimeter of the Poly-Si electrode as a result of source/drain implantation is one, little recognized, yield detractor associated with ultra shallow junction formation in scaled devices.[90–94] Figure 9 shows the gate-to-substrate leakage of transistor devices having 7.5 nm gate oxides after receiving different arsenic doses.[94] Unimplanted samples exhibit classical Fowler-Nordheim tunneling (3.1 eV barrier) through the oxide with the current being proportional to the gate area.[95] The conduction in implanted samples is enhanced by many orders of magnitude and is proportional to the gate perimeter. The degradation is also observed as a lowered oxide dielectric breakdown strength and is greatest for thinner oxides and higher implant dosages. The effect has been shown to be related to the physical ion bombardment along the gate edge. Figure 10 compares the degradation observed along the four different edges showing the greatest degradation

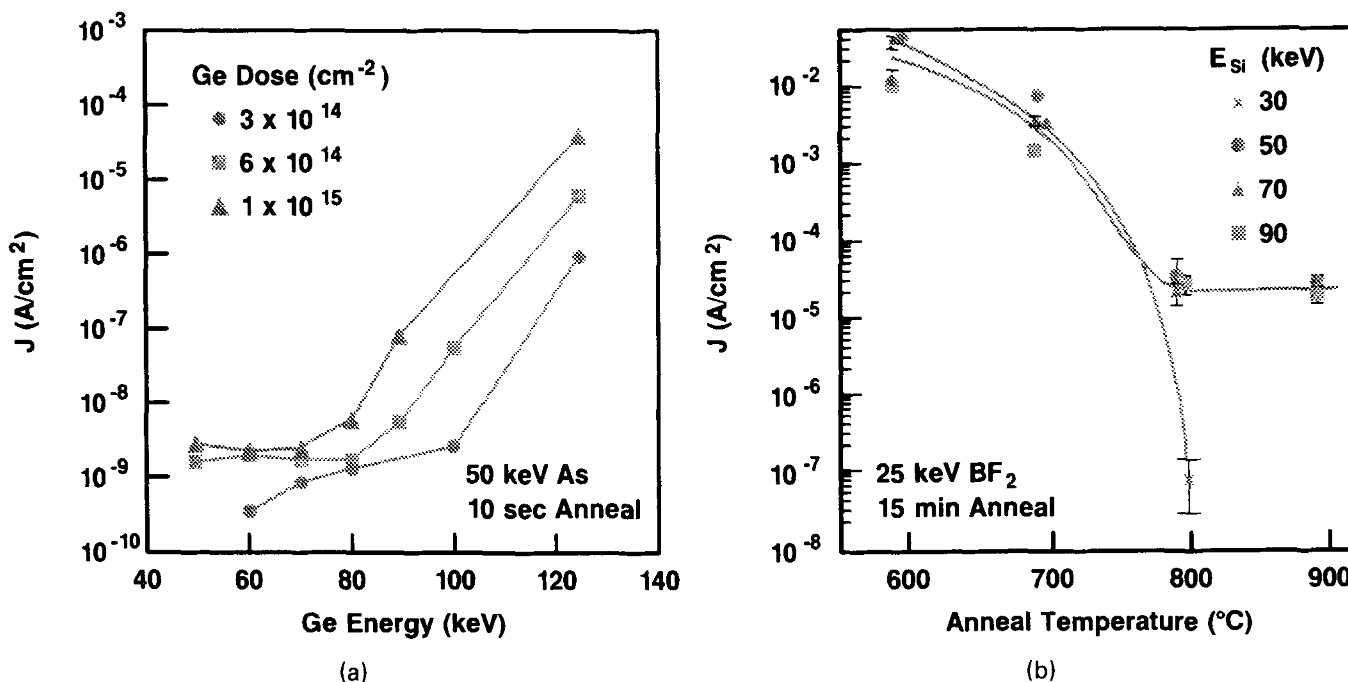
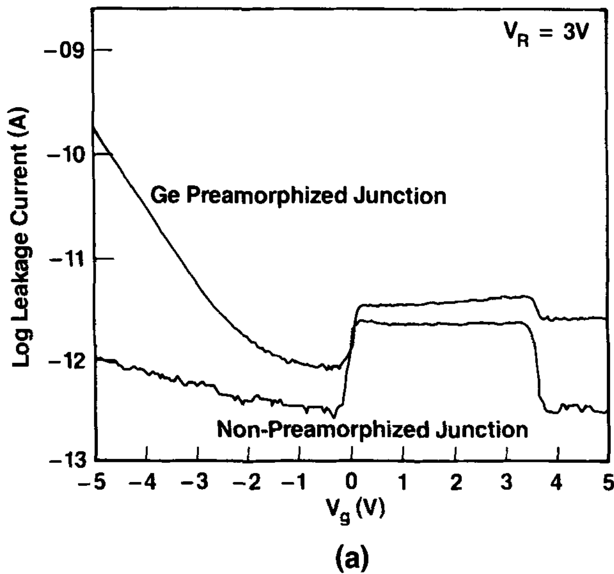


Fig. 7 — Junction leakage a) as a function of Ge preamorphization energy for 0.18 μm n^+ junctions showing enhanced leakage for Ge energies higher than 80 keV[66] and b) as a function of annealing temperature in p^+ junctions for different Si preamorphization energies.[67]



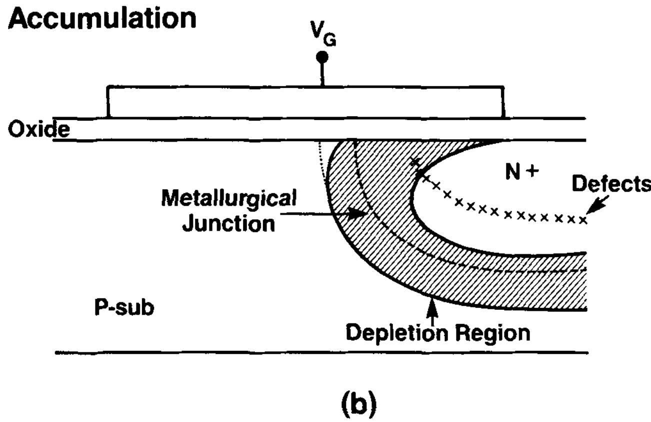


Fig. 8 — a) Gate-induced drain leakage via tunneling giving a comparison of non-preamorphized junctions where tunneling is band-to-band with preamorphized junctions where leakage is tunneling via mid-gap states.[78] b) Schematic illustration of the influence of gate accumulation bias in moving the junction depletion region into an area containing defects.

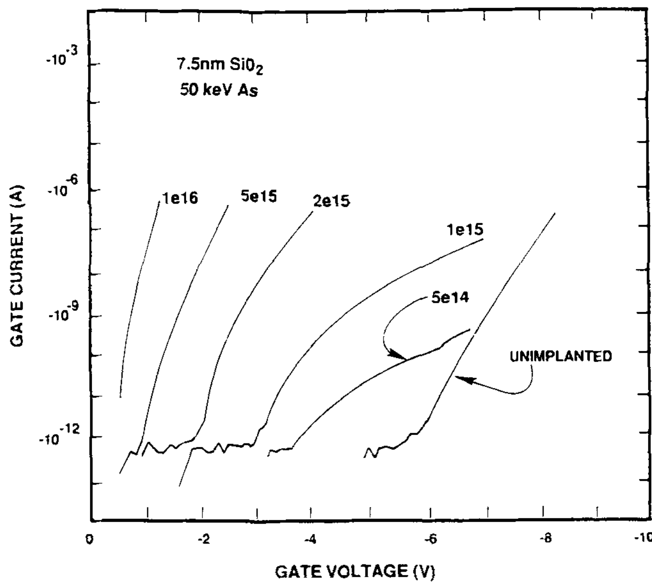


Fig. 9 — Degradation in gate oxide leakage due to junction implantation[94] (measured on 500 × 500 μm gates).

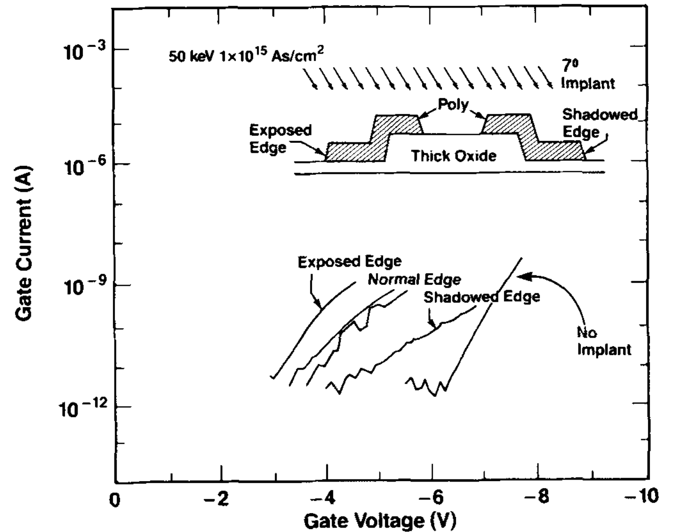


Fig. 10 — Orientation dependence of gate oxide degradation due to ion implantation.[94]

along the edge where ions impact the gate at an angle and the least degradation along the edge where the gate shadows the ion bombardment from the gate edge.[94] Apparently the radiation damage and knock-on of the gate electrode and gate oxide materials at the corner where the gate electrode touches the oxide and into the substrate are responsible for generating tunneling sites.[96]

The implantation of light atoms like boron has little effect, but arsenic and germanium do create considerable knock-on damage and give a very significant gate shorting in oxides thinner than 10 nm for typical source/drain or amorphization doses. The use of oxide spacers at gate edges, as done with LDD designs,[81,82] greatly reduces this degradation; however, this solution obviates the use of preamorphization prior to the light implantation. Unfortunately, precise control of doping profiles in LDD designs is exceedingly important in controlling short channel and hot carrier effects; the design of these structures without using preamorphization poses a challenge for future process development.

Charging of small gates during high current implantation has also been observed[97–99] as a potential cause of shorting. This charging is aggravated when the thin oxide Poly-Si gates are connected to large areas of Poly-Si over thick oxide. This large area "antenna" collects considerable charge which is forced to discharge through the thin oxide region. Flooding with electrons during implant has usually been able to eliminate this degradation. Similar charging can also occur in the final stages of Poly-Si reactive ion etching or during metal etch.

Characterization of Shallow Junctions

The characterization of ultra-shallow junctions is quite difficult. As junction depths scale to 100 nm or less, the conventional measurement techniques, namely secondary ion mass spectroscopy (SIMS) and spreading resistance probe (SRP), become increasingly inaccurate.

The SIMS technique only measures chemical concentrations and not electrically active dopant. The difference between chemical and electrical concentrations is expected to increase as junction depths are reduced as a natural consequence of lowered annealing temperatures giving less initial dopant activation and lower solid solubilities. Cratering, knock-on, and uneven sputter etching all contribute to errors in SIMS profiling. Extensive studies of the SIMS sputter profile technique have been conducted to better understand this analytical technique.[100–109] Both the primary beam energy and species are first-order determinants of the amount of knock-on and cascading as illustrated in Fig. 11.[108] As seen in Fig. 11a, lower primary beam energies give steeper profiles. The energy transferred to a boron atom by a 2 keV oxygen atom (4 keV O_2^+ beam) is about 1.9 keV; this is more than the energy imparted to boron during an 8 keV BF_2 implantation. Under these conditions, the use of such profiling energies is hardly innocuous for ultra-shallow junction profiling. Contrary to the commonly used O_2^+ beam for profiling boron, the use of Xe^+ or Cs^+ produces shallower profiles as seen in Fig. 11b.[108] The shorter range and less efficient energy transfer associated with the use of a heavy profiling beam reduces both knock-on of the dopant being profiled and cascading of the substrate matrix. To date, however, SIMS has not been able to measure dopant gradients much steeper than about 1 decade of dopant decrease per 8–10 nm. With this limitation, even atomically abrupt dopant profiles would yield a SIMS junction depth of about 30 nm.

A further complication in the measurement of ultra shallow junctions is the fact that many of these shallow junctions are formed with metal silicide cladding. The silicide consumes part of the silicon in the junction, further reducing the junction depth in the silicon. In addition, the silicide roughens the silicon surface. Figure 12 shows that boron dopant profiles in $CoSi_2$ have an apparent dependence on the silicide thickness as an artifact of increased silicide roughness for thicker silicides.[47] In contrast to results seen in profiling dopants in silicon substrates, SIMS dopant profiles in silicides are not necessarily improved (sharpened) at lower beam energies, at least for the Cameca SIMS where more glancing beam incidence accompanies lower beam energies. Selective sputtering and shadowing by the rough silicide surface seem to be worsened at the lowest profiling energies and beam angles so that the best profiles are seen at intermediate energies even though some knock on is expected.

Spreading resistance measurements also become inaccurate for ultra-shallow junction measurements due to carrier spilling, non-uniform shallow bevels, and the uncertain relationship between spreading resistance values and dopant concentration.[110–114] To obtain spreading resistance profiles for ultra-shallow junctions, ultra-shallow bevel angles are required on samples. Two aspects of this shallow bevel require special attention and refinement: 1) the production of a smooth (damage and scratch free) reproducible surface during the lapping and patterning and 2) attaining a uniform bevel angle with no rounding near the surface. Control of the probe tip preparation is critical to reducing the loading force and subsequent indentation into the surface. In addition, the analysis of spreading resistance data requires further refinement. Many different approximations have been proposed and used to reconstruct the doping profile from the spreading re-

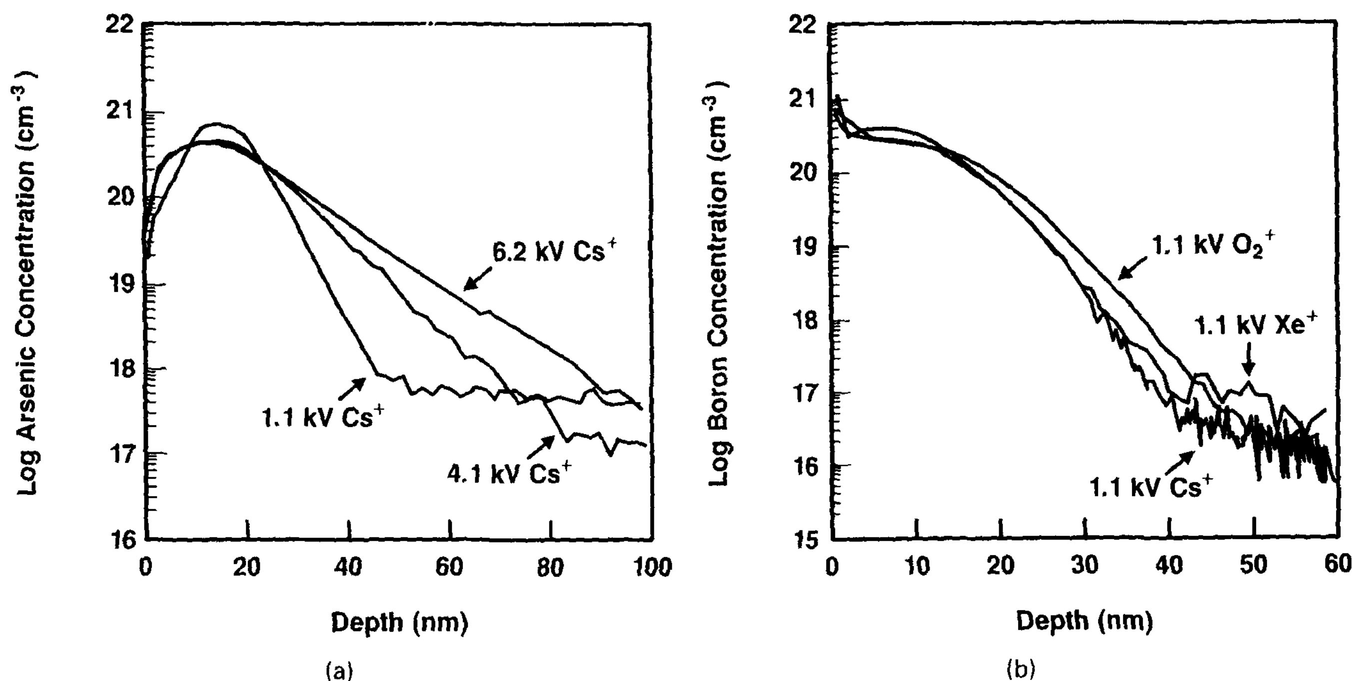


Fig. 11 — Comparison of SIMS profiles of boron vs a) Sputter profiling energy and b) Sputtering species for Cameca IMS-3f.[109]

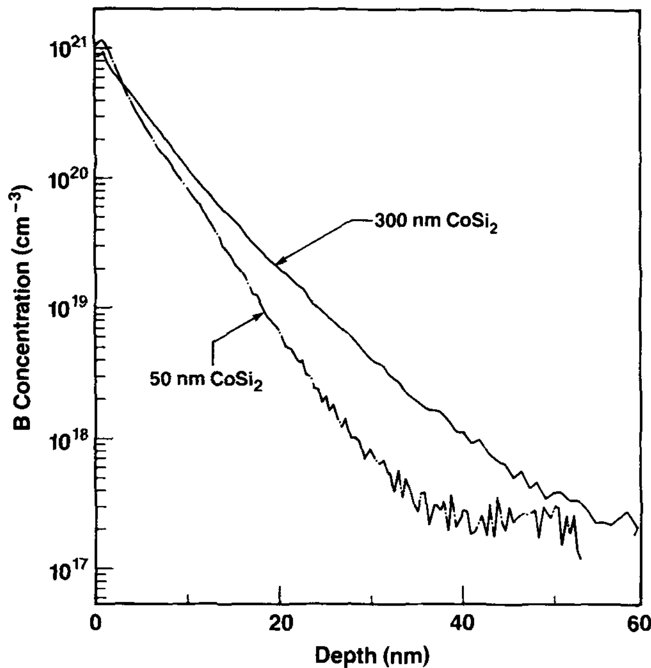


Fig. 12 — Effect of silicide thickness on measured SIMS profiles of *B* in $CoSi_2$.[47]

sistance profile; however, at present it is not possible to obtain an exact solution using the Poisson-Boltzmann equation.

SILICIDE FORMATION ON SHALLOW JUNCTIONS

The SALICIDE process is increasingly being adopted for junctions of 0.25 μm and below as a technique to reduce diffusion resistance. The process typically uses the evaporation of titanium metal to selectively react with exposed silicon to form $TiSi_2$ over junctions. Since the energy level of $TiSi_2$ is near the center of the silicon bandgap, this material provides equally low contact resistance to both n-type and p-type junctions. The process is limited, however, by several factors: silicon (junction) consumption during the metal/silicon reaction, dopant redistribution in the silicide increasing the contact resistance, and dopant evaporation. For instance, the disilicides of titanium and cobalt have found the most widespread application. Both of these materials have a resistivity of about 15 $\mu\Omega$-cm and each consumes about as much silicon as the amount of silicide formed. Empirically it has been observed that junction leakage increases whenever the silicon consumption becomes larger than about half of the junction depth, particularly when $TiSi_2$ is used. Thus silicided junctions are limited to about 2 $\Omega/\Box$ or greater for junction depths below about 150 nm. Dopant depletion by the silicide can reduce the dopant concentration at the silicide/silicon interface by a factor of ten and must be carefully controlled by proper annealing to avoid unacceptably large increases in contact resistance. Furthermore the presence of a polycrystalline silicide over heavily doped junctions provides a rapid pathway for the evaporation of excessive quantities (over 50%) of dopant.

Several alternatives, as outlined in Table IV, to the conventional salicide process have been examined in some detail. Both the conventional and concurrent approaches, which are described in this section, introduce dopants prior to the silicidation. Of most recent interest is the diffusion of dopants from a silicide source which will be discussed in the next section. With this technique dopants are introduced directly into the silicide or metal; thus, the implantation damage is confined to the silicide and away from the silicon. Since diffusion within the polycrystalline silicide is taken to be very rapid, the junction depth in the silicon is controlled as in the classical constant-source diffusion process.

Dopant Loss and Redistribution During Silicide Formation

Dopant loss from pre-existing junctions during silicide formation occurs by several mechanisms.[115] Studies have shown that dopant segregates into the metal ahead of the growing silicide interface, in the titanium case. When silicide formation is performed in a nitrogen atmosphere, dopant can be left in the outer oxygen- and nitrogen-rich layer, often designated as TiON. This dopant is lost when the layer is selectively etched away as part of the selective alignment process. Rapid diffusion of dopant, most likely via grain boundaries, into the silicide and completely through the silicide where it can evaporate provide two additional mechanisms for dopant loss. Traditionally, evaporation of dopant has been minimized by the use of capping oxide layers; however, dopants can diffuse into the oxide layer and be lost for all practical processes even though they remain within the sample. Table V gives examples of the dopant loss associated with the formation of

Table IV. Silicided Shallow Junctions

Conventional Junction	Concurrent Junction	Metal Source	Silicide Source
Device Patterning	Device Patterning	Device Patterning	Device Patterning
Implantation	Implantation	Metal Deposition	Metal Deposition
Junction Anneal	Metal Deposition	Implantation	1st Silicide Anneal
Metal Deposition	1st Silicide Anneal	1st Silicide Anneal	Selective Etch
1st Silicide Anneal	Selective Etch	Selective Etch	Silicide Formation
Selective Etch	Final Anneal	Anneal	Implantation
Silicide Formation	—	—	Junction Anneal

Table V. Dopant Loss in Silicided Shallow Junctions[114,47]

Process	Dopant Loss		Mechanism
	As	B	
Conventional Junctions			
Annealing Bare Silicon (w Ge)	10%	25%	Evaporation
Annealing Bare Silicon (w/o Ge)	20%	—	Evaporation
Annealing Oxide Capped Si	10–20%	25%	Diffusion into Oxide
Silicided Junctions			
Silicide Formation	10%	30%	Snowplow into TiON
Silicide Anneal	5–15%	35–65%	Evaporation from Silicide
Silicide Anneal	20–40%	35–65%	Diffusion into Silicide
Concurrent Silicided Junctions			
Silicide Formation (w/o Ge)	10–20%	40% (est)	Snowplow into TiON
Silicide Formation (w Ge)	10–20%	60% (est)	Snowplow into TiON
Junction Anneal (w Ge)	60–85%	40%	Evaporation from Silicide
Junction Anneal (w Ge)	70%	90–95%	Diffusion into Silicide
Junction Anneal (w Oxide, w/o Ge)	85%	40–60%	Diffusion into Silicide
Silicide Diffusion Source			
$CoSi_2$ Diffusion Source	40–95%	10–70%	Evaporation

60 nm of $TiSi_2$ on 200 nm junctions.[47,115] This table shows that a considerable amount of dopant, both boron and arsenic, can be lost during junction formation, and that the loss is greater when silicide processes are employed. Nevertheless, a lot of dopant is lost even without silicidation. The results of dopant redistribution due to silicide formation are seen in Fig. 13. The doping concentration is depressed at the silicide/silicon interface; this depression is larger for higher annealing temperatures. Since the contact resistance is critically dependent on this concentration, the contact resistance is degraded by this dopant depletion. Recalling, from Tables II and III, that contact resistance and diffusion resistance are components of the total device resistance, it is apparent that increased contact resistance offsets the benefit of reduced diffusion resistance in these silicided junctions. In the extreme case there might not be any benefit at all in using silicides.[39,40] Figure 13 also illustrates one of the SIMS measurement issues with shallow junctions, namely the considerable spreading of the titanium profile into the underlying silicon. This broadening is particularly apparent when Cs^+ is used as the incident ion beam.

A simple example illustrates the impact of this dopant redistribution: a non-silicided junction for a typical 1 μm technology device ($W/L = 3$, 2 μm $\times$ 1 μm contacts spaced 0.5 μm from the gate) might have a series resistance, $2(R_c + R_d)$, of about $2 \cdot (50 + 200/6) = 170\ \Omega$ (for $\rho_c = 10^{-6}\ \Omega\text{-cm}^2$, $\rho_d = 200\ \Omega/\square$). After silicidation, the contact resistivity of the metal to the silicide is reduced to $\sim 10^{-8}\ \Omega\text{-cm}^2$ making that component of the contact resistance only 0.5 Ω. However, even though the silicide has a low sheet resistance, say 3 $\Omega/\square$ in this example, dopant redistribution in the extreme case could reduce the silicide/silicon contact resistivity to $10^{-5}\ \Omega\text{-cm}^2$. A typical silicide to junction area would be 3 μm by 2 μm giving a total device contact resistance of $2 \times (10^{-5}\Omega\text{-cm}^2/3\ \mu\text{m} \cdot 2\ \mu\text{m}) = 330\ \Omega$ or nearly twice the series resistance of the non-silicided junction. Fortunately, the dopant depletion problem can be reduced by a) increasing the doping concentration particularly near the junction surface, b) restricting the silicide thickness to reduce the amount of junction (dopant) consumed, c) minimizing the anneals after silicide formation, or d) introducing more dopant into either the silicide or the metal[39,40] either prior to or after silicide formation.

One key question, still largely unanswered is the effect of silicide formation on dopant diffusion. The presence of excess vacancies generated by silicide formation when silicon is the diffusing species, as postulated to explain enhanced damage removal in $TiSi_2$ silicided junctions in the next section, would be expected to also have an impact on dopant diffusivity. Yet the experimentally observed impact in $TiSi_2$ is, at most, minor for conventional junctions where the junction is implanted and annealed prior to silicide formation.[115] The observation of enhanced antimony diffusion long after the formation of $TaSi_2$ seems to suggest extraordinarily long lifetimes for excess point defects, certainly much longer than are used to predict implantation-defect-enhanced diffusion.[70] The interpretation of data from concurrently formed junctions, where silicide formation and junction recrystallization and anneal occur simultaneously, is even less clear. In the concurrent process, dopants are nearer the surface, i.e. in the path of the growing silicide, than with conventional junctions. The extreme loss of dopant in this case can then reduce the dopant diffusivity simply by lowering the dopant concentration. Furthermore, excess point defects are already present during the initial stages of annealing of implanted samples; it is not apparent that one should expect vacancy generation when the metal reacts with an amorphous substrate, and if such vacancies were indeed generated, it would seem likely they would recombine with other point defects from the newly-recrystallized substrate.

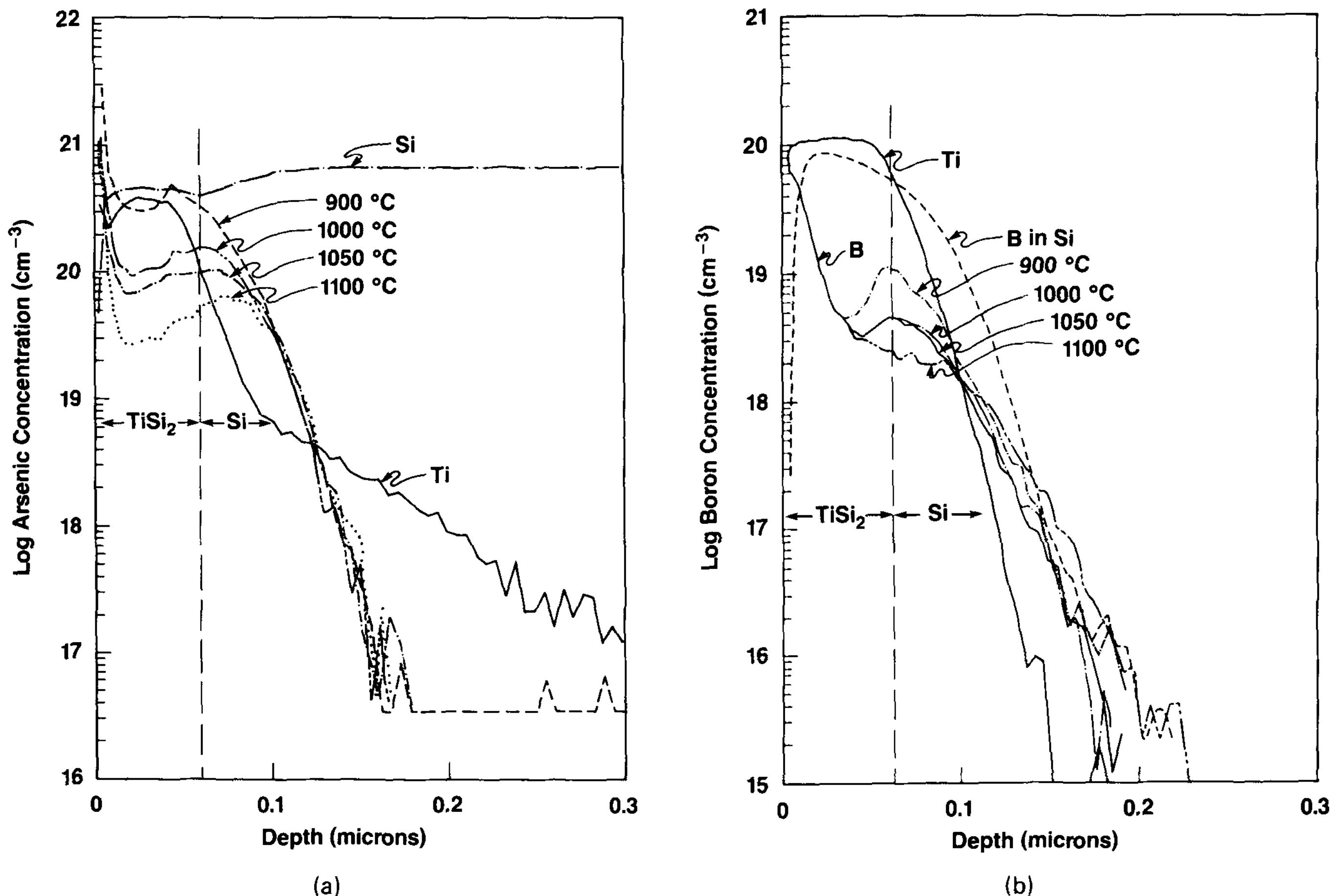


Fig. 13 — Dopant redistribution in concurrently-formed, $TiSi_2$-silicided n^+ and p^+ junctions after different annealing cycles.[115]

DAMAGE REMOVAL DURING SILICIDE FORMATION

One unanticipated benefit of siliciding shallow junctions is the reduction of crystal damage due to the silicide formation process.[17,18,20–22] Figure 14a compares cross sectional TEM micrographs of control and silicided p^+ junctions using $TiSi_2$ showing the elimination of defects in the silicided junction. Figure 14b schematically illustrates one proposed mechanism for this defect reduction: vacancies are generated as silicon atoms diffuse from the substrate through the forming silicide. These silicon vacancies then diffuse into the junction where they recombine with the interstitials that form the end-of-range dislocation loops thereby reducing the size or number of these loops. This model is far from a settled question, however. Ohdomari[17] reports vacancy generation during the formation of Pd_2Si where the metal is the diffusing species; Fahey and Dutton[116] report no vacancy generation during oxidation of WSi_2 where silicon is known to diffuse out of the substrate and into the silicide. Hu[19] has attributed enhanced diffusion to the point defects associated with tantalum silicide layers. Presumably these excess point defects should be responsible for both enhanced diffusion and defect elimination. Unfortunately, a silicide process has not been demonstrated which gives reproducible, complete elimination of crystal damage for the thin silicide films of typical interest on shallow junctions. On the other hand, the high stresses in thick silicide layers can be responsible for the creation of defects, particularly at gate or oxide edges.[43,117,118]

Silicon Consumption and Junction Leakage

Even though the silicon consumed by silicidation is typically some distance away from the junction depletion region, the presence of silicide on shallow junctions has been shown by many authors[13,14,16,21,29–32,38–43] to have an important electrical effect on the junction itself. Figure 15a illustrates the need for a considerable "buffer" between the bottom of the silicide and the metallurgical junction. Once the silicide thickness becomes greater than about half of the junction depth, the diode leakage increases. The need for an appreciable buffer makes scaling of junctions increasingly difficult. Unfortunately, the need for this buffer is very poorly understood. Silicides showing good, low leakage diodes even when 90% of the junction is consumed[119,120] are balanced with reports of high leakage with moderate buffer layers. Although the results are too sketchy to be conclusive, cobalt silicide may be more amenable to greater silicon consumption than $TiSi_2$ while still giving low diode leakage. If this observation is true, cobalt silicided junctions may be more extendible to

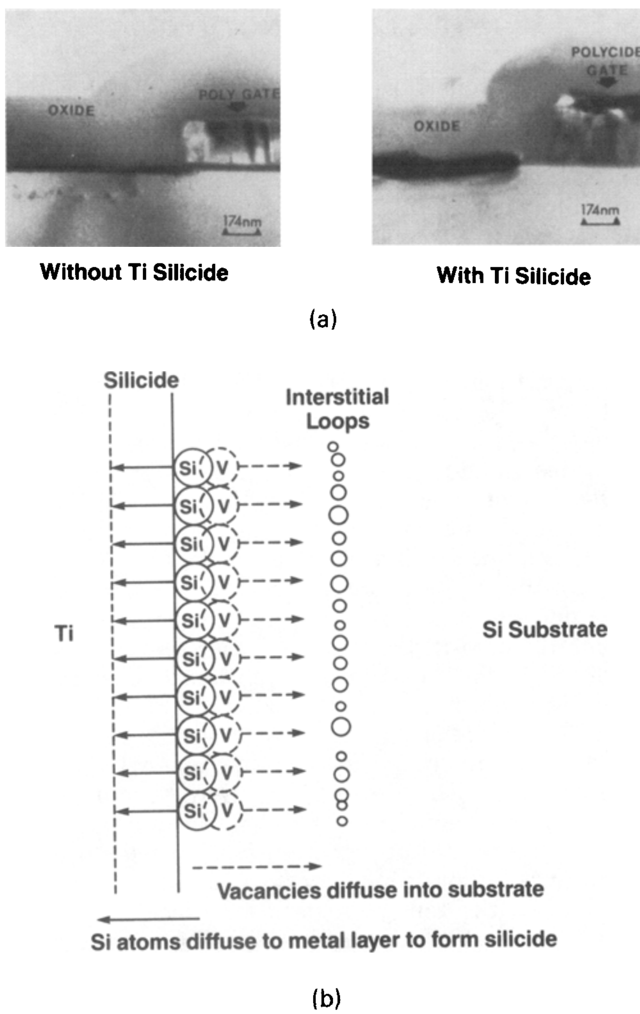
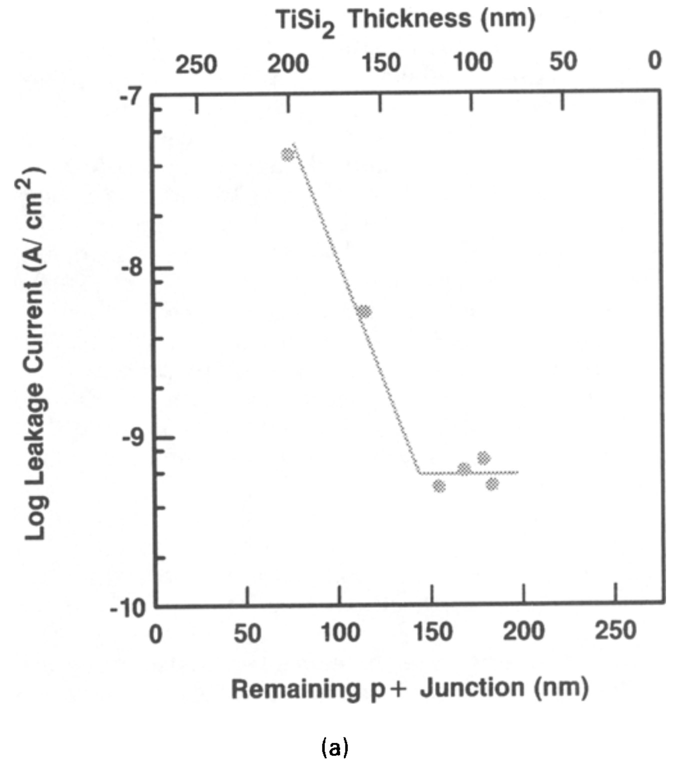


Fig. 14 — a) Damage reduction in $TiSi_2$ silicided p^+ junctions. b) Impact of point defect injection on defect removal.[20,21]

shallower junctions where the buffer thickness is reduced since equal thicknesses or sheet resistances of $CoSi_2$ and $TiSi_2$ consume about the same amount of silicon. Although it has a more limited stability and has not been very extensively examined, nickel silicide (NiSi) gives the least silicon consumption when normalized to its conductivity. Palladium silicided, arsenic junctions present a conceptually ideal case where arsenic is snowplowed ahead of the forming silicide thereby ensuring a high interfacial concentration along with considerable dopant below the silicide.[121] Unfortunately its limited thermal stability makes it somewhat difficult to practically capitalize on this advantage.

Several factors probably contribute to the variability seen in leakage results. The first is the silicide roughness, where considerable variations from study to study have been noted. Presumably the silicide roughness depends on substrate doping, substrate crystallinity,[122] native oxide thickness, annealing ambient, as well as the time and temperature of silicide formation or subsequent annealing. With very high temperature anneals, the silicides are unstable[47,48,118,123–125] and have been observed to agglomerate into balls, leaving exposed silicon. This will be discussed in more detail later. Typically, the magnitude of the roughness is about one-third of the silicide thickness, and the thickest region of the silicide must be considered when designing the buffer not the average thickness. Second, in many cases the silicon consumption during silicide formation is



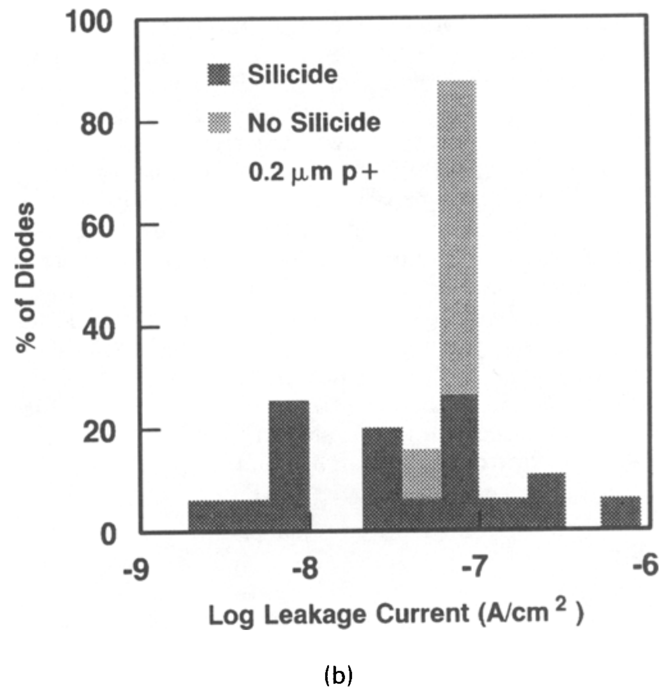


Fig. 15 — Leakage in silicided shallow junctions: a) leakage as a function of the amount of junction consumed,[16] b) statistical distribution of silicided and non-silicided diodes as measured in heavily accumulated gated diodes to emphasize edge tunneling.[21]

considerably greater than would be predicted from the simple ratios of silicide thickness/silicon consumption based on density. In the case of the widely-used $TiSi_2$, some Si is lost in the TiON layer formed with nitrogen annealing. If argon is used as the annealing atmosphere, considerable silicon is lost laterally into the titanium. Figure 16 shows cross sectional TEMs[118] of nitrogen and of argon annealed silicide showing marked differences in the amount of silicide formed. One can also speculate that the amount of silicon consumed is excessive when excess metal is used to form the silicide. To ensure a minimum sheet resistivity spec, many processes use more metal than is necessary to form the desired silicide thickness. It is reasonable to assume that some silicon is lost when the excess metal is etched off.

Several studies have identified the diode edge as the critical design area to minimize leakage.[13,14,39,40] Since the lateral junction motion is less than the vertical motion, the lateral buffer is less than the vertical buffer. Rough silicides and high silicon consumption aggravate the edges first. Also many different processes can contribute to excess junction consumption at pattern edges, or "trenching". These include the dry etching of the gates, ion implantation of the junctions, and, most important, excess silicon consumption that contributes to lateral silicide formation. Although severe trenching has been observed in the formation of $NiSi_2$ patterns,[126] it is apparently seldom seen in other Si-diffusion silicide formers like $TiSi_2$; however, the trenching may still explain the seeming superiority of $CoSi_2$ over $TiSi_2$. In addition, many manufacturing processes employ at least one oxide dip etch after junction formation but prior to silicidation. This etch has the effect of "walking" out the oxide window which serves to define the silicide pattern even closer to the junction edge so that junction leakage actually becomes dependent on the field isolation scheme.[13,14] The addition of dopant directly into the silicide to diffuse into the silicon has been shown[39,40] to be one clever way to eliminate this edge leakage.

SILICIDES AS DIFFUSION SOURCES FOR SHALLOW JUNCTIONS

Recently considerable interest has been shown in the use of silicide sources for shallow junction diffusion. Cobalt silicide,[30–32,35,37–8,42,43,46,47,49,139,142] $TiSi_2$,[23,24,27,33,34,39–41,43,44,51,134,140,141] WSi_2,[25,34,127–8] NbSi2,[7] $MoSi_2$,[135,137] and $TaSi_2$[28] have received attention. The concept of using the silicide as a diffusion source appears to have been a logical extension of the use of ion beam mixing through metal to form the silicide.[127–143,7,24,26,29–32,38,46] Implantation of metal with a dopant species, i.e. As, rather than inert gas or Si itself could simultaneously form both the silicide and the junction. The smoother silicide/silicon interface reported for ion beam mixing[31] provides an added bonus. Today, however, there are several strategies, as shown in Fig. 17 for using silicide sources for junction formation.

Although there is a continuum of possibilities for implanting into silicide sources, it is convenient to consider four cases in Fig. 17: 1) deep implantation through the silicide (metal); if the implant is deep enough, it can put the junction depth beyond the knock-on metal which otherwise might be responsible for poor leakage characteristics. However, this technique is restricted to deep junctions which could be formed by other techniques anyway, and it generates crystal damage just as any high energy implant process. 2) implantation peaked near the silicide (metal)/silicon interface. This approach maximizes the ion beam mixing effect of the implant but at the expense of creating considerable knock-on of metal into the junction region. In addition crystal damage in the silicon is generated by the implantation. This approach is best used with implantation through metal rather than silicide. The silicides and metals typically employed have shorter implantation ranges than in silicon, as listed in Table VI.[144] Thus even though the implant peak is placed at the interface, there can still be considerable straggle into the silicon resulting in a deep as-implanted profile. This extra depth, as well as the

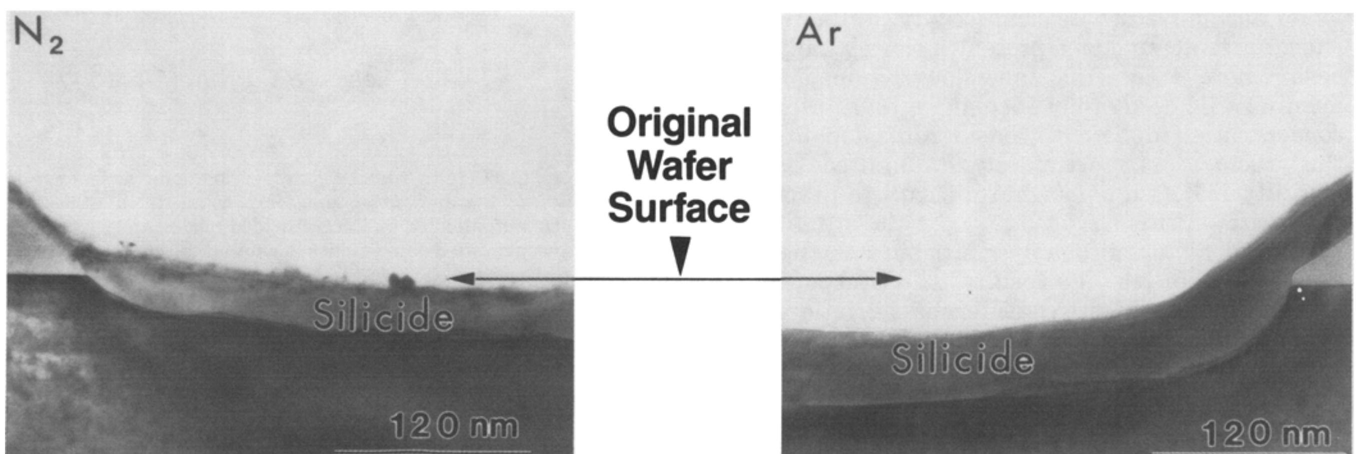


Fig. 16 — Silicon consumption for titanium silicided shallow junctions for 30 nm Ti deposition and formation at 650° C in N_2 on the left or in Ar on the right.[118]

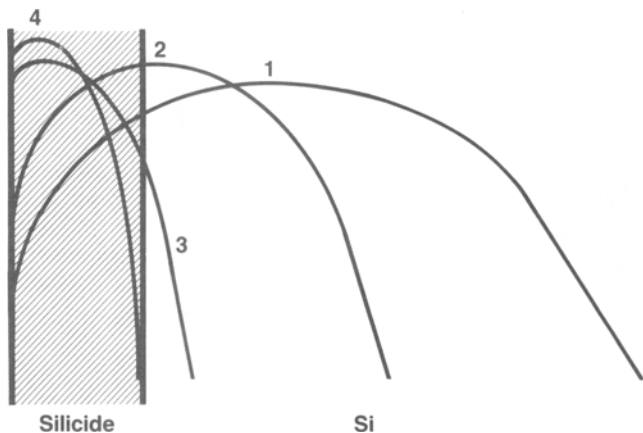


Fig. 17 — Strategies for silicide (metal) sources for junctions.

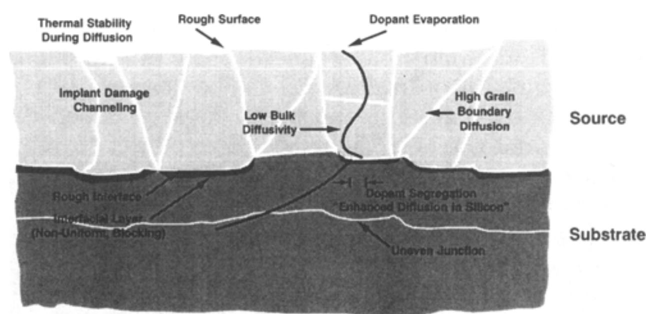


Fig. 18 — Issues associated with diffusion from polycrystalline diffusion sources.

knock-on region, is less of an issue when this silicon will be consumed in forming silicide from a metal source than it is when starting from the silicide. However, implantation through metal as a source for boron, p^+ junctions would require an accompanying implantation of a heavier species, *i.e.* Si, Ar, Ge, to promote cascade mixing. 3) implantation of the dopant tail through the silicide and into the silicon. This technique can be used to avoid damaging the silicon and can reduce the amount of dopant which must subsequently diffuse through the silicide and into the silicon in order to form a good junction. On the other hand, it is especially sensitive to silicide thickness fluctuations. 4) implantation of the dopant entirely within the silicide or metal layer. Using the silicide as a diffusion source (SADS) probably provides the simplest case to analyze; it also requires use of the lowest ion implantation energies and is most vulnerable to excessive dopant evaporation from the silicide surface during diffusion because of the shallow starting profile. Furthermore, for this technique to be useful, the dopant diffusion through the silicide must be rapid and the silicide must be stable for the thermal cycles required to drive dopant into silicon.

Polycrystalline Diffusion Sources

Polycrystalline diffusion sources offer several advantages for shallow junction formation, but they also present several serious challenges. Some of these issues associated with these sources are illustrated in Fig. 18. One of the prime advantages of a polycrystalline source is that the ion implantation damage can be confined to the poly layer rather than in the silicon where it is near the junction. Another plus is that polycrystalline sources offer the hope of offering a uniformly, heavily-doped source from which a classical constant-source diffusion process can be conducted; the heavy doping provides a high interfacial doping concentration and thus low contact resistance. The problems as outlined in the figure include the fact that many polycrystalline sources, especially the silicides are not smooth. Since the junction is seen to follow the roughness of the silicide,[37,43] the junction is therefore rough also. Even though the junction roughness follows that of the silicide and thus may reduce the "buffer" requirement as discussed earlier, the impact of such rough junctions on junction leakage or other device properties (snapback, short channel effect, hot electron stability) has not been addressed in any detail. The presence of a surface oxide or barrier prior to the formation or deposition of a polycrystalline diffusion source might also be responsible for aggravating the silicide roughness or acting as a barrier to diffusion as is the case when Poly-Si is used to diffuse bipolar emitters.[145–147] In many systems, as will be shown shortly, the bulk diffusivity is small compared to the diffusion of dopant in silicon. Thus the dopant does not homogenize within the silicide and instead exhibits either a U-shaped concentration profile with high dopant concentrations at both sil-

Table VI. Range of Dopants in Silicides from TRIM Simulations[144]

	8 keV BF_2		15 keV AS		25 keV Ge		20 keV Si	
Material	R_p (nm)	ΔR_p	R_p (nm)	ΔR_p	R_p (nm)	ΔR_p	R_p (nm)	ΔR_p
$TiSi_2$	6.7	3.6	10.0	3.9	14.9	5.8	21.4	11.2
$CoSi_2$	6.2	3.5	9.0	3.7	13.2	5.5	19.9	11.0
PtSi	5.6	3.2	6.9	3.8	9.5	5.2	15.2	8.7
Pd_2	5.9	3.4	7.4	3.9	10.8	5.8	17.1	9.6
NiSi	5.1	2.8	7.1	3.0	10.3	4.5	15.4	8.0
Si	10.5	5.8	16.6	5.8	24.5	8.9	26.6	12.4
Co	4.9	3.2	6.5	4.2				
Pt	5.4	3.0	5.0	3.0				
Pd	5.3	3.0	5.8	3.3				
Ni	4.6	2.6	5.8	2.8				

icide surfaces and a low concentration in the center or a profile which has a dopant peak at the polycrystalline/silicon interface. That behavior is illustrated for both arsenic and boron in poly-silicon in Fig. 19[84] and $CoSi_2$ in Fig. 20.[35,47] The effects of high grain boundary diffusion are further complicated when additional grain growth accompanies the diffusion process. This grain growth changes the dopant distribution between the grains and the grain boundaries. As will be discussed later, the conditions employed in diffusion from silicide sources can seriously encroach on the limits of the silicide thermal stability.

Introduction of Dopant and Diffusion in Silicides

The introduction and diffusion of dopant into the silicide layer requires careful attention. A careful examination of previously published SIMS dopant profile data in silicides[148] reveals the presence of considerable tails. These long tails, if real, would make it very difficult to contain the implanted dose within a thin silicide layer. Our studies have taken two approaches to this issue.[47] First we have used silicon or germanium preimplantation to amorphize or at least create sufficient disorder in the silicide to greatly reduce channeling. Even though the silicides are polycrystalline to begin with, their grain sizes are much larger than the film thickness, and X-ray studies[43,122] in polycrystalline films have certainly shown a preferential orientation. In addition some silicides like $CoSi_2$ have been shown to grow epitaxially.[149] Thus some channeling of implanted species might be anticipated in silicide films. Figure 21 shows top views of wafers that were half-implanted with Si and half with Ge prior to dopant implantation. These photos show a contrast between the implanted and unimplantated wafer halves indicating that preimplants indeed change the properties of the silicide; extensive TEM analysis[47] has shown that the silicides do not become amorphous but rather contain a band of heavily-defected material. The second approach to understanding dopant tails in silicides was to examine the SIMS technique. Several important observations have come out of that work. Lower SIMS profiling energies actually broaden the measured dopant peak, in contradiction to the result found in profiling single crystal silicon; this broadening is attributed to masking and preferential sputtering by the rough surface. Further as shown earlier in Fig. 12, the silicide thickness itself has a pronounced effect on the measured profile with thicker silicides producing broader profiles. Additional experiments, measuring dopant penetration through a thin silicide layer into the underlying silicon were conducted by etching off the silicide; typically the measured dopant penetration was no greater than the residual silicide left from an imperfect etchoff. Based on this work it seems reasonable to conclude that at least

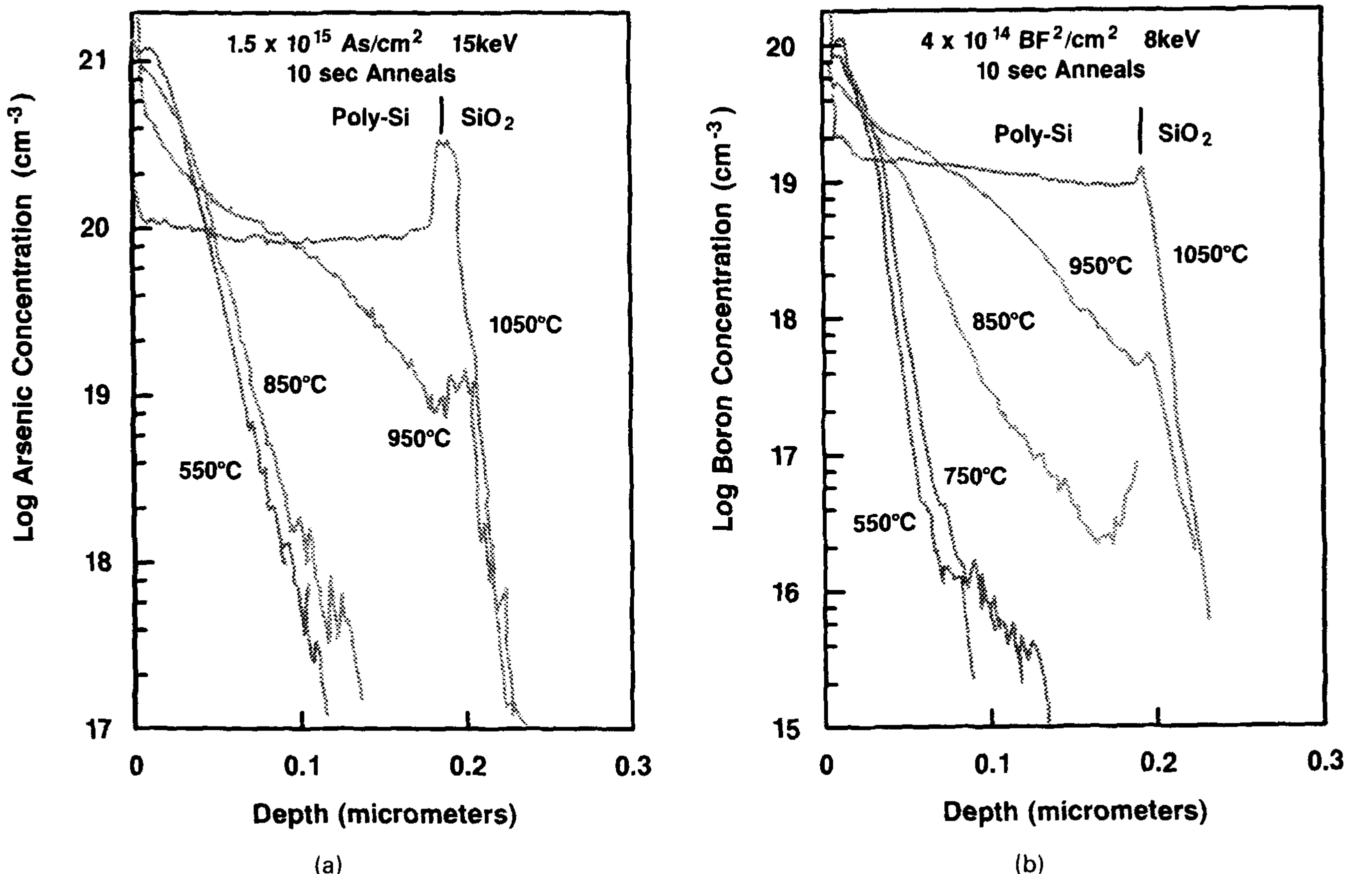


Fig. 19 — Diffusion of implanted a) boron, b) arsenic in 0.3 μm Poly-Si as a function of annealing.[84]

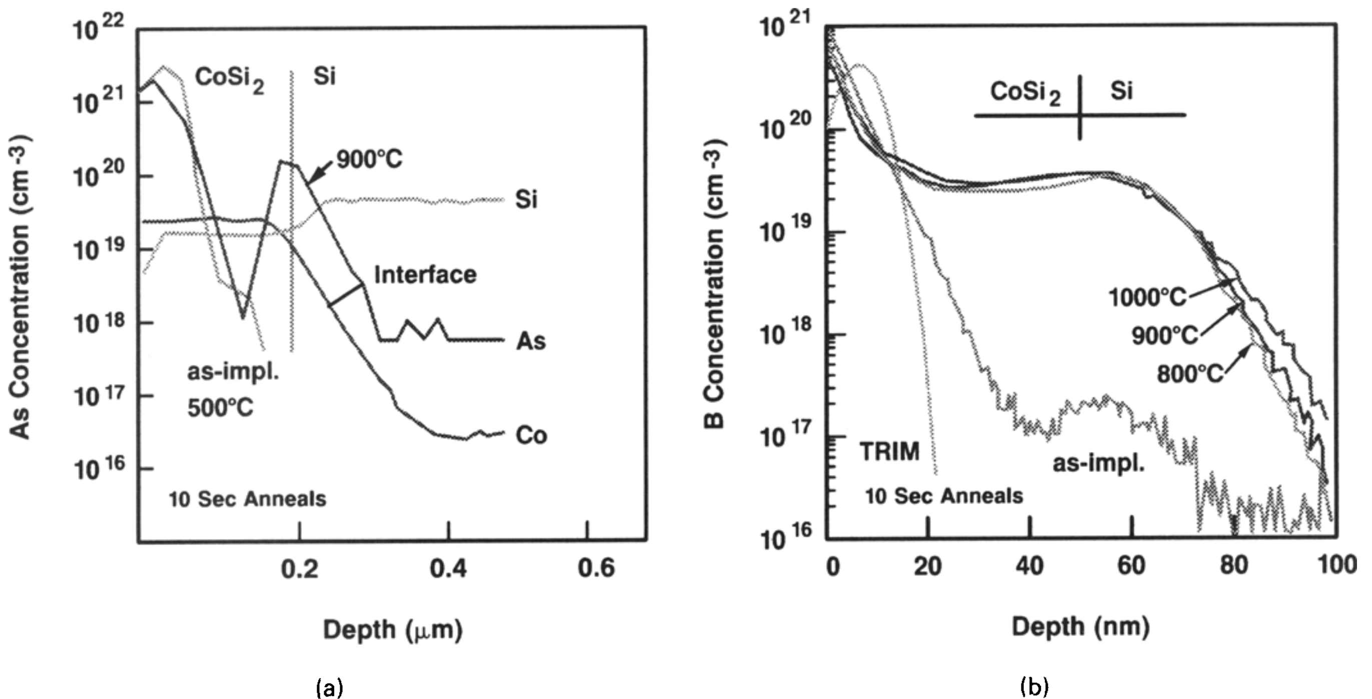


Fig. 20 — Diffusion of implanted a) arsenic,[35] b) boron[47] in $CoSi_2$ as a function of annealing.

the majority of the measured exponential dopant tails are artifacts, and that the actual profiles are reasonably predicted by TRIM as in Table VI.

Diffusion in silicides has been the topic of several studies.[150–154] Figure 20a[35] illustrates the problem associated with the diffusion of arsenic in $CoSi_2$. The arsenic diffusion is essentially entirely via grain boundaries for the range of thermal cycles that are reasonable to consider. Even at the middle of the temperature range, the SIMS profiles are heavily U-shaped, reflecting a thin grain-boundary layer that contains a high doping concentration and very lightly doped grains. The large surface area at the silicide/silicon interface gives a high SIMS concentration. While a high grain boundary diffusivity is beneficial in rapidly establishing a high doping concentration at the silicon/silicide surface, it also is responsible for rapid transport of dopant to the surface where it can readily evaporate. Table V illustrates the large amount of boron and arsenic that can be lost during a diffusion cycle. When grain boundary diffusion is slow in the silicide layer compared to bulk diffusion in the silicon, the dopant concentration at the silicide/silicon interface is often depressed. Since the as-implanted dopants are located closer to the surface than the silicon/silicide interface in the SADS process (case 4 of Fig. 17), evaporation from the surface competes with diffusion toward the silicon and some very interesting reversals in junction shape and depth can be observed as the diffusion temperature is increased. The interface doping concentration can in some instances be observed to decrease with temperature even though the diffusion in the silicide improves with increasing temperature.[47] This decreased dopant concentration is presumed to be due to the combination of increased evaporative loss at higher temperatures coupled with relatively higher diffusion in silicon than in silicide grain boundaries at higher temperatures.

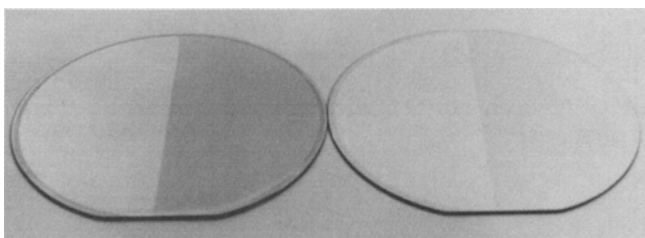


Fig. 21 — Damage associated with implantation of Ge (left half of left wafer) or Si (left half of right wafer) into $CoSi_2$.[47]

Stability of Silicides

The thermal stability of the silicide source defines the limit of the allowable time and temperature for diffusion of dopants into the silicon. The primary manifestation of the silicide instability is its resistivity increase as the annealing temperature is increased (see Fig. 22a). In some cases, *e.g.* NiSi, the instability is the result of the formation of other, more silicon-rich silicide phases. For the silicides more commonly used as diffusion sources, *i.e.* $CoSi_2$ and $TiSi_2$, the increase has been attributed to the agglomeration and spheroidization of the silicide.[123–125,48,118,154,155] In the extreme case, the silicide balls up and exposed silicon can be seen. Unfortunately for shallow junction formation, this instability is a strong function of the silicide thickness with thinner silicides degrading at lower temperatures. It is convenient to monitor the time and tem-

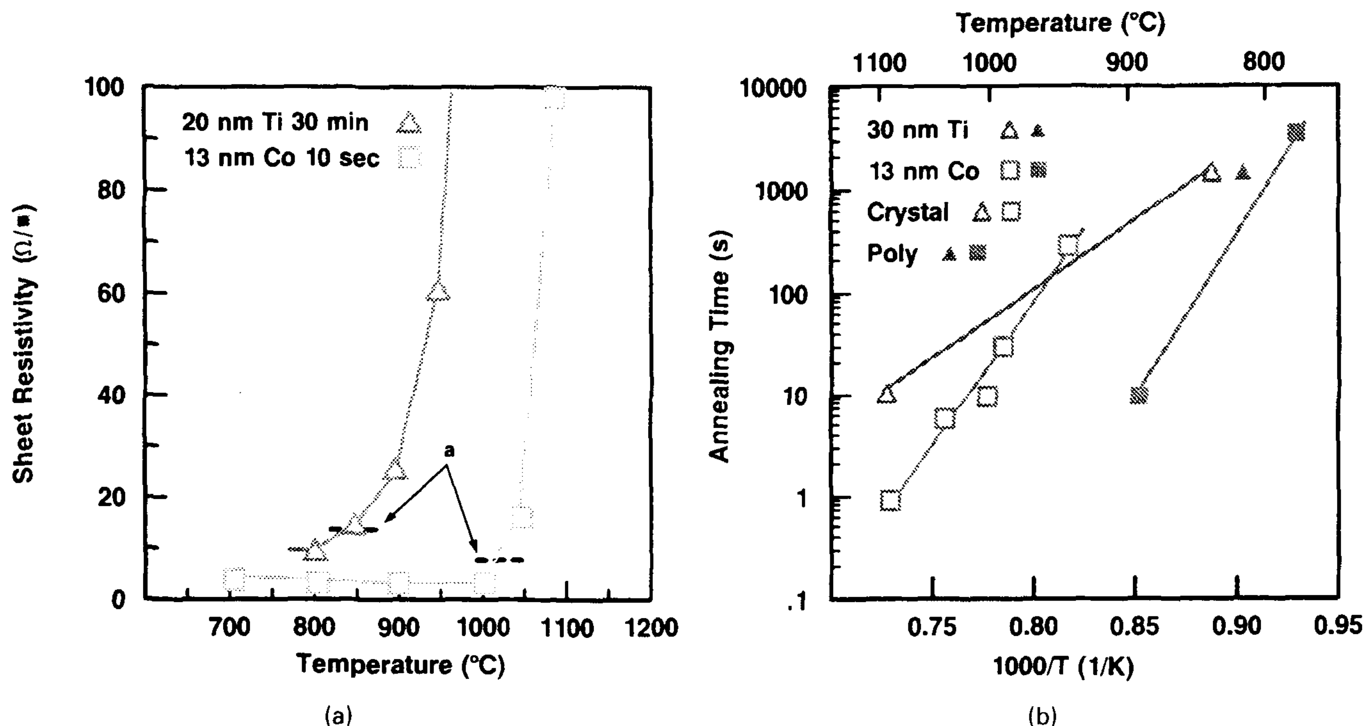


Fig. 22 — Stability of silicides during high temperature annealing: a) temperature dependence for 30 min $TiSi_2$ anneals,[123,124] and 10 sec $CoSi_2$[47] anneals. b) temperature dependence for a fixed degradation (30% increase) for both silicides on single crystal[47,123,124] and Poly-Si.[48,155]

perature at which a 30% increase in sheet resistance occurs. Using this criterion, the kinetics of the degradation for $CoSi_2$ and $TiSi_2$ are shown in Fig. 22b. These two silicides are interesting to compare. For typical furnace annealing conditions (~30 min annealing time), $CoSi_2$ is more stable than $TiSi_2$; however, for rapid thermal processing times (~10 sec), the stability order is reversed due to the higher activation energy for cobalt silicide degradation. Especially for $CoSi_2$, the silicides are much less stable on polysilicon than they are on single crystal. In fact a relayering phenomenon has been reported for $CoSi_2$ films on Poly-Si[48] on oxide where, after considerable annealing, the silicide is transported along Poly-Si grain boundaries and is ultimately left as a layer on top of the oxide but below the silicon. For longer furnace annealing times $TiSi_2$ has also been observed to penetrate along Poly-Si boundaries,[125] but this has not been seen with short, rapid thermal annealing even at 1100°; C.[155] Thus the allowable diffusion cycle is quite limited, especially at higher temperatures, for a SADS process using $CoSi_2$ when silicide is present on both polysilicon and on junction regions. The preferred process window for $TiSi_2$ processes appears to be at higher temperatures for short times.

Diffusion in Silicon

Since the junction depth is ultimately controlled by diffusion in silicon, it is important to thoroughly understand the diffusion in silicon. Just as with junction diffusion in silicon from polycrystalline silicon sources (bipolar emitter/base), anomalous diffusion has been reported[42,46,47] when using silicide sources and incorporated in process models.[70] Nevertheless it is quite difficult to unambiguously verify whether diffusion is indeed enhanced in silicon beneath silicide primarily because the accurate measurement of the diffusion depth in silicon is obscured by measurement errors. Figure 23a shows SIMS boron profiles in silicon after diffusion from a $CoSi_2$ source. The times and temperatures were adjusted to give roughly equal junction depths. Figure 23b shows the temperature dependence of the iso-depth diffusion and compares it with the theory for a constant source boron diffusion. The classical constant source diffusion solution, for junction depth, X_j, as a function of time, t, when the diffusion coefficient is independent of carrier concentration is:

$$X_j = 2 \cdot \mathrm{erfc}^{-1}(N_s/n_{sub}) \cdot (Dt)^{1/2} \quad (1)$$

where N_s and n_{sub} are the surface and bulk doping concentrations. In a typical case $N_s/n_{sub} \sim 10^4$ and erfc^{-1} $(10^4) \sim 2.75$. The diffusivity, D, is typically expressed in terms of a pre-exponential, D_o, and an activation energy, E_a:

$$D = D_o \cdot \exp(-E_a/kT) \quad (2)$$

However, at high doping concentrations, the diffusivity of both boron and arsenic are concentration dependent:

$$D_{boron} \sim h(D^o_{iB} + p/n_i \cdot D^+_B) \quad (3)$$

$$D_{arsenic} \sim h(D^o_{iAs} + n/n_i \cdot D^-_{As}) \quad (4)$$

where h is the electric field enhancement term (~2

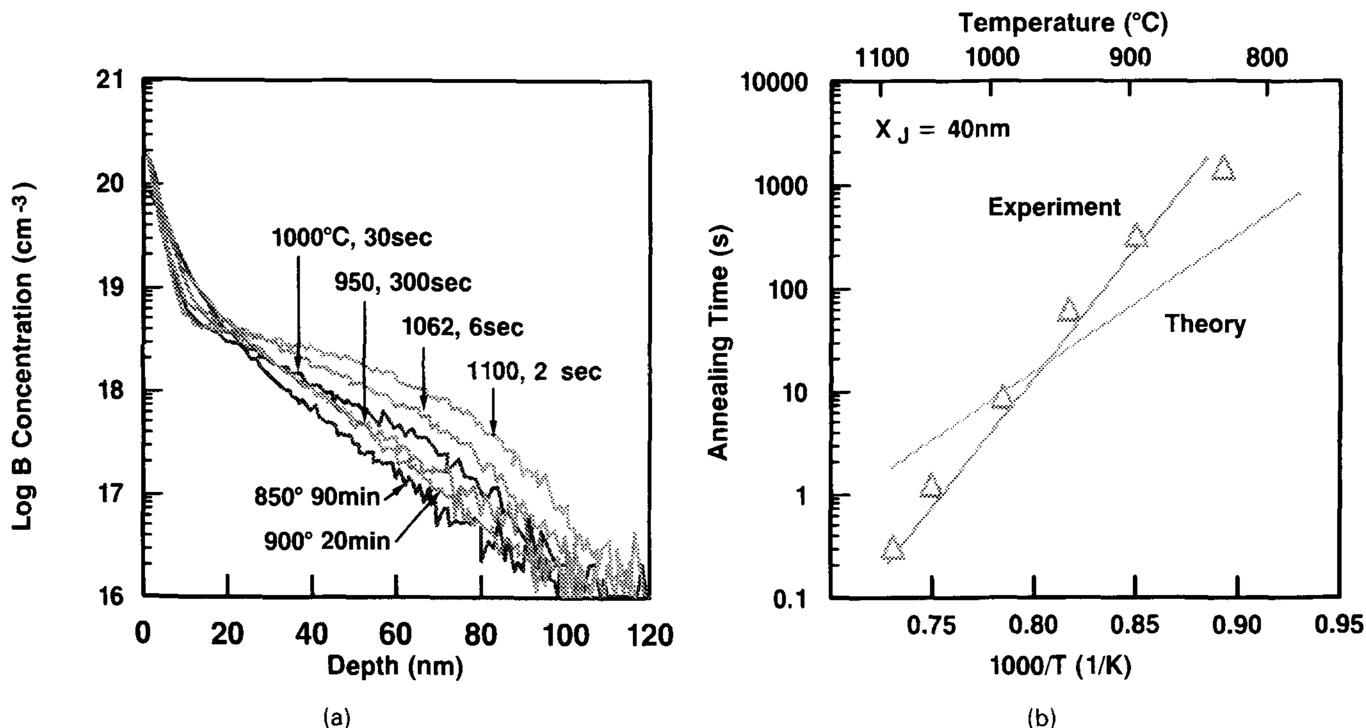


Fig. 23 — a) SIMS dopant profiles of junctions in Si diffused from a $CoSi_2$ source. b) Temperature dependence of the diffusion time needed to diffuse boron 40 nm into Si from a $CoSi_2$ source compared with conventional constant-source diffusion theory.[47,70]

at high doping), and p and n are the hole and electron concentrations which at high dopant concentrations are approximated by the electrically active boron and arsenic concentrations respectively, the D_i^o's are the intrinsic diffusivities of boron or arsenic associated with diffusion via neutral point defects, and n_i is the intrinsic electron concentration approximated by:[156]

$$n_i = 3.87 \times 10^{16} \cdot T^{3/2} \cdot \exp(-(0.605 + \Delta E_g)/kT)(\text{cm}^{-3})$$

$$\Delta E_g = -7.1 \times 10^{-10} \cdot (n_i/T)^{1/2} \,(\text{eV})$$

D_B^+ is the boron diffusion coefficient associated with positively charged point defects and D_{As}^- is the arsenic diffusivity associated with negatively charged defects. At very high doping concentrations, the terms on the right of Eqs. 3) and 4) predominate, and the derived expression[157] for the diffusion depth, X_d, analogous to equation 1), is given by:

$$X_d = 2.3\{(N_s/n_i) \cdot (D_o t) \cdot \exp(-E_a/kT)\}^{1/2}$$

For the case where the diffusivity is very high in the silicide layer and evaporation is negligible, N_s equals the implant dose divided by the silicide thickness. D_o and E_a are the preexponential term and activation energy for the appropriate dopant diffusivity term (D_B^+ or D_{As}^-) responsible for the concentration dependence (0.56 cm^2/sec and 3.42 eV respectively for boron).

From Fig. 23b, the diffusion from a $CoSi_2$ is seen to be "faster" at high temperatures, having a 5 eV activation energy, than would be predicted by the above equation. Presumably, the short times required to form a deep junction at high temperatures reflects an enhanced diffusivity in the silicon. This observation is especially curious since the silicide is formed early in the junction-formation process and excess point defects associated with the silicide formation, which might be responsible for enhanced diffusion, would have been expected to recombine prior to the introduction of dopant. Furthermore, the point defects associated with implantation damage during silicide formation should be confined to the silicide where they would not be expected to enhance diffusion in the silicon. However, in the case of poly-Si diffusion sources, enhanced diffusion has been correlated with the introduction of arsenic via ion implantation and does not occur with in-situ doped poly-Si.[158] Certainly considerably more study is needed to improve our physical understanding of diffusion in silicon when using these silicide sources.

Junction Leakage with Diffusion from Silicides

Low junction leakage (~1 nA/cm^2) has been reported in both n^+ and p^+ diodes made using $TiSi_2$[39–41] or $CoSi_2$[29,31,43,142] diffusion sources. However, the leakage observed appears to be strongly dependent on processing conditions and a considerable amount of discrepancy still exists. When dopants are implanted through metal or silicide (cases 1 and 2 in Fig. 17), high leakage is often observed[7,29,31,140] unless there is sufficient thermal cycle to diffuse the junction well beyond both the ion straggle damage and the knocked-on metal. When the diffusion anneal is long, the leakage appears to be as low as that in unsilicided junctions; however, this process

yields deeper junctions. Implantation of dopant barely past the silicide so that the tail reaches the silicon (case 3 in Fig. 17) would appear to produce a wider process window for obtaining low leakage compared to the case where dopants are totally contained within the silicide. The former case requires less of a thermal cycle to form a good junction and, thus, is less susceptible to slow dopant diffusion, compound formation with dopant, and the silicide thermal instability. The implant energy boundary between these two cases is about 0.32 and 0.51 keV/nm for $TiSi_2$ and 0.34 and 0.55 keV/nm for $CoSi_2$ for boron and arsenic implantation respectively. This boundary can be computed from $R_P + 5\Delta R_P$ values from Table VI.

Special note can be taken for two SADS processes. The first involves boron diffusion from $TiSi_2$ where TiB formation has been postulated[37,43] to explain the poor (slow) junction formation. Interestingly, B_2O_3 is the only phase that has been isolated to date.[41] The second case involves arsenic diffusion from $CoSi_2$ where the arsenic diffusion is by grain boundary diffusion in the silicide making this system especially vulnerable to excessive dopant evaporation and a low interfacial concentration.

SUMMARY

The ability to form low leakage shallow junctions is a key requirement for the success of future generations of ULSI technology. Low energy ion implantation continues to be the starting point for the formation of these shallow junctions. Geometrical shadowing of implants must be avoided to prevent asymmetrical device characteristics. The implantation of high dose arsenic at exposed poly-Si gate edges causes excess gate oxide leakage or even shorting which usually must be eliminated by protecting gate edges with oxide spacers. Preamorphization, either with germanium or with silicon, has been shown to be effective with moderately deep junctions (100–400 nm) in reducing the depth of the final junction as well as its sheet resistivity. However, the preamorphization step does increase the junction leakage slightly, and, under accumulated-gate biasing, the junction depletion region can intersect defects that are associated with preamorphization to give high tunneling leakage.

The addition of silicides to previously-formed shallow junctions is effective in reducing the diffusion sheet resistivity; however, the dopant evaporation and redistribution associated with silicidation may sufficiently increase the contact resistance to lessen or even negate any overall benefit. Furthermore the silicon consumption and the requirement of a large buffer between the junction depth and the bottom of the silicide to reduce leakage place severe constraints on the scalability of this silicide technology.

The technique of diffusing junctions from silicide sources offers the potential of scaling to even shallower junctions. This technique avoids the silicon crystal damage associated with ion implantation and, because the junction edge conforms to the silicide roughness, the buffer requirement is relaxed. Limitations on the thermal stability of most silicides, especially on poly-Si gates, does restrict this technique as does the low diffusivity and compound formation associated with some dopants in some silicide systems. Furthermore, our understanding of diffusion in silicon resulting from a silicide source requires much further work.

Despite all these potential problems and challenges for the future, considerable success has been shown in producing high-conductivity, low-leakage junctions in the 50–100 nm range.

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REFERENCES

1. C. M. Osburn and A. Reisman, J. Electron. Mater. *16,* 223 (1987).
2. Y. Kim, H. Z. Massoud, and R. B. Fair, J. Electron. Mater. *18,* 143 (1989).
3. K. K. Ng and W. T. Lynch, IEEE Trans. Electron Dev. *Ed-34,* 503 (1987).
4. D. Sharma, S. Goodwin-Johansson, D. S. Wen, C. K. Kim, and C. M. Osburn, Proc. of First Int. Symp. on Ultra Large Scale Integration Sci. and Tech., The Electrochem. Soc., *87-11,* 49 (1987).
5. S. Goodwin-Johansson and M. Kellam, private communications.
6. T. Shibata, K. Hieda, M. Sato, M. Konaka, R. L. M. Dang, and H. Iizuka, IEDM Tech. Digest, 647 (1981).
7. C. M. Osburn, M. Y. Tsai, S. Roberts, C. J. Lucchese, and C. Y. Ting, Proc. 1st Int. Symp. on VLSI Sci. and Tech., Electrochemical Society, *82-1,* 213 (1982).
8. C. K. Lau, Y. C. See, D. B. Scott, J. M. Bridges, S. M. Perna, and R. D. Davies, IEDM Tech. Digest, 714 (1982).
9. F. Runovc, H. Norstrom, R. Buchta, P. Woklund, and S. Petersson, Physica Scripta, *26,* 108 (1982).
10. T. Yamaguchi, S. Morimoto, G. H. Kawamoto, H. K. Park and G. C. Eiden, IEDM Tech. Digest, 522 (1983).
11. K. Maex, R. DeKeersmaecker, P. F. A. Alkemade, F. H. P. M. Habraken, and W. F. van der Weg, Proc. MRS Europe Conference, 315, June (1984).
12. K. Tsukamoto. T. Okamoto, M. Shimizu, T. Matsukawa, and H. Nakata, IEDM Tech. Digest, 130 (1984).
13. D. C. Chen, T. R. Cass, J. E. Turner, P. Merchant, and K. Y. Chiu, IEDM Tech. Digest, 411 (1985).
14. D. C. Chen, T. R. Cass, J. E. Turner, P. Merchant, and K. Y. Chiu, IEEE Trans. Electron Devices, *ED-33,* 1463 (1986).
15. M. E. Alperin, T. C. Holloway, R. A. Haken, C. D. Gosmeyer, R. V. Karnaugh, and W. D. Parmantie, IEEE J. Solid State Circuits, *SC-20,* 61 (1985).

16. J. Amano, K. Mauka, M. P. Scott, and J. E. Turner, Appl. Phys. Lett., *49,* 737 (1986).
17. I. Ohdomari, K. Takano, T. Chikyow, H. Kawarada, J. Nakanishi, and T. Ueno, M. R. S. Symp. Proc. *54,* 63 (1986).
18. K. Maex, R. de Keersmaecker, C. Claeys, J. Vanhellemont, and P. F. A. Alkemade, Proc. of the 5th Inter. Symp. on Silicon Mater. Sci. and Tech., The Electrochem. Soc. *86-4,* 346 (1986).
19. S. M. Hu, Appl. Phys. Lett. *51,* 308 (1987).
20. D. S. Wen, P. L. Smith, C. M. Osburn, and G. A. Rozgonyi, Appl. Phys. Lett., *51,* 1182 (1987).
21. D. S. Wen, P. L. Smith, C. M. Osburn, and G. A. Rozgonyi, J. Electrochem. Soc., *136,* 466 (1989).
22. M. H. Wang, W. Lur, H. C. Cheng, and L. J. Chen, MRS Symp. Proc. *100,* 93 (1988).
23. K. Maex and R. DeKeersmaecker, Proc. 14th ESSDERC, Sept. (1984).
24. K. Maex, R. F. DeKeersmaecker, and P. F. A. Alkemade, MRS Symp. Proc. *45,* 153 (1985).
25. F. C. Shone, K. C. Saraswat, and J. D. Plummer, IEDM Tech. Dig., 407 (1985).
26. D. L. Kwong, D. C. Meyers, and N. S. Alvi, IEEE Electron Dev. Lett., *EDL-6,* 244 (1985).
27. D. L. Kwong, Y. H. Ku, S. K. Lee, and E. Lewis, J. Appl. Phys. *61,* 5084 (1987).
28. H. Gierisch, F. Neppl, E. Franzel, P. Eichinger, and K. Hieber, Proc. MRS Symp., Spring, Palo Alto CA (1986).
29. R. Liu and T. P. H. F. Wendling, Workshop on Refractory Metals and Silicides for VLSI IV, San Juan Bautista, CA, May (1986).
30. R. Liu, D. S. Williams, and W. T. Lynch, IEDM Technical Digest 58, (1986).
31. R. Liu, D. S. Williams, and W. T. Lynch, J. Appl. Phys. *63,* 1990 (1988).
32. S. J. Hillenius, R. Liu, G. E. Georgiou, R. L. Field, D. S. Williams, A. Komblit, D. M. Boulin, R. L. Johnston, and W. T. Lynch, IEDM Tech. Digest, 252 (1986).
33. N. Natsuaki, K. Ohyu, T. Suzuki, N. Kobayashi, N. Hashimoto, and Y. Wada, IEEE 1986 Symp. VLSI Tech., 37 (1986).
34. N. Kobayashi, N. Hashimoto, K. Ohyu, T. Kaga, and S. Iwata, IEEE 1986 Symp. VLSI Tech., 49 (1986).
35. B. M. Ditchek, M. Tabasky, and E. S. Bulat, MRS Symp. Proc. *92,* 199 (1987).
36. J. D. Plummer, Workshop on Refractory Metals and Silicides for VLSI V, San Juan Bautista, CA, May (1987).
37. V. Probst, P. Lippens, L. Van den Hove, K. Maex, H. Schaber, and R. DeKeersmaecker, Proc. 17th ESSDERC, 437, Bologna, Italy, Sept. (1987).
38. R. Liu, F. A. Baiocchi, L. M. Heimbrook, J. Kovalchick, D. L. Malm, D. S. Williams, and W. T. Lynch, Proc. of First Int. Symp. on Ultra Large Scale Integration Sci. and Tech., The Electrochem. Soc. *87-11,* 446 (1987).
39. Y. Taur, B. Davari, D. Moy, J. Y.-C. Sun, and C. Y. Ting, IBM J. Res. Develop. *31,* 627 (1987).
40. B. Davari, Y. Taur, D. Moy, F. M. d'Heurle, and C. Y. Ting, Proc. of First Int. Symp. on Ultra Large Scale Integration Sci. and Tech., The Electrochem. Soc. *87-11,* 368 (1987).
41. Y.-H. Ku, Ph.D Thesis, University of Texas/Austin, May (1988).
42. P. B. Moynagh, A. A. Brown, and P. J. Rosser, J. Phys. *C4,* 187 (1988).
43. L. Van den hove, Ph.D. Thesis, Katholieke Universiteit Leuven, June (1988).
44. D. X. Cao, H. B. Harrison, and G. K. Reeves, MRS Symp. Proc. *100,* 737 (1988).
45. L. M. Rubin, N. Herbots, D. Hoffman, and D. Ma, Proc. MRS Symp., Dec. (1988).
46. P. B. Moynagh, A. A. Brown, and P. J. Rosser, Proc. MRS Symp., Spring, San Diego (1989).
47. H. Jiang, P. Smith, D. Griffis, Z.-G. Xiao, C. M. Osburn, G. McGuire, and G. A. Rozgonyi, presented at Electrochem. Soc. Annual Meeting, Los Angeles, CA., May (1989).
48. S. Nygren and S. Johansson, submitted to J. Appl. Phys.
49. L. Van den hove, P. Lippins, K. Maex, L. Hobbs, and R. DeKeersmaecker, European Workshop on Refractory Metals and Silicides, Leuven, Belgium, *A.2.2,* April (1989).
50. N. F. Stogdale and K. J. Barlow, European Workshop on Refractory Metals and Silicides, Leuven, Belgium, *A.2.6,* April (1989).
51. E. A. Maydell-Ondrusz, R. E. Harper, I. H. Wilson, and K. G. Stephens, Vacuum. *34,* 995 (1984).
52. O. W. Holland, D. Fathy, S. P. Withrow, and T. P. Sjoreen, J. Vac. Sci. Technol. B *6,* 569 (1988).
53. K. Cho, W. R. Allen, T. G. Finstad, W. K. Chu, J. Liu, and J. J. Wortman, Nucl. Instrm. Methods Phys. Res. B *7/8,* 265 (1985).
54. B-Y. Tsaur and C. H. Anderson, Jr., J. Appl. Phys. *54,* 6336 (1983).
55. I. D. Calder, H. M. Naguib, D. Houghton, and F. R. Shepherd, Mater. Res. Soc. Symp. Proc. 35, 353 (1985).
56. D. K. Sadana, W. Maszara, J. J. Wortman, G. A. Rozgonyi, and W. K. Chu, J. Electrochem. Soc. *131,* 943 (1984).
57. M. Delfino, D. K. Sadana, and A. E. Morgan, Appl. Phys. Lett. *49,* 575 (1986).
58. E. Ganin, G. Scilla, T. O. Sedgwick, and G. A. Sai-Halasz, Ext. Abstract, M.R.S. Fall Meeting, 50 (1986).
59. J. Liu, J. Wortman, and R. Fair, Digest of the 41st Annual IEEE Res. Conf. June (1985).
60. A. A. Naem and I. D. Calder, J. Appl. Phys. *62,* 569 (1987).
61. I.-W Wu, R. T. Fulks, and J. C. Mikkelsen, Jr., J. Appl. Phys. *60,* 2422 (1986).
62. P. K. Vasudev, A. E. Schmidtz, and G. L. Olson, MRS Symp. Proc. *35,* 367 (1984).
63. R. G. Wilson, J. Appl. Phys., *54,* 6879 (1983).
64. M. C. Ozturk, J. J. Wortman, A. Ajmera, and G. Rozgonyi, Abstract Mater. Res. Soc. Spring Mg., 48 (1987).
65. A. Ajmera and G. Rozgonyi, Appl. Phys. Lett. *49,* 1269 (1986).
66. M. C. Ozturk, J. J. Wortman, C. M. Osburn, A. Ajmera, G. Rozgonyi, E. Frey, W. K. Chu, and C. Lee, IEEE Trans. Electron Dev. *35,* 659 (1988).
67. S. D. Brotherton, J. R. Ayres, J. B. Clegg, and J. P. Gowers, J. Electron. Mater. *18,* 173 (1989).
68. M. Miyake, S. Aoyama, S. Hirota, and T. Kobayashi, J. Electrochem. Soc. *135,* 2872 (1988).
69. S. Chevacharoenkul, C. M. Osburn, and G. McGuire, in preparation.
70. R. B. Fair, "PREDICT: Process Estimator for the Design of Integrated Circuit Technologies," Microelectronics Center of North Carolina, (1986).
71. S.-N. Hong, G. A. Ruggles, J. J. Wortman, E. Myers, and J. J. Hren, submitted to Electron. Lett. (1989).
72. Y. Oowaki, Y. Itoh, M. Momodomi, F. Horiguchi, S. Watanabe, M. Ogura, and H. Nishimura, IEDM Dig. Tech. Papers. 492 (1985).
73. R. W. Gregor, IEEE Electron Devices Lett. *EDL-7,* 677 (1986).
74. T. Y. Chan, A. T. Wu, P. K. Ko, C. Hu, and R. R. Razouk, IEEE Electron Devices Lett. *EDL-7,* 16 (1986).
75. T. Y. Chan, A. T. Wu, P. K. Ko, and C. Hu, IEEE Electron Devices Lett. *EDL-8,* 326 (1987).
76. D. S. Wen, Ph.D. Thesis, North Carolina State University, May (1988).
77. M. Nakano, Electrochem. Soc. *89-,* 123 (1989).
78. D. S. Wen, S. Goodwin-Johansson, and C. M. Osburn, IEEE Trans. on Elec. Dev. *35,* 1107 (1988).
79. S. Ogura, P. Tsang, W. Walker, D. Critchlow, and J. Shepard, IEEE Trans. Electron Devices, *ED-27,* 1359 (1980).
80. P. J. Tsang, S. Ogura, W. W. Walker, J. F. Shepard, and D. Critchlow, IEEE Trans. Electron Devices *ED-29,* 590 (1982).
81. J. Riseman, U.S. Patent 4234362 (1980).
82. J. J. Sanchez, K. K. Hsueh, and T. A. DeMassa, IEEE Trans. Electron Devices *ED-36,* 1125 (1989).
83. M. C. Ozturk, Ph.D. Thesis, North Carolina State University, (1988).
84. C. M. Osburn, S. Chevacharoenkul, G. McGuire, J. Fulghum, and D. Griffis, in preparation.
85. R. B. Fair, "Diffusion and Oxidation of Silicon," in *Microelectronics Processing,* eds. D. W. Hess and K. F. Jensen, Adv. in Chem. Series 221 (American Chemical Society), 265 (1989).
86. B. Hamilton, T. O. Sedgwick, and J. C. Gelpey, MRS Soc. Symp. Proc. *100,* 323 (1988).

87. J. Chen, T. Y. Chan, I. C. Chen, P. K. Ko, and C. Hu, IEEE Elec. Dev. Lett. *EDL-8,* 515 (1987).
88. T. Y. Chan, J. Chen, P. K. Ko and C. Hu, Tech. Digest IEDM, 718 (1987).
89. C. Chang and J. Lien, Tech. Digest IEDM, 714 (1987).
90. C. M. Osburn, A. Cramer, A. M. Schwieghart, and M. R. Wordeman, Proc. of First Int. Symp. on Very Large Scale Integration Sci. Tech., The Electrochem. Soc. *82-7,* 354 Detroit (1982).
91. D. Flowers, J. Electrochem. Soc. *134,* 698 (1987).
92. H. L. Peek, and D. Wolters, Ext. Abs. 18th Conf. Solid State Devices and Mater. 487, Tokyo (1986).
93. H. L. Peek, and J. F. Verwey, Insulating Films on Semiconductors, eds. J. J. Simone, and J. Buxo, Elsevier Science Publishers B. V., North Holland, (1986).
94. M. Stinson and C. Osburn, unpublished.
95. M. Lenzlinger and E. H. Snow, J. Appl. Phys, *40,* 278 (1969).
96. M. Stinson and C. M. Osburn, unpublished.
97. P. E. Bakeman and A. F. Puttlitz, Nuclear Instrum. Methods Phys. Res. *B6, 399* (1085).
98. V. Basra, C. M. McKenna, and S. B. Felch, Nuclear Instrum. Methods Phys. Res. *B21,* 360 (1987).
99. S. B. Felch, V. Basra, and C. M. McKenna, IEEE Trans. Electron Devices. *ED-35,* 2338 (1988).
100. W. Vandervorst, H. E. Maes, and R. F. DeKeersmaecker, J. Appl. Phys. *56,* 1425 (1984).
101. D. J. Godfrey, R. D. Groves, M. G. Dowsett, and A. F. W. Willoughby, Physica *129B,* 181 (1985).
102. J. E. Turner and J. Amano, Appl. Phys. Lett. *50,* 1601 (1987).
103. S. Clayton, B. Offord, T. Sedgwick, R. Reedy, A. Michel, and G. Scilla, Electron. Lett. *24,* 831 (1988).
104. A. Casel and H. Jorke, Appl. Phys. Lett. *50,* 989 (1987).
105. *J. B. Clegg, Surf. Interface Analysis 10, 332 (1987).*
106. H. H. Anderson, App. Phys. *18,* 131 (1979).
107. H. Frenzel, E. Frenzel, and P. Davies, Springer Series in Chemical Physics: SIMS V, ed. A. Benninghover, R. J. Cotton, D. S. Simons, and H. W. Werner *44,* 316, (1989).
108. J. L. Hunter, Jr., S. F. Corcoran, D. P. Griffis, and C. M. Osburn, Am. Vac. Soc., 36th Nat. Symp., Oct. (1989).
109. J. J. Lee, J. E. Fulghum, G. E. McGuire, M. A. Ray, C. M. Osburn, and R. W. Linton, Am. Vac. Soc., 36th Nat. Symp., Oct. (1989).
110. S. M. Hu, J. Appl. Phys. *53,* 1499 (1982).
111. G. G. Sweeney, and T. R. Alvarez in *Emerging Semiconductor Technology* ed. by D. C. Gupta and P. A. Langer, Am. Soc. T. Mater. *STP 960,* 521 (1986).
112. J. R. Ehrestein in *Emerging Semiconductor Technology* ed. by D. C. Gupta and P. A. Langer, Am. Soc. T. Mater. *STP 960,* 453 (1986).
113. J. Albers in *Emerging Semiconductor Technology* ed. by D. C. Gupta and P. A. Langer, Am. Soc. T. Mater. *STP 960,* 480 (1986).
114. M. Pawlik in *Emerging Semiconductor Technology* ed. by D. C. Gupta and P. A. Langer, Am. Soc. T. Mater. *STP 960,* 502 (1986).
115. C. M. Osburn, T. Brat, D. Sharma, N. Parikh, W.-K. Chu, D. Griffis, S. Corcoran, and S. Lin, J. Electrochem. Soc. *135,* 1490 (1988).
116. P. Fahey and R. W. Dutton, Appl. Phys. Lett. *52,* 1092 (1988).
117. L. Van den hove, J. Vanhellemont, R. Wolters, W. Classen, R. DeKeersmaecker, and G. Declerk, Proc. of First Int. Symp. on Adv. Mater. for ULSI, Electrochem. Soc. *88-19,* 165 (1988).
118. C. M. Osburn, P. Smith, D.-S Wen, G. McGuire, S. Chevacharoenkul, and J.-B Yan, M.R.S. Mtg., Dec. (1989).
119. E. K. Broadbent, R. Irani, and A. E. Morgan, Proc. IEEE V-MIC, 175 (1988).
120. E. K. Broadbent, M. Delfino, A. E. Morgan, D. K. Sadana, and P. Maillot, IEEE Electron Device Lett. *EDL-6,* 318 (1987).
121. M. Wittmer, C.-Y. Ting, I. Ohdonari, and K. N. Tu, J. Appl. Phys. *53,* 6781 (1982).
122. Z.-G Xiao, H. Jiang, J. Honeycutt, G. Rozgonyi, C. M. Osburn, and G. McGuire, presented at Electrochem. Soc. Annual Mtg., Los Angeles, CA, May (1989).
123. C. Y. Ting, F. M. d'Heurle, S. S. Iyer, and P. M. Fryer, J. Electrochem. Soc. *133,* 2621 (1986).
124. C. Y. Ting and S. S. Iyer, Proc. IEEE V-MIC, 307 (1985).
125. C. Y. Wong, L. K. Wang, and P. A. McFarland, J. Electrochem, Soc., Ext. Abs. *85, 466* (1985).
126. L. R. Zheng, L. S. Hung, and J. W. Mayer, Appl. Phys. Lett. *41,* 646 (1982).
127. M. Y. Tsai, C. S. Petersson, F. M. d'Heurle and V. Maniscalco, Appl. Phys. Lett. *37,* 295 (1980).
128. F. M. d'Heurle, C. S. Petersson, and M. Y. Tasi, J. Appl. Phys. *51,* 5976 (1980).
129. F. M. d'Heurle, M. Y. Tasi, C. S. Petersson, and B. Stritzker, J. Appl. Phys. *53,* 3069 (1982).
130. L. S. Wielunski, C. D. Lien, B. X. Liu, and M.-A. Nicolet, J. Vac. Sci. Technol. *20,* 182 (1982).
131. A. H. Hamdi and M.-A Nicolet, Thin Solid Films *119,* 357 (1984).
132. H. Okabayashi, M. Morimoto, and E. Nagasawa, IEEE Trans. Electron Devices *ED-31,* 1329 (1984).
133. B. Y. Tsaur, C. K. Chen, C. H. Anderson, Jr., and D. L. Kwong, J. Appl. Phys., submitted.
134. M. Delfino, E. K. Broadbent, A. E. Morgan, B. J. Burrow, and M. H. Norcott, IEEE Electron Device Lett. *EDL-6,* 591 (1985).
135. D. L. Kwong, D. C. Meyers, and N. S. Alvi, 2nd Int. Symp. on VLSI Science and Technol., Electrochem. Soc. *85-,* 195 (1985).
136. D. L. Kwong, D. C. Meyers, and N. S. Alvi, IEEE Electron Device Lett. *EDL-6,* 244 (1985).
137. D. L. Kwong, D. C. Meyers, N. S. Alvi, L. W. Li, and E. *Norbeck, Appl. Phys. Lett. 47, 688 (1985).*
138. L. R. Zheng, L. S. Hung, J. W. Mayer, and K. W. Choi, Nucl. Instrum. Methods Phys. Res. *B7/8,* 413 (1985).
139. K. Maex, L. Van den hove, and R. F. der Keersmaecker, Thin Solid Films *140,* 149 (1986).
140. D. L. Kwong and N. S. Alvi, J. Appl. Phys. *60,* 688 (1986).
141. N. Yu, Z. Zhou, W. Zhou, S. Tsou, and D. Zhu, Nucl. Instrum. Methods Phys. Res. *B19/20,* 427 (1987).
142. A. E. Morgan, E. K. Broadbent, M. Delfinio, B. Coulman, and D. K. Sadana, J. Electrochem. Soc. *134,* 925 (1987).
143. E. Nagasawa, H. Okabayashi, and M. Morimoto, IEEE Trans. Electron Devices *ED-34,* 581 (1987).
144. H. Jiang, C. M. Osburn, Z.-G. Xiao, G. A. Rozgonyi, G. McGuire, ESSDERC, Berlin W. Germany, Sept (1989).
145. H. J. Bohm, H. Wendt, and H. Oppolzer, K. Masseli, and R. Kassing, J. Appl. Phys. *62,* 2784 (1987).
146. M. Delfino, J. G. deGroot, K. N. Ritz, and P. Maillot, J. Electrochem. Soc. *136,* 215 (1989).
147. D. E. Burke and S.-Y. Yung, to be published Solid-State Electron., (1988).
148. M. Delfino, A. E. Morgan, P. Maillot, E. K. Broadbent, J. Appl. Phys. *64,* 607 (1988).
149. H. Ishiwara, *Thin Film Interfaces and Interactions,* ed. by J. E. E. Baglin and J. M. Poate, The Electrochem. Soc., 159 (1980).
150. P. Gas, V. Deline, F. M. d'Heurle, A. Michel, and G. Scilla, J. Appl. Phys. *60,* 1634 (1986).
151. O. Thomas, P. Gas, F. M. d'Heurle, F. G. LeFoues, A Michel, and G. Scilla, J. Vac. Sci. Technol. A *6,* 1736 (1988).
152. O. Thomas, P. Gas, A. Charai, F. K. LeGoues, A. Michel, G. Scilla and F. M. d'Heurle, J. Appl. Phys. *64,* 2973 (1988).
153. A. H. van Ommen, H. J. W. vanHoutum, and A. M. L. Theunissen, J. Appl. Phys. *60,* 627 (1986).
154. J. Amano, P. Merchant, T. R. Cass, J. N. Miller, and T. Koch, J. Appl. Phys. *59,* 2689 (1986).
155. J. Narayan, T. A. Stephenson, T. Brat, D. Fathy, and S. J. Pennycook, J. Appl. Phys. *60,* 631 (1986).
156. F. J. Morin and J. P. Maita, Phys. Rev. *94,* 1525 (1954).
157. R. B. Fair, J. Appl. Phys. *43,* 1278 (1972).
158. M. Arienzo, private communication.